

Precision Analog Front Ends

FEATURES

- Precision (up to 17 Bits) A/D Converter "Front End"
- 3-Pin Control Interface to Microprocessor
- Flexible: User Can Trade-Off Conversion Speed for Resolution
- Single Supply Operation (TC510/514)
- 4 Input, Differential Analog MUX (TC514)
- Automatic Input Voltage Polarity Detection
- Low Power Dissipation TC500/500A: 10mW
TC510/514: 18mW
- Wide Analog Input Range $\pm 4.2V$ (TC500A/510)
- Directly Accepts Bipolar and Differential Input Signals

ORDERING INFORMATION

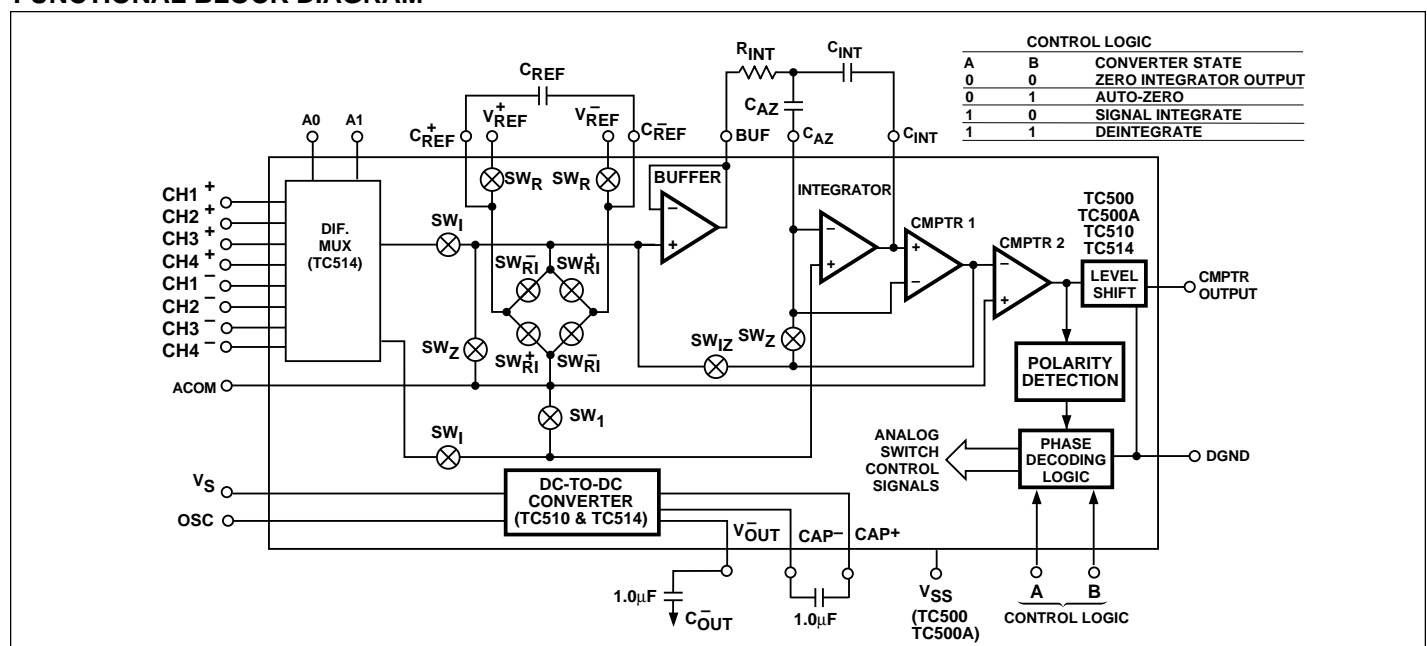
Part No.	Package	Temp. Range
TC500ACOE	16-Pin SOIC	0°C to +70°C
TC500ACPE	16-Pin Plastic DIP (Narrow)	0°C to +70°C
TC500COE	16-Pin SOIC	0°C to +70°C
TC500CPE	16-Pin Plastic DIP (Narrow)	0°C to +70°C
TC510COG	24-Pin SOIC	0°C to +70°C
TC510CPF	24-Pin Plastic DIP (300 Mil.)	0°C to +70°C
TC514COI	28-Pin SOIC	0°C to +70°C
TC514CPJ	28-Pin Plastic DIP (300 Mil.)	0°C to +70°C
TC500EV	Evaluation Kit for TC500/500A/510/514	

GENERAL DESCRIPTION

The TC500/500A/510/514 family are precision analog front ends that implement dual slope A/D converters having a maximum resolution of 17 bits plus sign. As a minimum, each device contains the integrator, zero crossing comparator and processor interface logic. The TC500 is the base (16 bit max) device and requires both positive and negative power supplies. The TC500A is identical to the TC500, except it has improved linearity allowing it to operate to a maximum resolution of 17 bits. The TC510 adds an on-board negative power supply converter for single supply operation. The TC514 adds both a negative power supply converter and a 4 input differential analog multiplexer.

Each device has the same processor control interface consisting of 3 wires: control inputs A and B and zero-crossing comparator output (CMPTR). The processor manipulates A, B to sequence the TC5xx through four phases of conversion: Auto Zero, Integrate, Deintegrate and Integrator Zero. During the Auto Zero phase, offset voltages in the TC5xx are corrected by a closed-loop feedback mechanism. The input voltage is applied to the integrator during the Integrate phase. This causes an integrator output dv/dt directly proportional to the magnitude of the input voltage. The higher the input voltage, the greater the magnitude of the voltage stored on the integrator during this phase. At the start of the Deintegrate phase, an external voltage reference is applied to the integrator, and at the same time, the external host processor starts its on-board timer. The processor

FUNCTIONAL BLOCK DIAGRAM



**TC500
TC500A
TC510
TC514**

GENERAL DESCRIPTION (Cont.)

maintains this state until a transition occurs on the CMPTR output, at which time the processor halts its timer. The resulting timer count is the converted analog data. Integrator Zero (the final phase of conversion) removes any residue remaining in the integrator in preparation for the next conversion.

The TC500/500A/510/514 offer high resolution (up to 17 bits) superior 50Hz/60Hz noise rejection, low power operation, minimum I/O connections, low input bias currents and lower cost compared to other converter technologies having similar conversion speeds.

ABSOLUTE MAXIMUM RATINGS*

TC510/514 Positive Supply Voltage (V _{DD} to GND)	+10.5V
TC500/500A Supply Voltage (V _{DD} to V _{SS})	+18V
TC500/500A Positive Supply Voltage (V _{DD} to GND)	+12V

TC500/500A Negative Supply Voltage

(V _{SS} to GND)	- 8V
Analog Input Voltage (V _{IN} or V _{IN})	V _{DD} to V _{SS}
Logic Input Voltage	V _{DD} +0.3V to GND - 0.3V
Voltage on OSC	- 0.3V to (V _{DD} +0.3V) for V _{DD} < 5.5V
Ambient Operating Temperature Range	0°C to +70°C
Storage Temperature Range	- 65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

* Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: TC510/514: V_{DD} = +5V, TC500/500A: V_S = ±5V unless otherwise specified. C_{AZ} = C_{REF} = 0.47 μF

Symbol	Parameter	Test Conditions	T _A = +25°C			T _A = 0°C to +70°C			Unit
			Min	Typ	Max	Min	Typ	Max	
Analog									
	Resolution	Note 1	60	—	—	—	—	—	μV
ZSE	Zero-Scale Error with Auto Zero Phase	TC500/510/514 TC500A	—	—	0.005 0.003	—	0.005 0.003	0.012 0.009	% F.S.
ENL	End Point Linearity	TC500/510/514, Notes 1, 2, TC500A	—	0.005	0.015 0.010	—	0.015 0.010	0.060 0.045	% F.S. % F.S.
NL	Best Case Straight Line Linearity	TC500/510/514, Notes 1, 2, TC500A	—	0.003	0.008 0.005	—	—	—	% F.S. % F.S.
ZS _{TC}	Zero-Scale Temperature Coefficient	Over Operating Temperature Range	—	—	—	—	1	2	μV/°C
SYE	Full-Scale Symmetry Error (Roll-Over Error)	Note 3	—	0.01	—	—	0.03	—	% F.S.
FS _{TC}	Full-Scale Temperature Coefficient	Over Operating Temperature Range External Reference TC = 0ppm/°C	—	—	—	—	10	—	ppm/°C
I _{IN}	Input Current	V _{IN} = 0V	—	6	—	—	—	—	pA
V _{CMR}	Common-Mode Voltage Range		V _{SS} +1.5	—	V _{DD} - 1.5	V _{SS} +1.5	—	V _{DD} - 1.5	V
	Integrator Output Swing		V _{SS} +0.9	—	V _{DD} - 0.9	V _{SS} +0.9	—	V _{SS} +0.9	V
	Analog Input Signal Range	ACOM = GND = 0V	V _{SS} +1.5	—	V _{DD} - 1.5	V _{SS} +1.5	—	V _{SS} +1.5	V
V _{REF}	Voltage Reference Range	V _{REF} V _{REF}	V _{SS} +1	—	V _{DD} - 1	V _{SS} +1	—	V _{DD} - 1	V

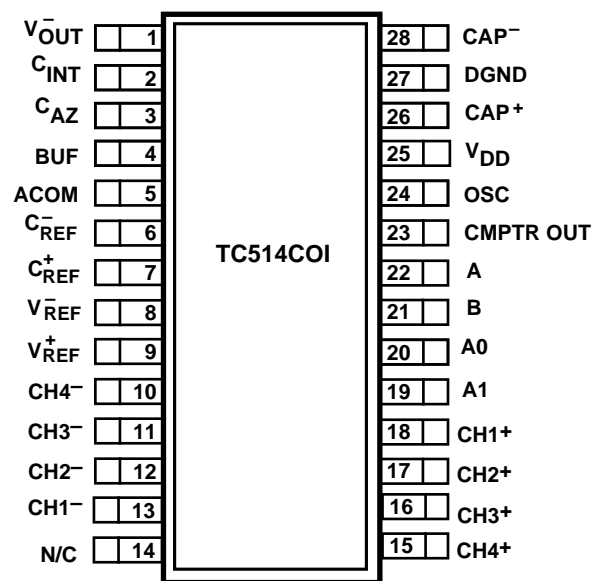
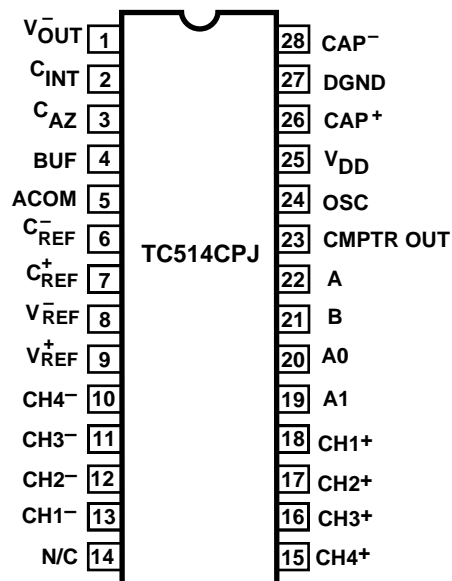
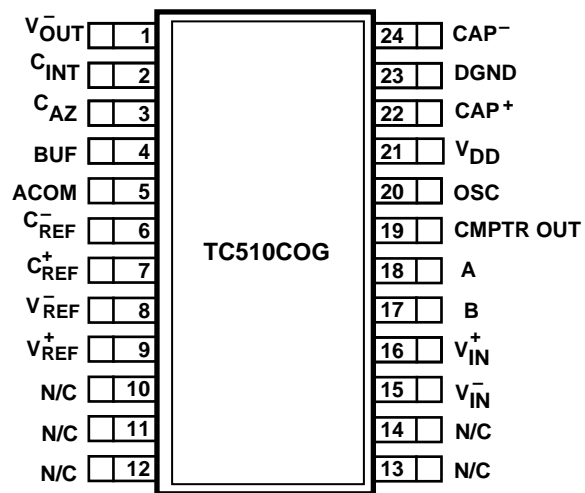
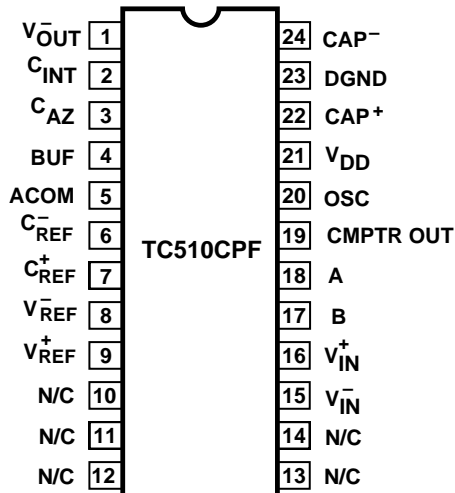
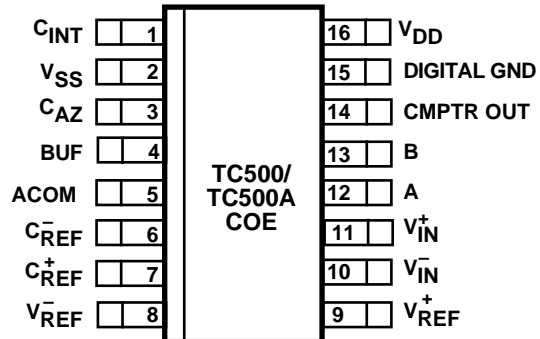
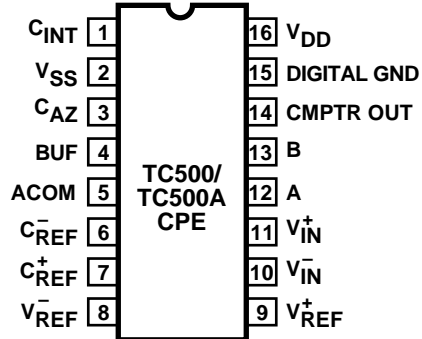
ELECTRICAL CHARACTERISTICS: (Cont.)

Symbol	Parameter	Test Conditions	T _A = +25°C			T _A = 0°C to +70°C			Unit
			Min	Typ	Max	Min	Typ	Max	
Digital									
V _{OH}	Comparator Logic 1, Output High	I _{SOURCE} = 400μA	4	—	—	4	—	—	V
V _{OL}	Comparator Logic 0, Output Low	I _{SINK} = 2.1mA	—	—	0.4	—	—	0.4	V
V _{IH}	Logic 1, Input High Voltage		3.5	—	—	3.5	—	—	V
V _{IL}	Logic 0, Input Low Voltage		—	—	1	—	—	1	V
I _L	Logic Input Current	Logic 1 or 0	—	—	—	—	0.3	—	μA
t _D	Comparator Delay		—	2	—	—	3	—	μsec
Multiplexer (TC514 Only)									
	Maximum Input Voltage	V _{DD} = 5V	-2.5	—	2.5	-2.5	—	2.5	V
R _{DS(ON)}	Drain/Source ON Resistance	V _{DD} = 5V	—	6	10	—	—	—	kΩ
Power (TC510/514 Only)									
I _S	Supply Current	V _{DD} = 5V, A = 1, B = 1	—	1.8	2.4	—	—	3.5	mA
P _D	Power Dissipation	V _{DD} = 5V	—	18	—	—	—	—	mW
V _{DD}	Positive Supply Operating Voltage Range		4.5	—	5.5	4.5	—	5.5	V
R _{OUT}	Operating Source Resistance	I _{OUT} = 10mA	—	60	85	—	—	100	Ω
	Oscillator Frequency	(Note 3)	—	100	—	—	—	—	kHz
I _{OUT}	Maximum Current Out	V _{DD} = 5V	—	—	-10	—	—	-10	mA
Power (TC500/500A Only)									
I _S	Supply Current	V _S = ±5V, A = B = 1	—	1	1.5	—	—	2.5	mA
P _D	Power Dissipation	V _{DD} = 5V, V _{SS} = -5V	—	10	—	—	—	—	mW
V _{DD}	Positive Supply Operating Voltage Range		4.5	—	7.5	4.5	—	7.5	V
V _{SS}	Negative Supply Operating Voltage Range		-4.5	—	-7.5	-4.5	—	-7.5	V

- NOTES:**
1. Integrate time ≥ 66msec, auto-zero time ≥ 66msec, V_{INT} (peak) ≈ 4V.
 2. End point linearity at ±1/4, ±1/2, ±3/4 F.S. after full-scale adjustment.
 3. Roll-over error is related to C_{INT}, C_{REF}, C_{AZ} characteristics.

TC500
TC500A
TC510
TC514

PIN CONFIGURATIONS



PIN DESCRIPTION

Pin No. (TC500, 500A)	Pin No. (TC510)	Pin No. (TC514)	Symbol	Description
1	2	2	C _{INT}	Integrator output. Integrator capacitor connection.
2	Not Used	Not Used	V _{SS}	Negative power supply input (TC500/500A only).
3	3	3	C _{AZ}	Auto-zero input. The Auto-zero capacitor connection.
4	4	4	BUF	Buffer output. The Integrator capacitor connection.
5	5	5	ACOM	This pin is grounded in most applications. It is recommended that ACOM and the input common pin (V _{IN} or C _{FN}) be within the analog common mode range (CMR).
6	6	6	C _{REF} ⁻	Input. Negative reference capacitor connection.
7	7	7	C _{REF} ⁺	Input. Positive reference capacitor connection.
8	8	8	V _{REF} ⁻	Input. External voltage reference (-) connection.
9	9	9	V _{REF} ⁺	Input. External voltage reference (+) connection.
10	15	Not Used	V _{IN} ⁻	Negative analog input.
11	16	Not Used	V _{IN} ⁺	Positive analog input.
12	18	22	A	Input. Converter phase control MSB. (See input B.)
13	17	21	B	Input. Converter phase control LSB. The states of A, B place the TC5xx in one of four required phases. A conversion is complete when all four phases have been executed: Phase control input pins: AB = $\left\{ \begin{array}{l} 00: \text{Integrator Zero} \\ 01: \text{Auto Zero} \\ 10: \text{Integrate} \\ 11: \text{Deintegrate} \end{array} \right.$
14	19	23	CMPTR OUT	Zero crossing comparator output. CMPTR is HIGH during the Integration phase when a <u>positive</u> input voltage is being integrated and is LOW when a negative input voltage is being integrated. A HIGH-to-LOW transition on CMPTR signals the processor that the Deintegrate phase is completed. CMPTR is undefined during the Auto-Zero phase. It should be monitored to time the Integrator Zero phase (see text).
15	23	27	DGND	Input. Digital ground.
16	21	25	V _{DD}	Input. Power supply positive connection.
	22	26	CAP ⁺	Input. Negative power supply converter capacitor (+) connection.
	24	28	CAP ⁻	Input. Negative power supply converter capacitor (-) connection.
	1	1	V _{OUT} ⁻	Output. Negative power supply converter output and reservoir capacitor connection. This output can be used to power other devices in the circuit requiring a negative bias voltage.
	20	24	OSC	Oscillator control input. The negative power supply converter normally runs at a frequency of 100kHz. The converter oscillator frequency can be slowed down (to reduce quiescent current) by connecting an external capacitor between this pin and V _{DD} . (See Typical Characteristics Curves).
		18	CH1 ⁺	Positive analog input pin. MUX channel 1.
		13	CH1 ⁻	Negative analog input pin. MUX channel 1.
		17	CH2 ⁺	Positive analog input pin. MUX channel 2.
		12	CH2 ⁻	Negative analog input pin. MUX channel 2.
		16	CH3 ⁺	Positive analog input pin. MUX channel 3.
		11	CH3 ⁻	Negative analog input pin. MUX channel 3.
		15	CH4 ⁺	Positive analog input pin. MUX channel 4.

TC500
TC500A
TC510
TC514

PIN DESCRIPTION (Cont.)

Pin No (TC500/A)	Pin No (TC510)	Pin No (TC514)	Symbol	Description
		10	CH4 ⁻	Negative analog input pin. MUX channel 4
		20	A0	Multiplexer input channel select input LSB. (See A1).
		19	A1	Multiplexer input channel select input MSB.
				Phase control input pins: A1, A0 = $\begin{cases} 00 = \text{Channel 1} \\ 01 = \text{Channel 2} \\ 10 = \text{Channel 3} \\ 11 = \text{Channel 4} \end{cases}$

GENERAL THEORY OF OPERATION

Dual-Slope Conversion Principles (Figure 2)

Actual data conversion is accomplished in two phases: input signal Integration and reference voltage Deintegration.

The integrator output is initialized to 0V prior to the start of Integration. During Integration, analog switch S1 connects V_{IN} to the integrator input where it is maintained for a fixed time period (t_{INT}). The application of V_{IN} causes the integrator output to depart 0V at a rate determined by the magnitude of V_{IN} , and a direction determined by the polarity of V_{IN} . The Deintegration phase is initiated immediately at the expiration of t_{INT} .

During Deintegration, S1 connects a reference voltage (having a polarity opposite that of V_{IN}) to the integrator input. At the same time, an external precision timer is started. The Deintegration phase is maintained until the comparator output changes state, indicating the integrator has returned to its starting point of 0V. When this occurs, the precision timer is stopped. The Deintegration time period (t_{DEINT}), as measured by the precision timer, is directly proportional to the magnitude of the applied input voltage.

A simple mathematical equation relates the Input Signal, Reference Voltage and Integration time:

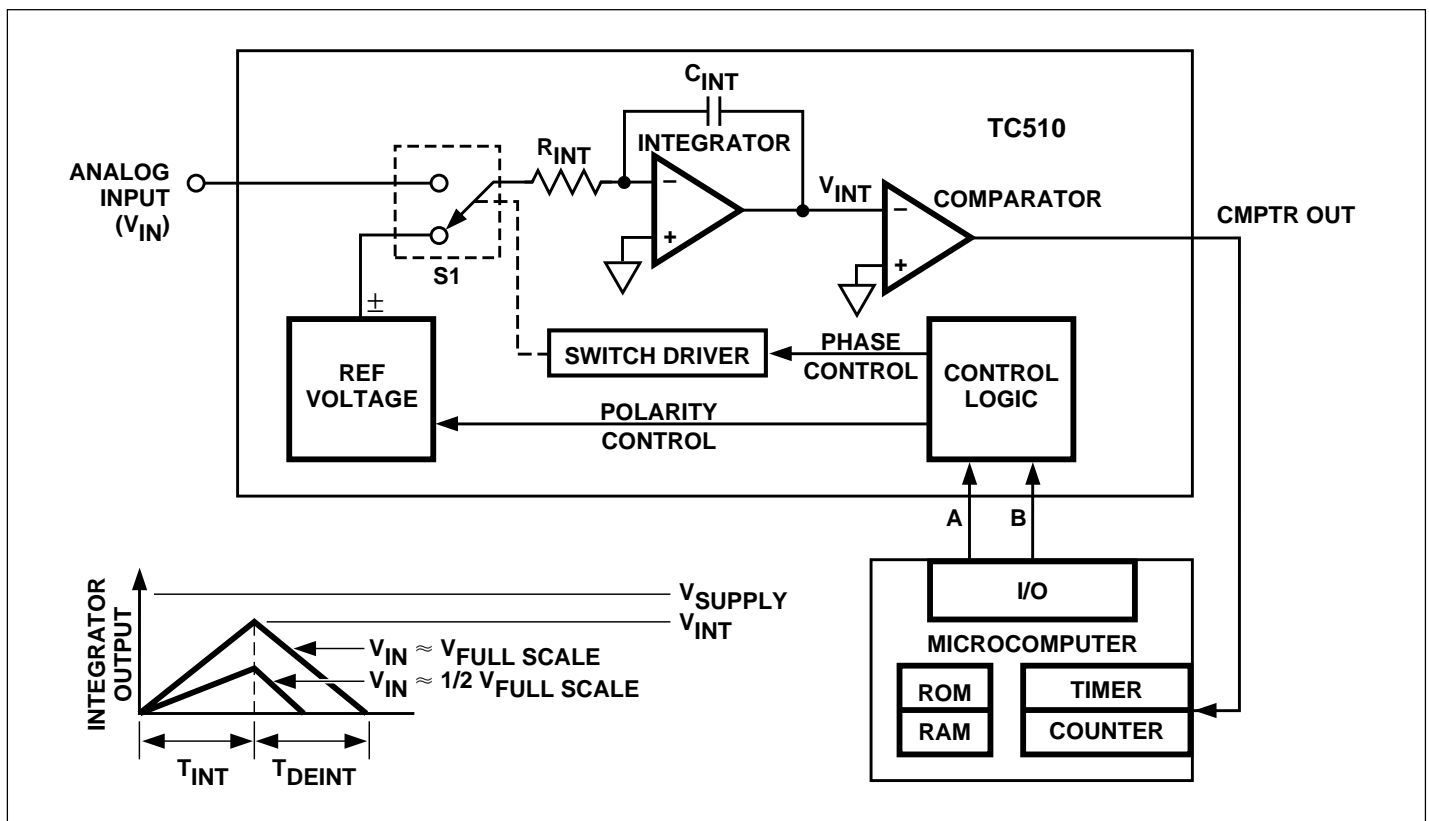


Figure 2. Basic Dual-Slope Converter

$$\frac{1}{R_{INT} C_{INT}} \int_0^{t_{INT}} V_{IN}(t) dt = \frac{V_{REF} t_{DEINT}}{R_{INT} C_{INT}}$$

where:

- V_{REF} = Reference Voltage
- t_{INT} = Signal Integration time (fixed)
- t_{DEINT} = Reference Voltage Integration time (variable)

For a constant V_{IN} :

$$V_{IN} = V_{REF} \frac{t_{DEINT}}{t_{INT}}$$

The dual-slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle.

An inherent benefit is noise immunity. Input noise spikes are integrated (averaged to zero) during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high-noise environments.

Integrating converters provide inherent noise rejection with at least a 20dB/decade attenuation rate. Interference signals with frequencies at integral multiples of the integration period are, theoretically, completely removed since the average value of a sine wave of frequency (1/t) averaged over a period (t) is zero.

Integrating converters often establish the integration period to reject 50/60Hz line frequency interference signals. The ability to reject such signals is shown by a normal mode rejection plot (Figure 4). Normal mode rejection is limited in practice to 50 to 65dB, since the line frequency can deviate by a few tenths of a percent (Figure 3).

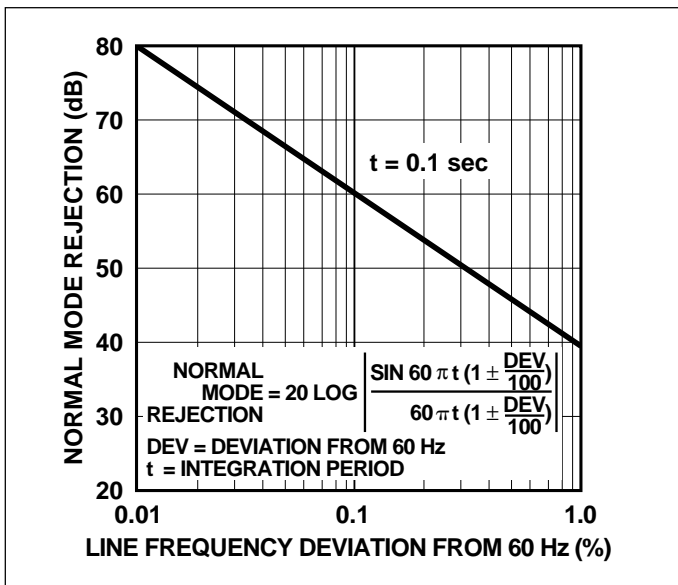


Figure 3. Line Frequency Deviation

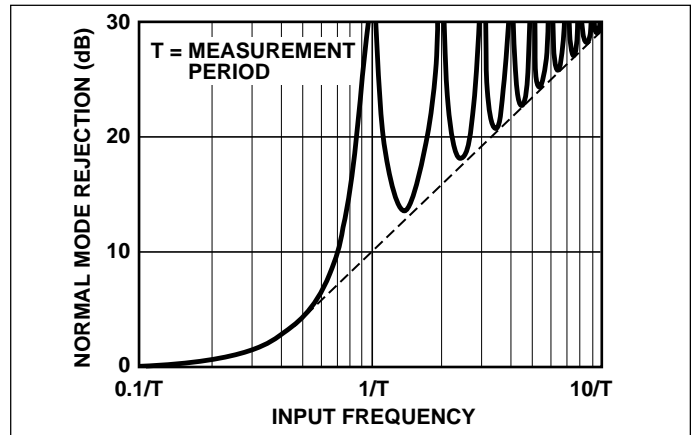


Figure 4. Integrating Converter Normal Mode Rejection

TC500/500A/510/514 CONVERTER OPERATION

The TC500/500A/510/514 incorporates an Auto zero and Integrator phase in addition to the input signal Integrate and reference Deintegrate phases. The addition of these phases reduce system errors and calibration steps, and shorten overrange recovery time. A typical measurement cycle uses all four phases in the following order:

- (1) Auto zero
- (2) Input signal integration
- (3) Reference deintegration
- (4) Integrator output zero

The internal analog switch status for each of these phases is summarized in Table 1. This table is referenced to the *Functional Block Diagram* on the first page of this data sheet.

Auto-Zero Phase (AZ)

During this phase, errors due to buffer, integrator and comparator offset voltages are nulled out by charging C_{AZ} (auto-zero capacitor) with a compensating error voltage.

The external input signal is disconnected from the internal circuitry by opening the two SW_I switches. The internal input points connect to analog common. The reference capacitor is charged to the reference voltage potential through SW_R . A feedback loop, closed around the integrator and comparator, charges the C_{AZ} capacitor with a voltage to compensate for buffer amplifier, integrator and comparator offset voltages.

TC500
TC500A
TC510
TC514

Table 1. Internal Analog Gate Status

Internal Analog Gate Status							
Conversion Phase	SW _I	SW _{RI} ⁺	SW _{RI} ⁻	SW _Z	SW _R	SW ₁	SW _{IZ}
Auto-Zero (A = 0, B = 1)				Closed	Closed	Closed	
Input Signal Integration (A = 1, B = 0)	Closed						
Reference Voltage		Closed*				Closed	
Deintegration (A = 1, B = 1)							
Integrator Output Zero (A = 0, B = 0)					Closed	Closed	Closed

*Assumes a positive polarity input signal. SW_{RI}⁻ would be closed for a negative input signal.

Analog Input Signal Integration Phase (INT)

The TC5xx integrates the differential voltage between the (V_{IN}⁺) and (V_{IN}⁻) inputs. The differential voltage must be within the device's common-mode range V_{CMR}.

The input signal polarity is normally checked via software at the end of this phase: CMPTR = 1 for positive polarity; CMPTR = 0 for negative polarity.

Reference Voltage Deintegration Phase (DINT)

The previously charged reference capacitor is connected with the proper polarity to ramp the integrator output back to zero. An externally-provided, precision timer is used to measure the duration of this phase. The resulting time measurement is proportional to the magnitude of the applied input voltage.

Integrator Output Zero Phase (IZ)

This phase guarantees the integrator output is at 0V when the Auto Zero phase is entered and that only system offset voltages are compensated. This phase is used at the end of the reference voltage deintegration phase and MUST be used for ALL TC5xx applications having resolutions of 12 bits or more. If this phase is not used, the value of the Auto-Zero capacitor (C_{AZ}) must be about 2 to 3 times the value of the integration capacitor (C_{INT}) to reduce the effects of charge-sharing. The Integrator Output Zero phase should be programmed to operate until the Output of the Comparator returns "HIGH". The overall Timing System is shown in Figure 8.

ANALOG SECTION

Differential Inputs (V_{IN}⁺, V_{IN}⁻)

The TC5xx operates with differential voltages within the input amplifier common-mode range. The amplifier common-mode range extends from 1.5V below positive supply to 1.5V above negative supply. Within this common-mode

voltage range, common-mode rejection is typically 80dB. Full accuracy is maintained, however, when the inputs are no less than 1.5V from either supply.

The integrator output also follows the common-mode voltage. The integrator output must not be allowed to saturate. A worst-case condition exists, for example, when a large, positive common-mode voltage with a near full-scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications, the integrator swing can be reduced. The integrator output can swing within 0.9V of either supply without loss of linearity.

Analog Common

Analog common is used as V_{IN} return during system-zero and reference deintegrate. If V_{IN}⁻ is different from analog common, a common-mode voltage exists in the system. This signal is rejected by the excellent CMR of the converter. In most applications, V_{IN}⁻ will be set at a fixed known voltage (i.e., power supply common). A common-mode voltage will exist when V_{IN}⁻ is not connected to analog common.

Differential Reference (V_{REF}⁺, V_{REF}⁻)

The reference voltage can be anywhere within 1V of the power supply voltage of the converter. Roll-over error is caused by the reference capacitor losing or gaining charge due to stray capacitance on its nodes. The difference in reference for (+) or (-) input voltages will cause a roll-over error. This error can be minimized by using a large reference capacitor in comparison to the stray capacitance.

Phase Control Inputs (A, B)

The A, B unlatched logic inputs select the TC5xx operating phase. The A, B inputs are normally driven by a microprocessor I/O port or external logic.

Comparator Output

By monitoring the comparator output during the fixed signal integrate time, the input signal polarity can be determined by the microprocessor controlling the conversion. The comparator output is HIGH for positive signals and LOW for negative signals during the signal-integrate phase (see timing diagram).

During the reference deintegrate phase, the comparator output will make a HIGH-to-LOW transition as the integrator output ramp crosses zero. The transition is used to signal the processor that the conversion is complete.

The internal comparator delay is 2 μ sec, typically. Figure 5 shows the comparator output for large positive and negative signal inputs. For signal inputs at or near zero volts, however, the integrator swing is very small. If common-mode noise is present, the comparator can switch several times during the beginning of the signal-integrate period. To ensure that the polarity reading is correct, the comparator output should be read and stored at the end of the signal integrate phase.

The comparator output is undefined during the Auto-Zero Phase and is used to time the Integrator Output Zero phase. (See *Integrator Output Zero Phase of System Timing* section).

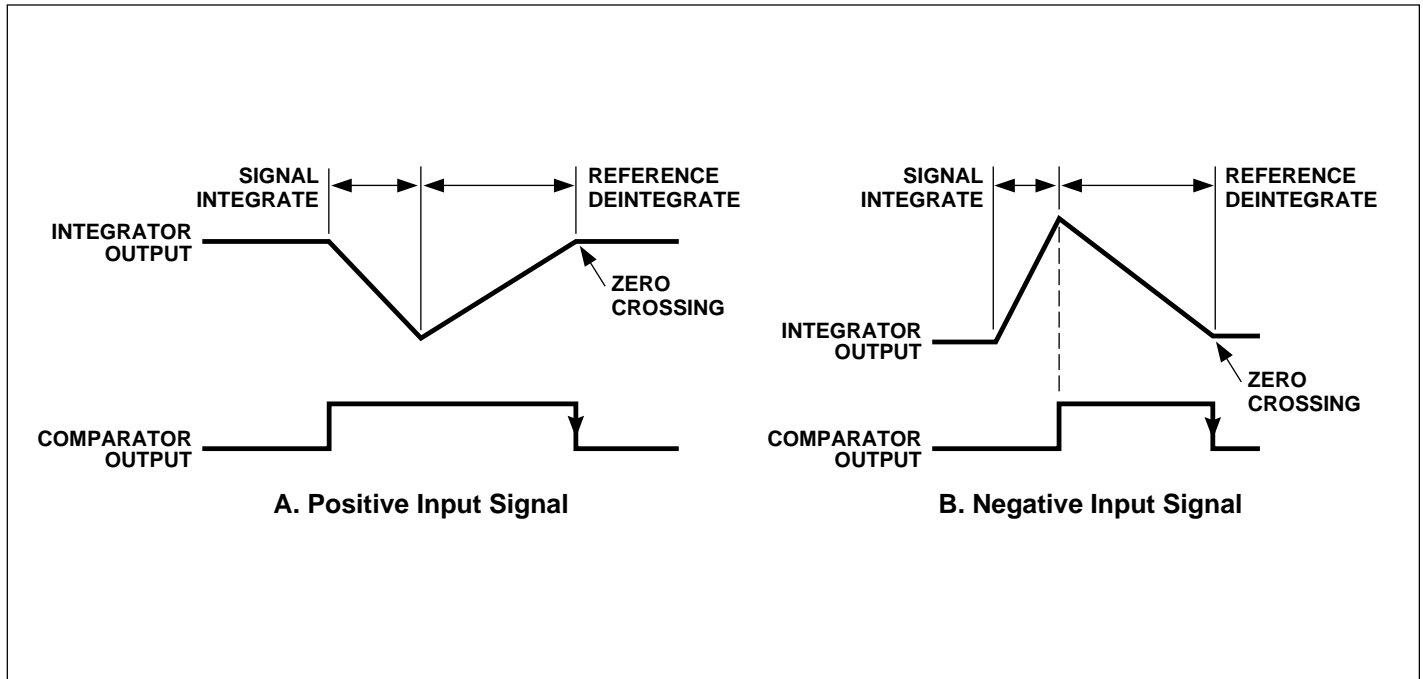


Figure 5. Comparator Output

TC500
TC500A
TC510
TC514

APPLICATIONS

Component Value Selection

The procedure outlined below allows the user to arrive at values for the following TC5xx design variables:

- (1) Integration Phase Timing
- (2) Integrator Timing Components (R_{INT} , C_{INT})
- (3) Auto Zero and Reference Capacitors
- (4) Voltage Reference

Select Integration Time

Integration time must be picked as a multiple of the period of the line frequency. For example, t_{INT} times of 33msec, 66msec and 132msec maximize 60Hz line rejection.

DINT and I_Z Phase Timing

The duration of the DINT phase is a function of the amount of voltage stored on the integrator during TINT, and the value of V_{REF} . The DINT phase must be initiated immediately following I_{NT} and terminated when an integrator output zero-crossing is detected. In general, the maximum number of counts chosen for DINT is twice that of INT (with V_{REF} chosen at $V_{IN(max)}/2$).

Calculate Integrating Resistor (R_{INT})

The desired full-scale input voltage and amplifier output current capability determine the value of R_{INT} . The buffer and integrator amplifiers each have a full-scale current of 20 μ A.

The value of R_{INT} is therefore directly calculated as follows:

$$R_{INT}(\text{in } M\Omega) = \frac{V_{IN MAX}}{20}$$

where: $V_{IN MAX}$ = Maximum input voltage (full count voltage)

R_{INT} = Integrating Resistor (in $M\Omega$)

For loop stability, R_{INT} should be $\geq 50k\Omega$.

Select Reference (C_{REF}) and Auto Zero (C_{AZ}) Capacitors

C_{REF} and C_{AZ} must be low leakage capacitors (such as polypropylene). The slower the conversion rate, the larger the value C_{REF} must be. Recommended capacitors for C_{REF} and C_{AZ} are shown in Table 1. Larger values for C_{AZ} and C_{REF} may also be used to limit roll-over errors.

Table 1. C_{REF} and C_{AZ} Selection

Conversions Per Second	Typical Value of C_{REF} , C_{AZ} (μ F)	Suggested * Part Number
>7	0.1	WIMA MK12 .1/63/20
2 to 7	0.22	WIMA MK12 .22/63/20
2 or less	0.47	WIMA MK12 .47/63/20

*WIMA Corp. listing on the last page of this data sheet.

Calculate Integrating Capacitor (C_{INT})

The integrating capacitor must be selected to maximize integrator output voltage swing. The integrator output voltage swing is defined as the absolute value of V_{DD} (or V_{SS}) less 0.9V (i.e., $|V_{DD} - 0.9V|$ or $|V_{SS} + 0.9V|$). Using the 20 μ A buffer maximum output current, the value of the integrating capacitor is calculated using the following equation.

$$C_{INT} = (\text{in } \mu\text{F}) = \frac{(t_{INT}) (20 \times 10^{-6})}{(V_S - 0.9)}$$

where: t_{INT} = Integration Period

V_S = Applied Supply Voltage

It is critical that the integrating capacitor has a very low dielectric absorption. Polypropylene capacitors are an example of one such chemistry. Polyester and Polyb carbonate capacitors may also be used in less critical applications. Table 2 summarizes recommended capacitors for C_{INT} .

Table 2. Recommend Capacitor for C_{INT}

Value	Suggested Part Number*
0.1	WIMA MK12 .1/63/20
0.22	WIMA MK12 .22/63/20
0.33	WIMA MK12 .33/63/20
0.47	WIMA MK12 .47/63/20

*WIMA Corp. listing on the last page of this data sheet.

Calculate V_{REF}

The reference deintegration voltage is calculated using:

$$V_{REF} (\text{in Volts}) = \frac{(V_S - 0.9) (C_{INT}) (R_{INT})}{2(t_{INT})}$$

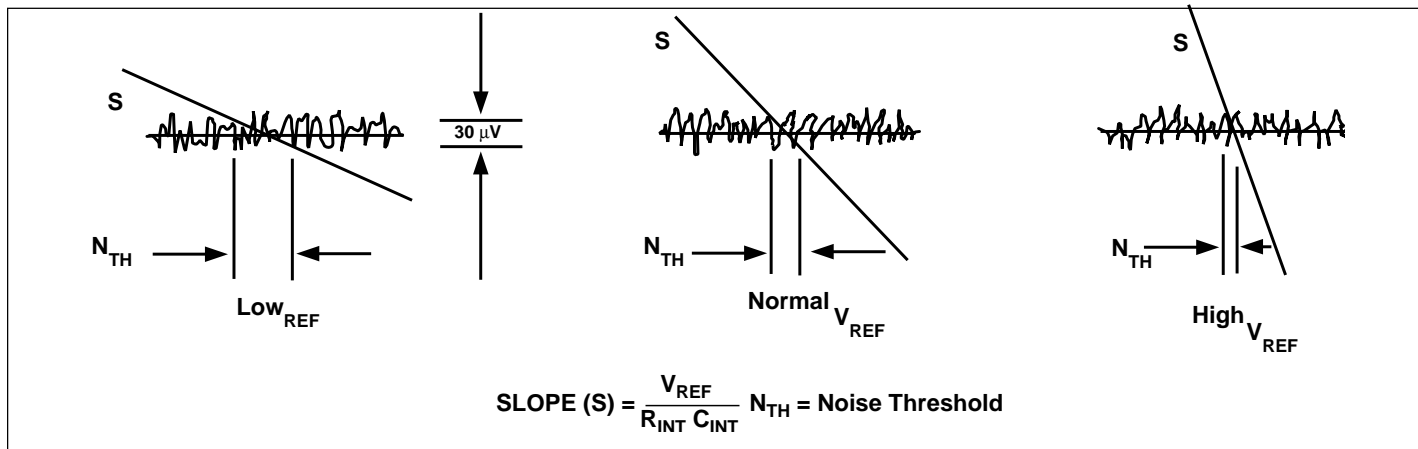


Figure 6. Noise

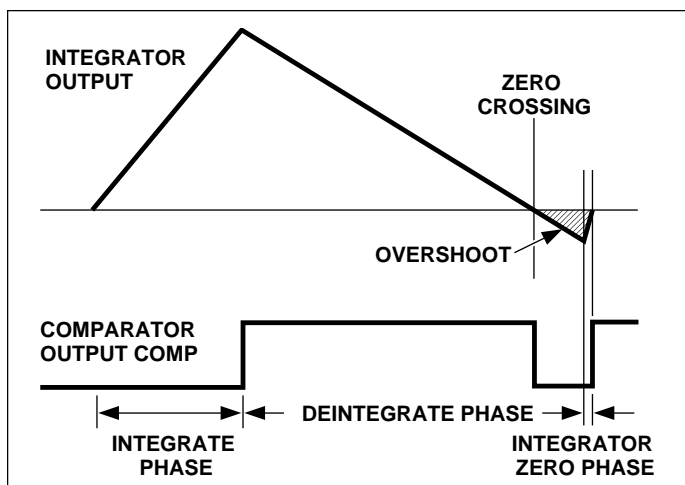


Figure 7. Overshoot

DESIGN CONSIDERATIONS

Noise

The threshold noise (NTH) is the algebraic sum of the integrator noise and the comparator noise. This value is typically 30μV. Figure 6 shows how the value of the reference voltage can affect the final count. Such errors can be reduced by increased integration times, in the same way that 50/60Hz noise is rejected. The signal-to-noise ratio is related to the integration time (t_{INT}) and the integration time constant (R_{INT}) (C_{INT}) as follows:

$$S/N \text{ (dB)} = 20 \text{ Log} \left(\frac{V_{IN}}{30 \times 10^{-6}} \cdot \frac{t_{INT}}{(R_{INT}) \cdot (C_{INT})} \right)$$

System Timing

To obtain maximum performance from the TC5xx, the overshoot at the end of the Deintegration phase must be minimized. Also, the Auto Zero phase must be terminated as soon as the comparator output returns high. (See timing diagram, Figure 8).

Figure 8 shows the overall timing for a typical system in which a TC5xx is interfaced to a microcontroller. The microcontroller drives the A, B inputs with I/O lines and monitors the comparator output, CMPTR, using an I/O line or dedicated timer-capture control pin. It may be necessary to monitor the state of the CMPTR output in addition to having it control a timer directly for the Reference Deintegration phase. (This is further explained below.)

The timing diagram in Figure 8 is not to scale as the timing in a real system depends on many system parameters and component value selections. There are four critical timing events (as shown in Figure 8): sampling the input polarity; capturing the deintegration time; minimizing overshoot and properly executing the Integrator Output Zero phase.

Auto-Zero Phase

The length of this phase is usually set to be equal to the Input Signal Integration time. This decision is virtually arbitrary since the magnitudes of the various system errors are not known. Setting the Auto-Zero time equal to the Input Integrate time should be more than adequate to null out system errors. The system may remain in this phase indefinitely, i.e., Auto-Zero is the appropriate idle state for a TC5xx device.

Input Signal Integrate Phase

The length of this phase is constant from one conversion to the next and depends on system parameters and component value selections. The calculation of t_{INT} is shown elsewhere in this data sheet. At some point near the end of this phase, the microcontroller should sample CMPTR to determine the input signal polarity. This value is, in effect, the Sign Bit for the overall conversion result. Optimally, CMPTR should be sampled just before this phase is terminated by changing AB from 10 to 11. The consideration here

TC500
TC500A
TC510
TC514

is that, during the initial stage of input integration when the integrator voltage is low, the comparator may be affected by noise and its output unreliable. Once integration is well underway, the comparator will be in a defined state.

Reference Deintegration

The length of this phase must be precisely measured from the transition of AB from 10 to 11 to the falling edge of CMPTR. The comparator delay contributes some error in timing this phase. The typical delay is specified to be 2μsec. This should be considered in the context of the length of a single count when determining overall system performance and possible single-count errors. Additionally, Overshoot will result in charge accumulating on the integrator after its output crosses zero. This charge must be nulled during the Integrator Output Zero phase.

Integrator Output Zero phase

The comparator delay and the controller's response latency may result in Overshoot causing charge buildup on the integrator at the end of a conversion. This charge must be removed or performance will degrade. The Integrator Output Zero phase should be activated (AB = 00) until CMPTR goes high. It is absolutely critical that this phase be terminated immediately so that Overshoot is not allowed to occur in the opposite direction. At this point, it can be assured that the integrator is near zero. Auto Zero should be entered (AB = 01) and the TC5xx held in this state until the next cycle is begun.

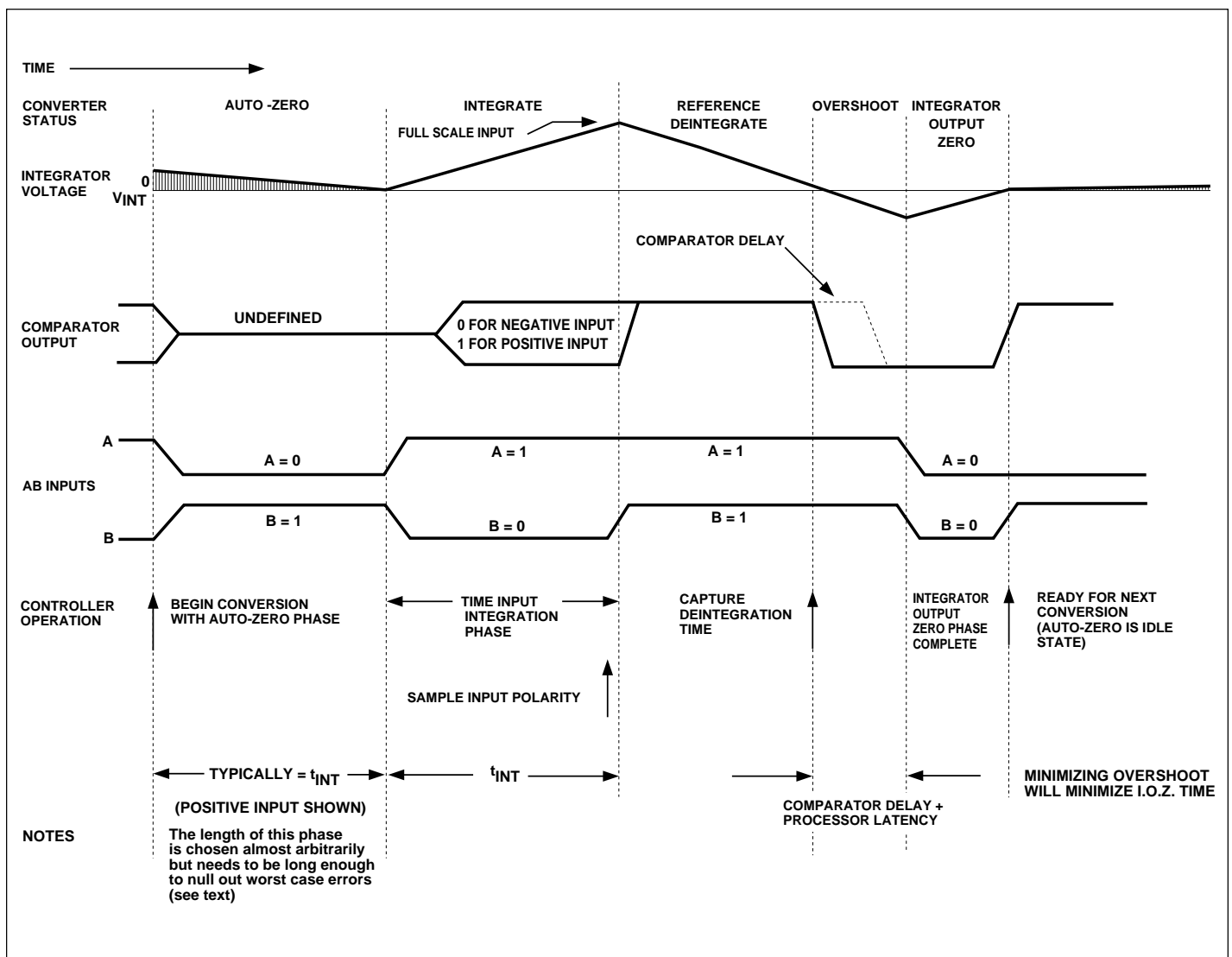


Figure 8. Typical Dual Slope A/D Converter System Timing

Design Example

Given: Required Resolution: 16 Bits (65,536 counts).
Maximum V_{IN} : $\pm 2V$
Power Supply Voltage: +5V
60Hz System

Step 1: Pick integration time (t_{INT}) as a multiple of the line frequency:

$$1/60\text{Hz} = 16.6\text{msec. Use } 4\times \text{ line frequency} = 66\text{msec}$$

Step 2: Calculate R_{INT}

$$R_{INT} \text{ (in } \text{M}\Omega) = V_{INMAX}/20 = 2/20 = \underline{100\text{k}\Omega}$$

Step 3: Calculate C_{INT} for maximum (4V) integrator output swing:

$$\begin{aligned} C_{INT} \text{ (in } \mu\text{F}) &= (t_{INT}) (20 \times 10^{-6}) / (V_S - 0.9) \\ &= (.066) (20 \times 10^{-6}) / (4.1) \\ &= .32\mu\text{F (use closest value: } \underline{0.33\mu\text{F}}) \end{aligned}$$

NOTE: Microchip recommended capacitor:
WIMA p/n: MK12 .33/63/10

Step 4: Choose C_{REF} and C_{AZ} based on conversion rate:

$$\begin{aligned} \text{Conversions/sec} &= 1/(t_{AZ} + t_{INT} + 2 t_{INT} + 2\text{msec}) \\ &= 1/(66\text{msec} + 66\text{msec} + 132\text{msec} + 2\text{msec}) \\ &= 3.7 \text{ conversions/sec} \end{aligned}$$

From which $C_{AZ} = C_{REF} = \underline{0.22\mu\text{F}}$ (see Table 1)

NOTE: Microchip recommended capacitor:
WIMA p/n: MK12 .22/63/10

Step 5: Calculate V_{REF}

$$\begin{aligned} V_{REF} \text{ (in Volts)} &= \frac{(V_S - 0.9) (C_{INT}) (R_{INT})}{2(t_{INT})} \\ &= (4.1) (0.33 \times 10^{-6}) (10^5) / 2(.066) \\ &= \underline{1.025V} \end{aligned}$$

USING THE TC510/514

Negative Supply Voltage Converter (TC510, TC514)

A capacitive charge pump is employed to invert the voltage on V_{DD} for negative bias within the TC510/514. This voltage is also available on the V_{OUT}^- pin to provide negative bias elsewhere in the system. Two external capacitors are required to perform the conversion.

Timing is generated by an internal state machine driven from an on-board oscillator. During the first phase, capacitor C_F is switched across the power supply and charged to V_S^+ . This charge is transferred to capacitor C_{OUT}^- during the second phase. The oscillator normally runs at 100kHz to ensure minimum output ripple. This frequency can be reduced by placing a capacitor from OSC to V_{DD} . The relationship between the capacitor value is shown in the typical characteristics curves at the end of this data sheet.

Analog Input Multiplexer (TC514)

The TC514 is equipped with a four input differential analog multiplexer. Input channels are selected using select inputs (A1, A0). These are high-true control signals (i.e., channel 0 is selected when (A1, A0) = 00).

EVALUATION KIT (TC500EV)

The TC500EV consists of a pre-assembled, 4 inch by 6 inch printed circuit board that connects to the serial port of any PC or dumb terminal. Design software is also included. TC500EV helps reduce design time and optimize converter performance. Please contact your local Microchip representative for more information.

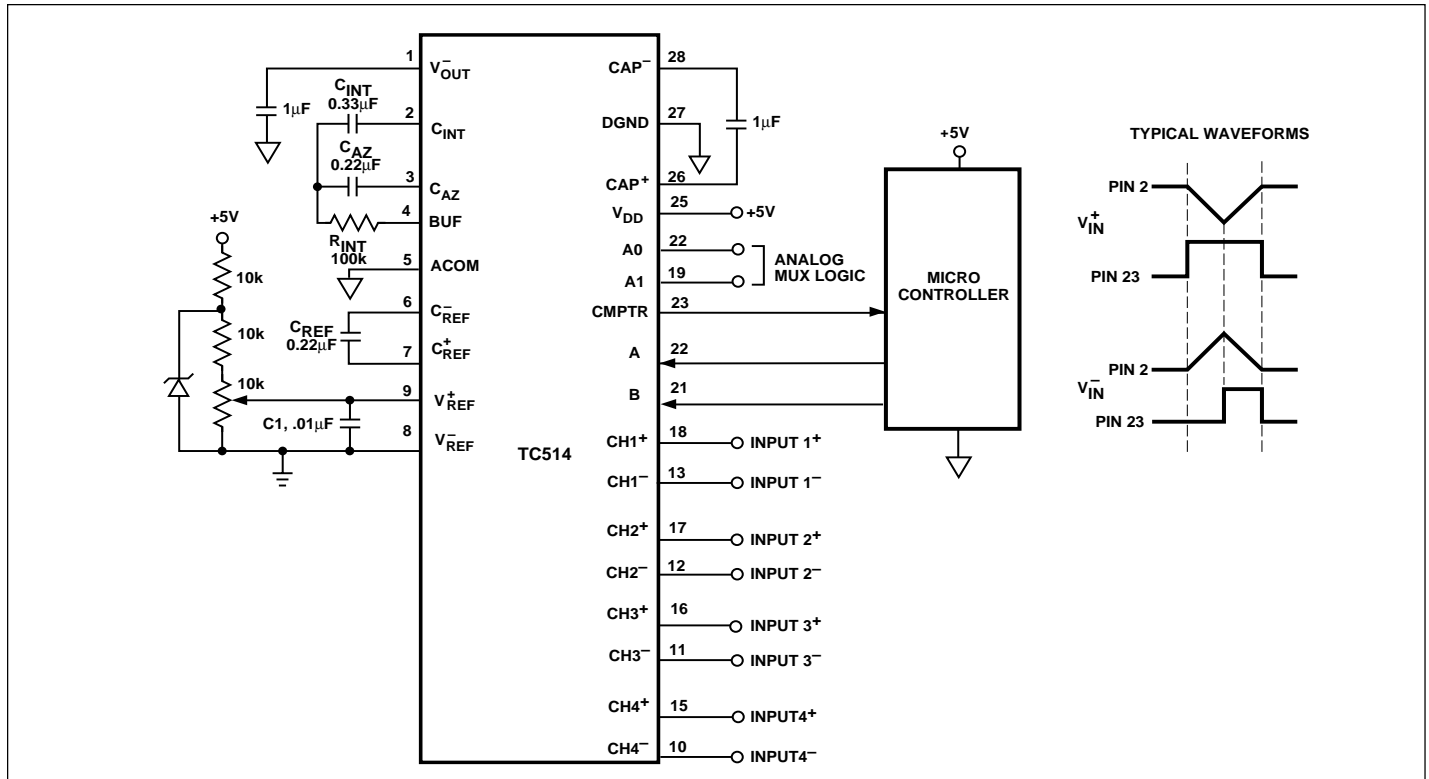


Figure 10. TC514 Design Example (See "Design Example")

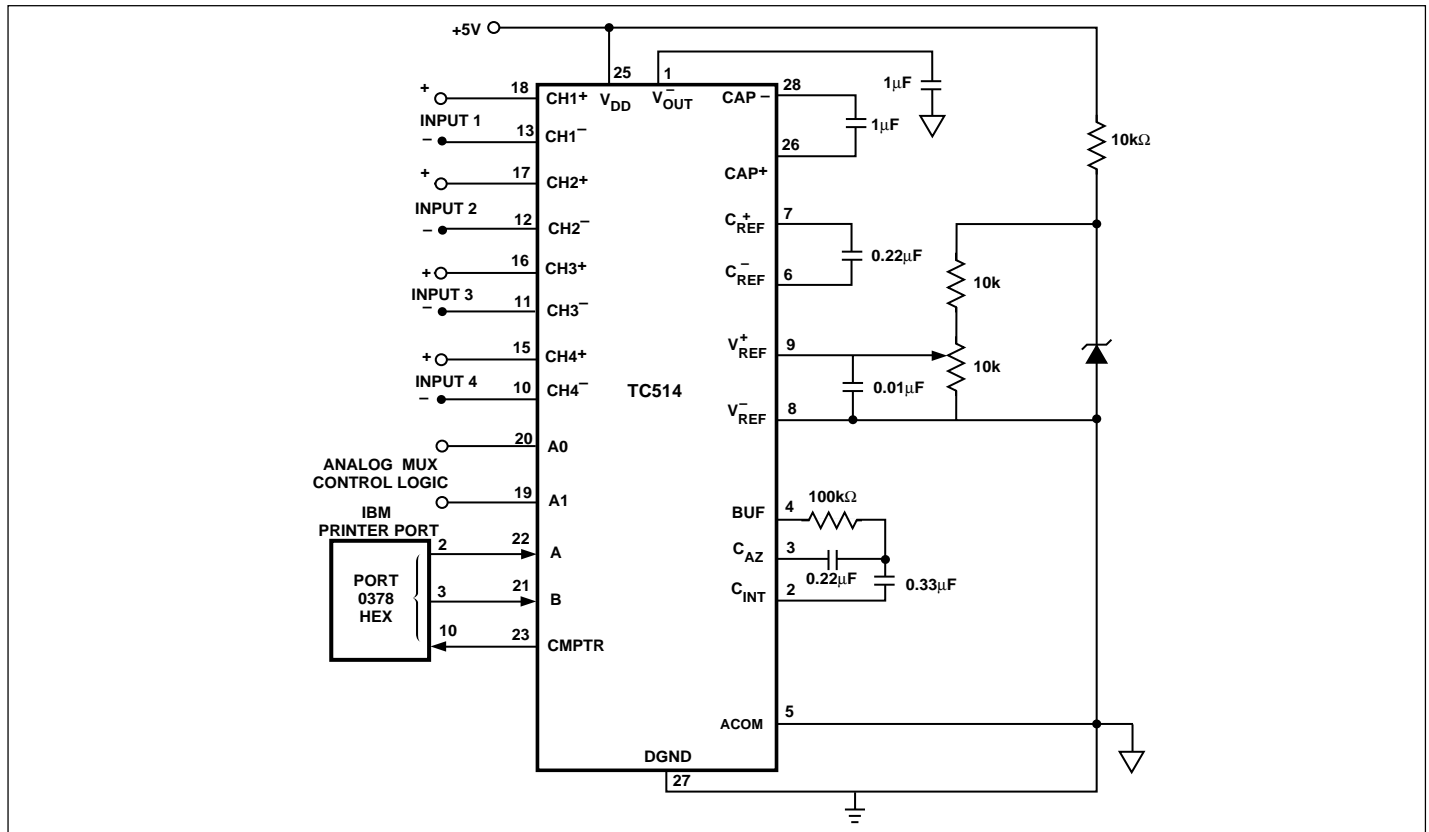
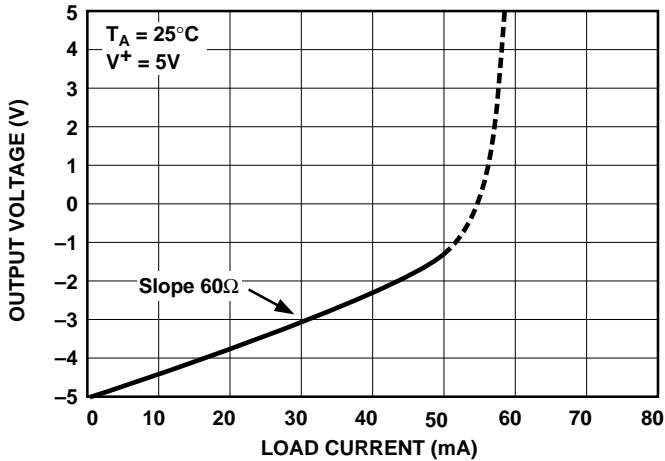


Figure 11. TC514 to IBM Compatible Printer Port

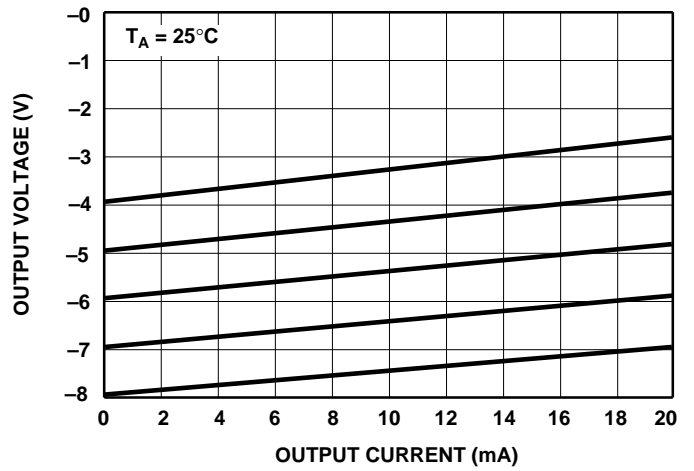
TC500
TC500A
TC510
TC514

TYPICAL PERFORMANCE CHARACTERISTICS OF INTERNAL DC-TO-DC CONVERTER

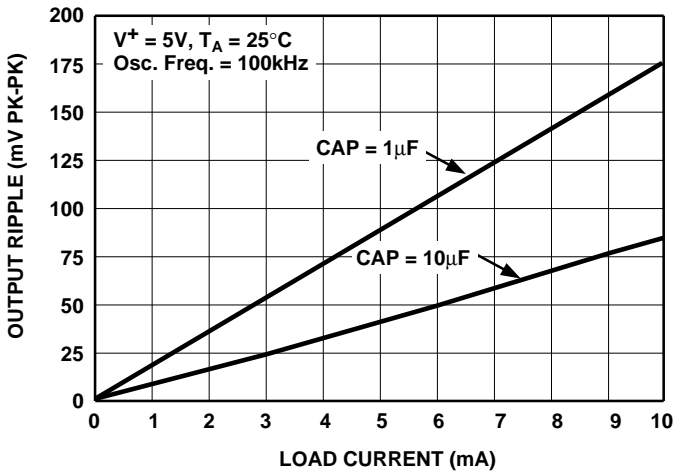
Output Voltage vs Load Current



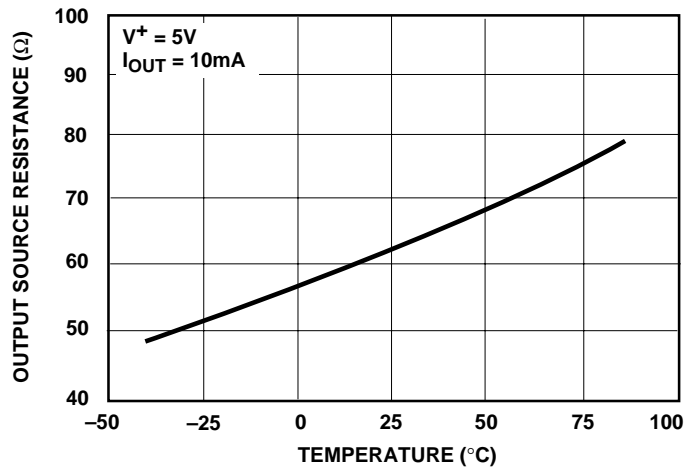
Output Voltage vs. Output Current



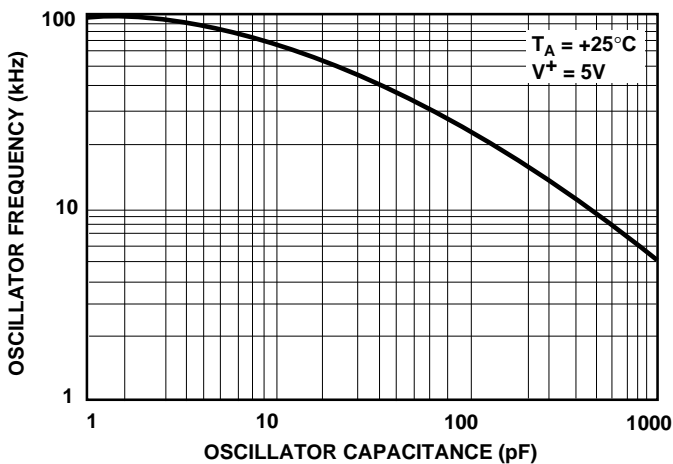
Output Ripple vs. Load Current



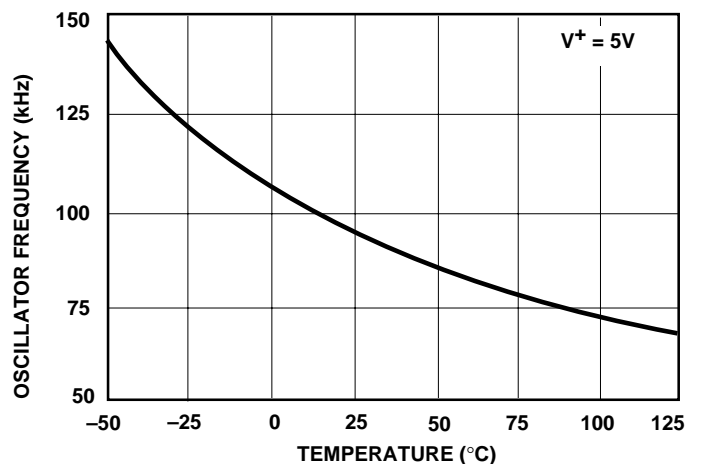
Output Source Resistance vs. Temperature



Oscillator Frequency vs. Capacitance

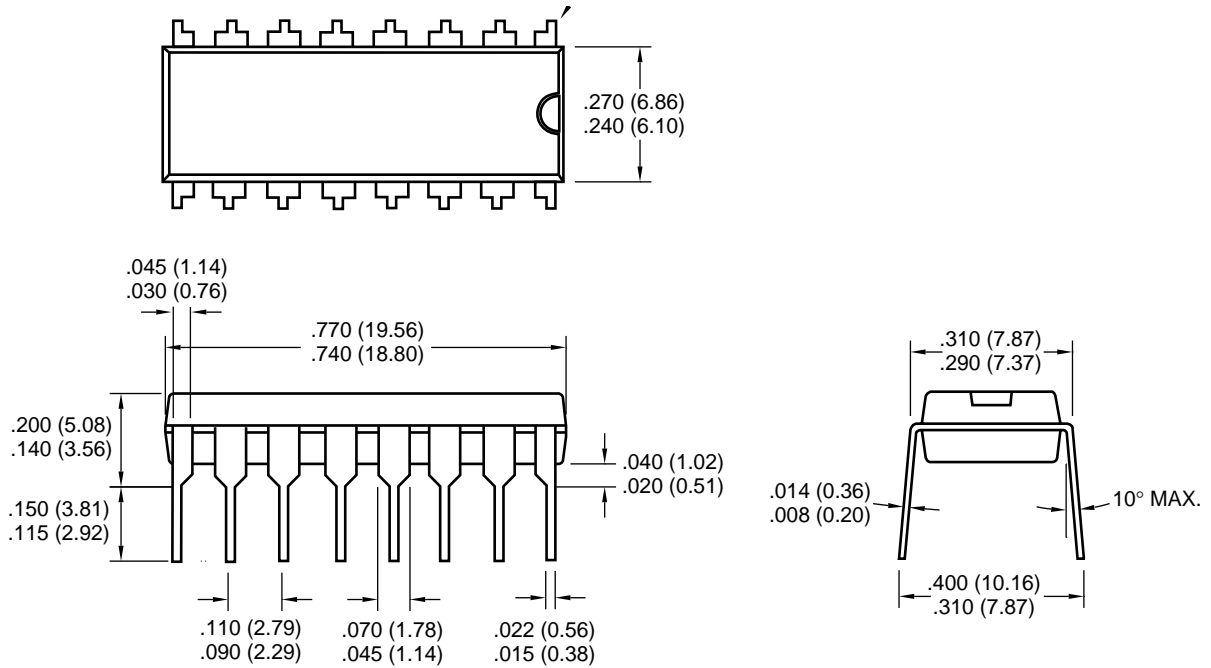


Oscillator Frequency vs. Temperature

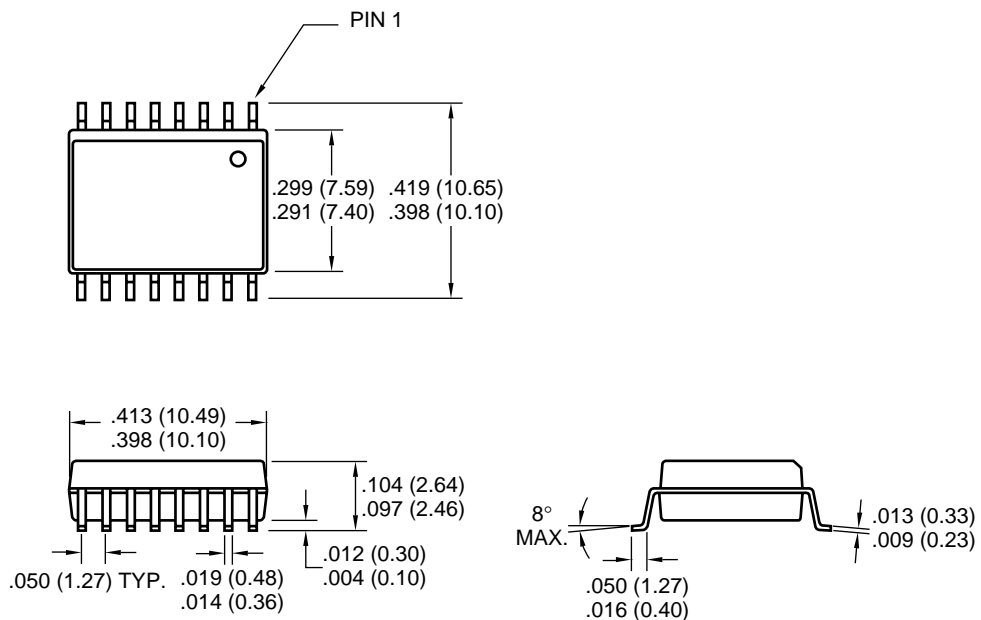


PACKAGE DIMENSIONS

16-Pin Plastic DIP (Narrow)



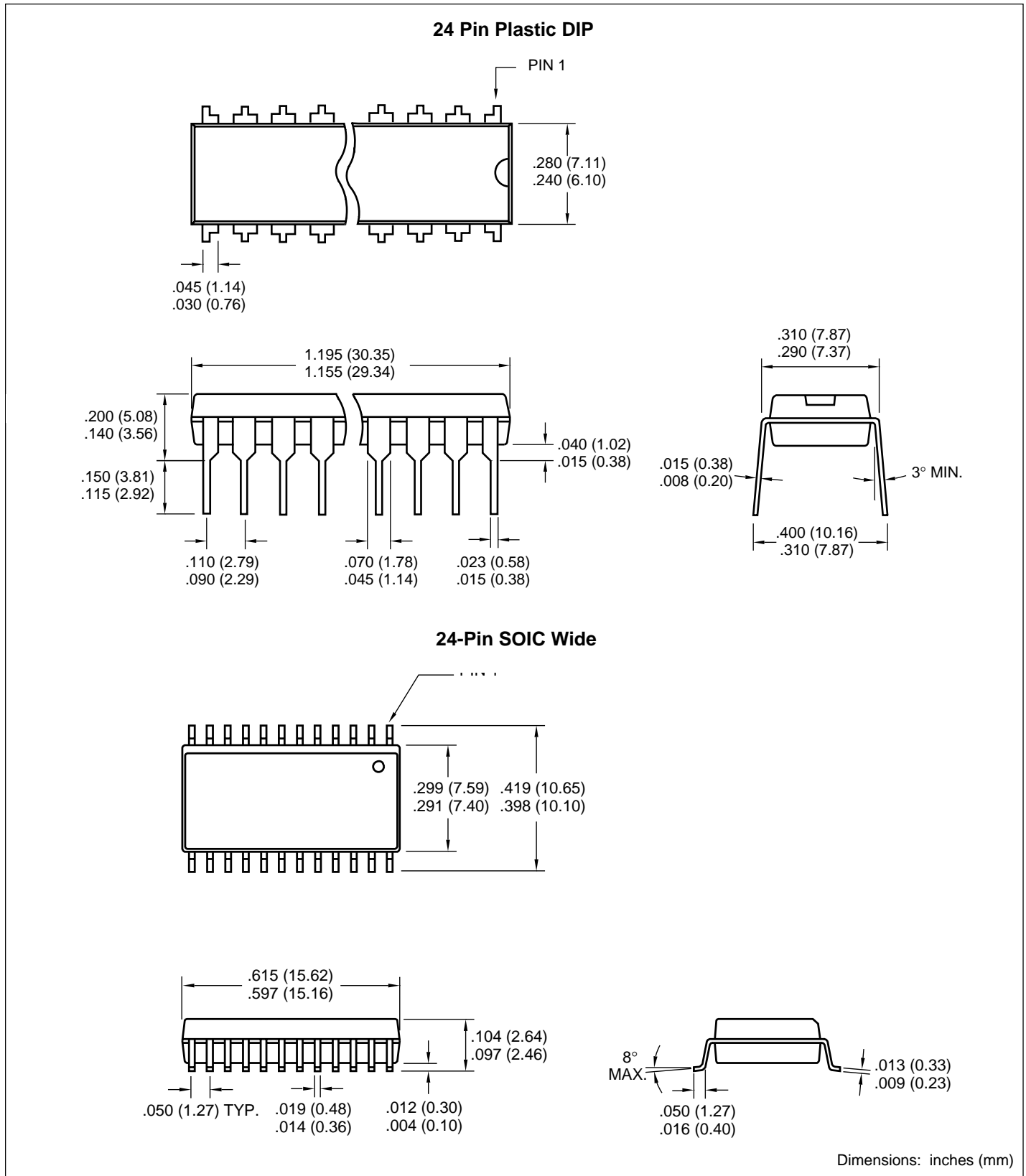
16-Pin SOIC



Dimensions: inches (mm)

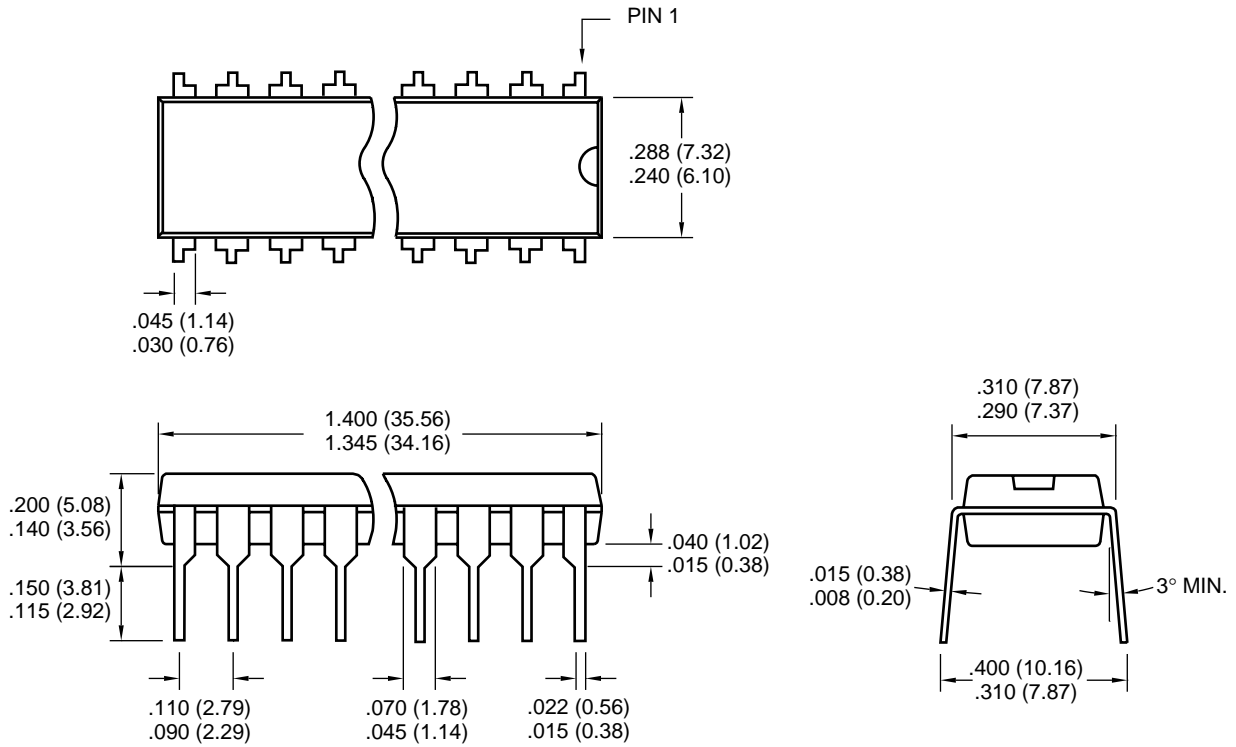
TC500
TC500A
TC510
TC514

PACKAGE DIMENSIONS (Cont.)

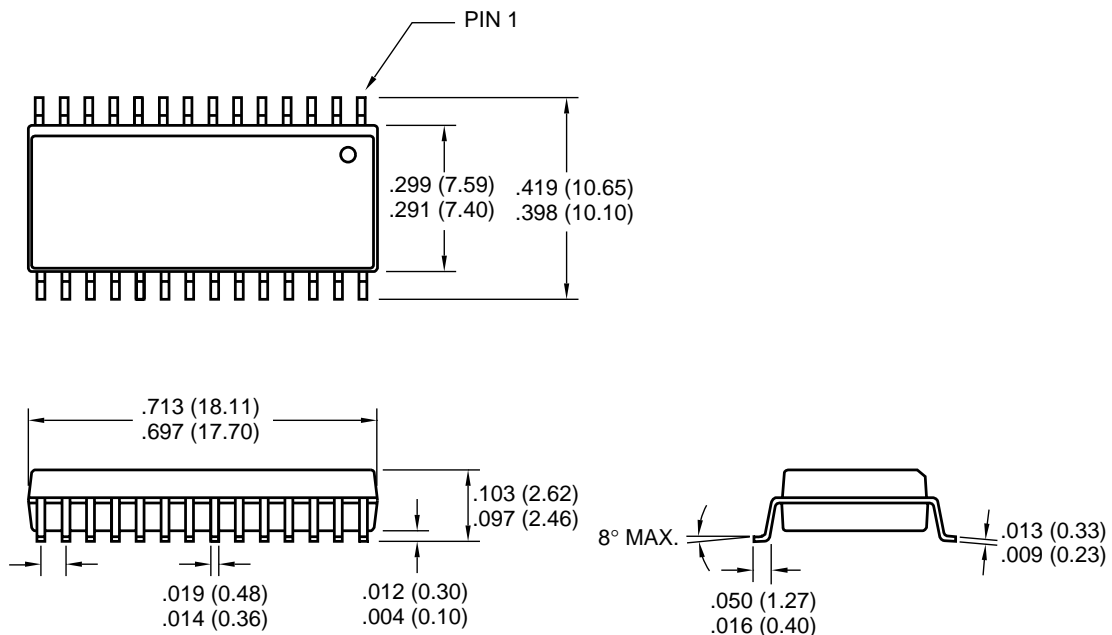


PACKAGE DIMENSIONS (Cont.)

28-Pin Plastic DIP (300 Mil.)



28-Pin SOIC



Dimensions: inches (mm)

TC500
TC500A
TC510
TC514

WIMA Corporation Capacitor Representatives (Tables 1 and 2 in Applications Section)

Australia:

ADILAM ELECTRONICS (PTY.) LTD.
 P.O. Box 664
 3 Nicole Close
 Bayswater 3153
 Tel.: 3-761-4466
 Fax: 3-761-4161

Canada:

R-THETA INC.
 130 Matheson Blvd. East, Unit 2
 Mississauga, Ont. L4Z1Y6
 Tel.: 905-890-0221
 Fax: 905-890-1628

Hong Kong:

REALTRONICS CO. LTD.
 E-3, Hung-On Building
 2, King's Road
 Tel.: 25-70-1151
 Fax: 28-06-8474

India:

SUSAN AGENCIES
 P.O. Box 2138
 Srirampuram P.O.
 Bangalore-560 021
 Tel.: 080-332-0662
 Fax: 080-332-4338

Israel:

M.G.R. TECHNOLOGY
 P.O. Box 2229
 Rehavot 76121
 Tel.: 972-841-1719
 Fax: 972-841-4178

Japan:

UNIDUX INC.
 5-1-21, Kyonan-Cho
 Musashino-Shi
 Tokyo 180
 Tel.: 04-2232-4111
 Fax: 04-2232-0331

Malaysia:

MA ELECTRONICS (M) SDN BHD
 346-B Jalan Jelutong
 11600 Penang
 Tel.: 604-281-4518
 Fax: 604-281-4515

Singapore:

MICROTRONICS ASSOC. (PTE.) LTD.
 8, Lorong Bakar Batu
 03-01, Kolam Ayer Ind. Park
 Singapore 1334
 Tel.: 65-748-1835
 Tlx: 34 929
 Fax: 65-743-3065

South Africa:

KOPP ELECTRONICS LIMITED
 P.O. Box 3853
 2128 Rivonia
 Tel.: 011-444-2333
 Fax: 011-444-1706

South Korea:

YONG JUN ELECTRONIC CO.
 #201, Sungwook Bldg.
 1460-16, Seocho-Dong
 Seocho-Ku
 Seoul, Korea
 Tel.: 25-231-8002
 Fax: 25-231-803

Taiwan, R.O.C.:

SOLOMON TECHNOLOGY CORP.
 7th Floor No. 2
 Lane 47, Sec. 3
 Nan Kang Road
 Taipei
 Tel.: 886-2788-8989
 Fax: 886-288-8275

Thailand:

MICROTRONICS THAI LTD.
 50/68 T.T. Court
 Cheng Wattana Road
 Amphur Pak-Kreed
 Nonthaburi 11120
 Tel.: 66-2584-5807, Ext. 102
 Fax: 66-2583-3775

USA:

THE INTER-TECHNICAL GROUP, INC.
WIMA DIVISION
 175 Clearbrook Road
 P.O. Box 535
 Elmsford, NY 10523-0535
 Tel.: 914-347-2474
 Fax: 914-347-7230

TAW ELECTRONICS, INC.

4215, W. Burbank, Blvd.
 Burbank, CA, 91505
 Tel.: 818-846-3911
 Fax: 818-846-1194

Venezuela:

MAGNETICA, S.A.
 Apartado 78117
 Caracas 1074 A
 Tel.: 58-2241-7509
 Fax: 58-2241-5542



WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: <http://www.microchip.com>

Rocky Mountain

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966 Fax: 480-792-7456

Atlanta

500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Austin

Analog Product Sales
8303 MoPac Expressway North
Suite A-201
Austin, TX 78759
Tel: 512-345-2030 Fax: 512-345-6085

Boston

2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848 Fax: 978-692-3821

Boston

Analog Product Sales
Unit A-8-1 Millbrook Tarry Condominium
97 Lowell Road
Concord, MA 01742
Tel: 978-371-6400 Fax: 978-371-0050

Chicago

333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas

4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423 Fax: 972-818-2924

Dayton

Two Prestige Place, Suite 130
Miamisburg, OH 45342
Tel: 937-291-1654 Fax: 937-291-9175

Detroit

Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Los Angeles

18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

Mountain View

Analog Product Sales
1300 Terra Bella Avenue
Mountain View, CA 94043-1836
Tel: 650-968-9241 Fax: 650-967-1590

New York

150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose

Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto

6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

China - Beijing

Microchip Technology Beijing Office
Unit 915
New China Hong Kong Manhattan Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Shanghai

Microchip Technology Shanghai Office
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

Hong Kong

Microchip Asia Pacific
RM 2101, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India

Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, OIShaughnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan

Microchip Technology Intl. Inc.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471-6166 Fax: 81-45-471-6122

Korea

Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea
Tel: 82-2-554-7200 Fax: 82-2-558-5934

ASIA/PACIFIC (continued)

Singapore

Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan

Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Australia

Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

Denmark

Microchip Technology Denmark ApS
Regus Business Centre
Lautrup høj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France

Arizona Microchip Technology SARL
Parc diActivite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - 1er Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany

Arizona Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Germany

Analog Product Sales
Lochamer Strasse 13
D-82152 Martinsried, Germany
Tel: 49-89-895650-0 Fax: 49-89-895650-22

Italy

Arizona Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom

Arizona Microchip Technology Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

All rights reserved. © 2001 Microchip Technology Incorporated. Printed in the USA. 1/01  Printed on recycled paper.

01/09/01

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, except as maybe explicitly expressed herein, under any intellectual property rights. The Microchip logo and name are registered trademarks of Microchip Technology Inc. in the U.S.A. and other countries. All rights reserved. All other trademarks mentioned herein are the property of their respective companies.