



# PRESETTABLE BCD/DECADE UP/DOWN COUNTERS

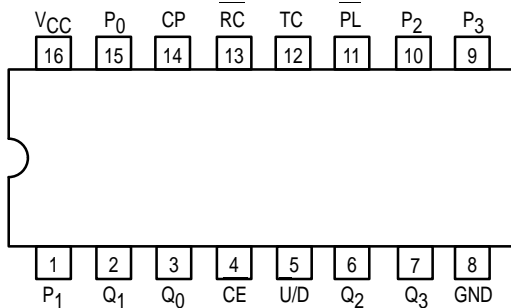
## PRESETTABLE 4-BIT BINARY UP/DOWN COUNTERS

The SN54/74LS190 is a synchronous UP/DOWN BCD Decade (8421) Counter and the SN54/74LS191 is a synchronous UP/DOWN Modulo-16 Binary Counter. State changes of the counters are synchronous with the LOW-to-HIGH transition of the Clock Pulse input.

An asynchronous Parallel Load (PL) input overrides counting and loads the data present on the  $P_n$  inputs into the flip-flops, which makes it possible to use the circuits as programmable counters. A Count Enable (CE) input serves as the carry/borrow input in multi-stage counters. An Up/Down Count Control (U/D) input determines whether a circuit counts up or down. A Terminal Count (TC) output and a Ripple Clock (RC) output provide overflow/underflow indication and make possible a variety of methods for generating carry/borrow signals in multistage counter applications.

- Low Power . . . 90 mW Typical Dissipation
- High Speed . . . 25 MHz Typical Count Frequency
- Synchronous Counting
- Asynchronous Parallel Load
- Individual Preset Inputs
- Count Enable and Up/Down Control Inputs
- Cascadable
- Input Clamp Diodes Limit High Speed Termination Effects

### CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

CE	Count Enable (Active LOW) Input
CP	Clock Pulse (Active HIGH going edge) Input
U/D	Up/Down Count Control Input
PL	Parallel Load Control (Active LOW) Input
$P_n$	Parallel Data Inputs
$Q_n$	Flip-Flop Outputs (Note b)
RC	Ripple Clock Output (Note b)
TC	Terminal Count Output (Note b)

### NOTES:

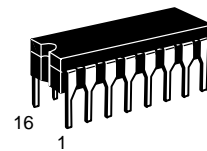
- a. 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.  
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

### LOADING (Note a)

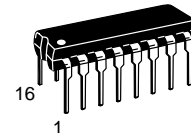
	HIGH	LOW
CE	1.5 U.L.	0.7 U.L.
CP	0.5 U.L.	0.25 U.L.
U/D	0.5 U.L.	0.25 U.L.
PL	0.5 U.L.	0.25 U.L.
$P_n$	0.5 U.L.	0.25 U.L.
$Q_n$	10 U.L.	5 (2.5) U.L.
RC	10 U.L.	5 (2.5) U.L.
TC	10 U.L.	5 (2.5) U.L.

## SN54/74LS190 SN54/74LS191

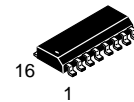
PRESETTABLE BCD/DECADE  
UP/DOWN COUNTERS  
PRESETTABLE 4-BIT BINARY  
UP/DOWN COUNTERS  
LOW POWER SCHOTTKY



J SUFFIX  
CERAMIC  
CASE 620-09



N SUFFIX  
PLASTIC  
CASE 648-08

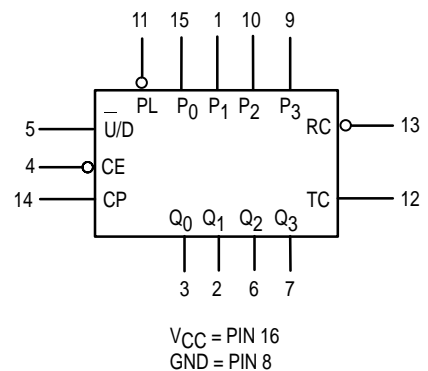


D SUFFIX  
SOIC  
CASE 751B-03

### ORDERING INFORMATION

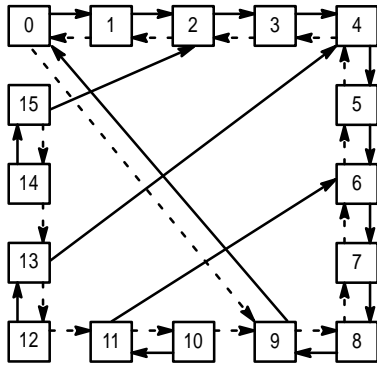
SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

### LOGIC SYMBOL



# SN54/74LS190 • SN54/74LS191

## STATE DIAGRAMS

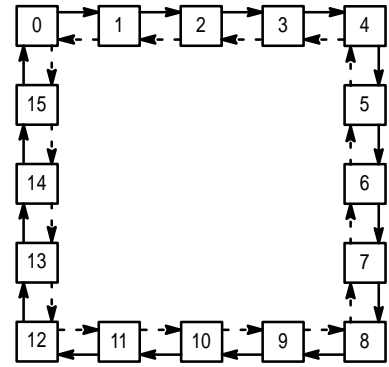


LS190

**LS190**  
 UP:  $TC = Q_0 \cdot Q_3 \cdot \overline{(U/D)}$   
 DOWN:  $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (U/D)$

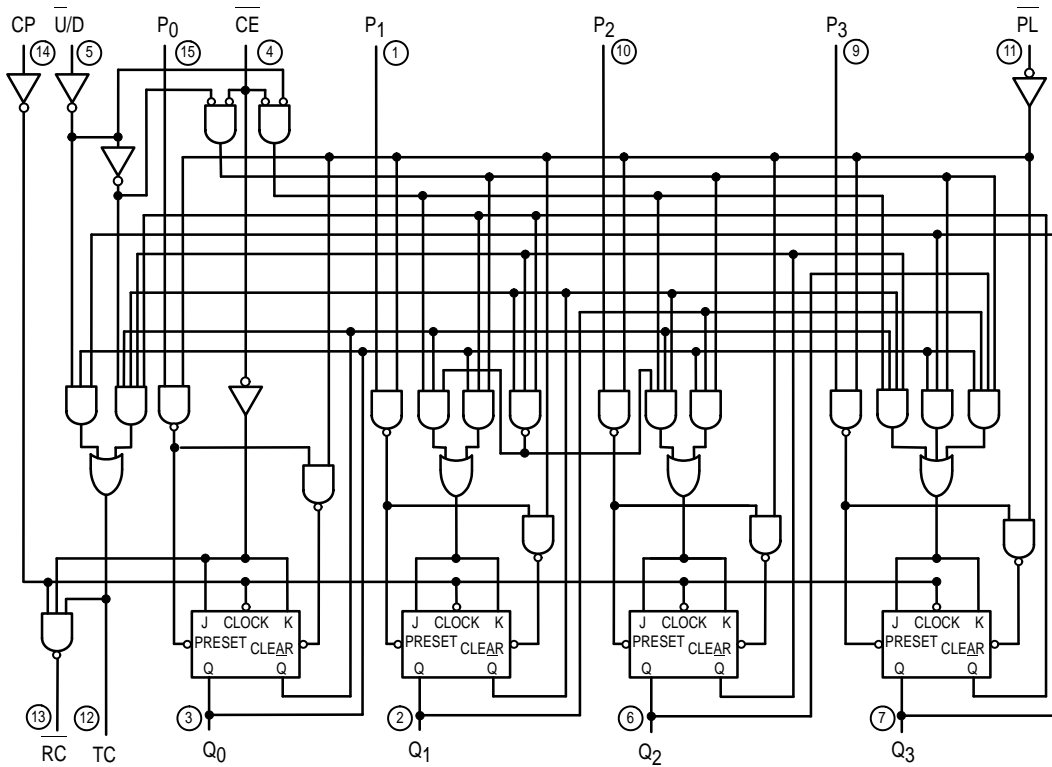
**LS191**  
 UP:  $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{(U/D)}$   
 DOWN:  $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (U/D)$

COUNT UP ———  
 COUNT DOWN - - - - -



LS191

## LOGIC DIAGRAMS

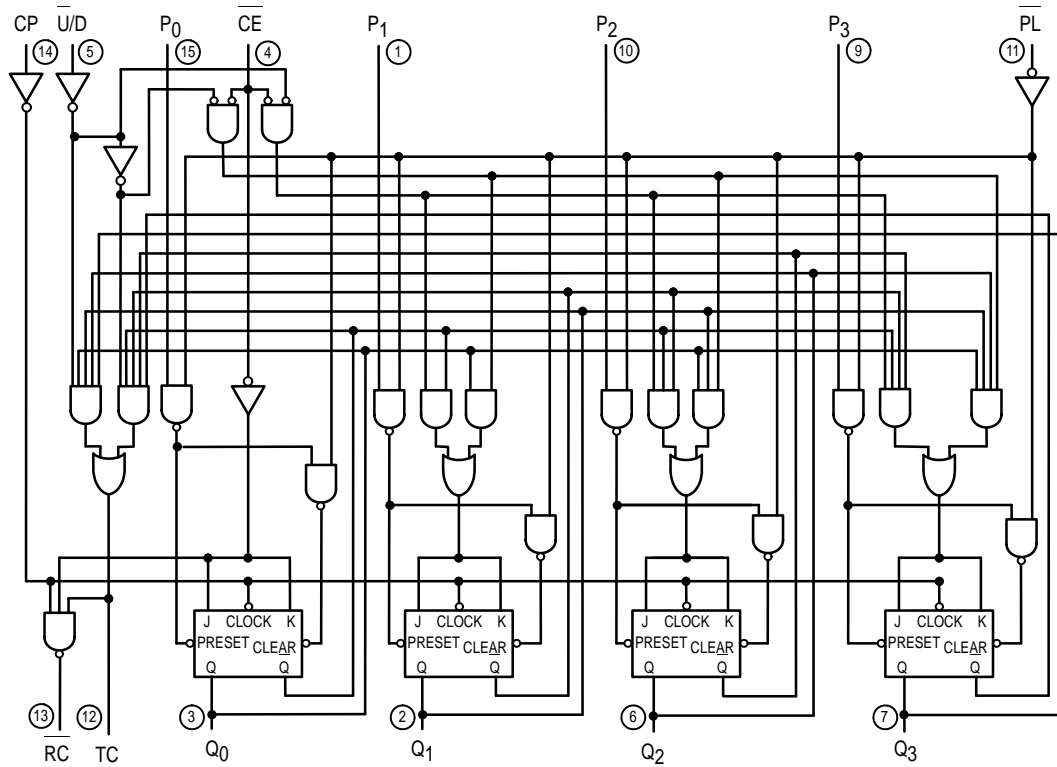


DECADE COUNTER  
 LS190

$V_{CC}$  = PIN 16  
 GND = PIN 8  
 ○ = PIN NUMBERS

# SN54/74LS190 • SN54/74LS191

## LOGIC DIAGRAMS (continued)



$V_{CC}$  = PIN 16  
 GND = PIN 8  
 ○ = PIN NUMBERS

**BINARY COUNTER  
 LS191**

# SN54/74LS190 • SN54/74LS191

## FUNCTIONAL DESCRIPTION

The LS190 is a synchronous Up/Down BCD Decade Counter and the LS191 is a synchronous Up/Down 4-Bit Binary Counter. The operating modes of the LS190 decade counter and the LS191 binary counter are identical, with the only difference being the count sequences as noted in the state diagrams. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load (PL) input is LOW, information present on the Parallel Data inputs (P<sub>0</sub>–P<sub>3</sub>) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the CE input inhibits counting. When CE is LOW, internal state change are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the U/D input signal, as indicated in the Mode Select Table. When counting is to be enabled, the CE signal can be made LOW when the clock is in either state. However, when counting is to be inhibited, the LOW-to-HIGH CE transition must occur only while the clock is HIGH. Similarly, the U/D signal should only be changed when either CE or the clock is HIGH.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches maximum (9 for the LS190, 15 for the LS191) in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until U/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.



The TC signal is also used internally to enable the Ripple

Clock (RC) output. The RC output is normally HIGH. When CE is LOW and TC is HIGH, the RC output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multi-stage counters, as indicated in Figures a and b. In Figure a, each RC output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on CE inhibits the RC output pulse, as indicated in the RC Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.



A method of causing state changes to occur simultaneously in all stages is shown in Figure b. All clock inputs are driven in parallel and the RC outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stop before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the RC output of any package goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure c avoids ripple delays and their associated restrictions. The CE input signal for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figures a and b doesn't apply, because the TC output of a given stage is not affected by its own CE.



MODE SELECT TABLE

INPUTS				MODE
PL	CE	U/D	CP	
H	L	L		Count Up
H	L	H		Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

RC TRUTH TABLE

INPUTS			RC OUTPUT
CE	TC*	CP	
L	H		
H	X	X	H
X	L	X	H

\* TC is generated internally

- L = LOW Voltage Level
- H = HIGH Voltage Level
- X = Don't Care
-  = LOW-to-HIGH Clock Transition
-  = LOW Pulse

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## GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I <sub>OH</sub>	Output Current — High	54, 74			-0.4	mA
I <sub>OL</sub>	Output Current — Low	54 74			4.0 8.0	mA

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V <sub>IL</sub>	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA	
V <sub>OH</sub>	Output HIGH Voltage	54	2.5	3.5	V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table	
		74	2.7	3.5	V		
V <sub>OL</sub>	Output LOW Voltage	54, 74		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
		74		0.35	0.5	V	
I <sub>IH</sub>	Input HIGH Current Other Inputs CE			20 60	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V	
	Other Inputs CE			0.1 0.3	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V	
I <sub>IL</sub>	Input LOW Current Other Inputs CE			-0.4 -1.2	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V	
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX	
I <sub>CC</sub>	Power Supply Current			35	mA	V <sub>CC</sub> = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

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## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f <sub>MAX</sub>	Maximum Clock Frequency	20	25		MHz	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, PL to Output Q		22 33	33 50	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Data to Output Q		20 27	32 40	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Clock to $\overline{\text{RC}}$		13 16	20 24	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Clock to Output Q		16 24	24 36	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Clock to TC		28 37	42 52	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	$\overline{\text{U/D}}$ to $\overline{\text{RC}}$		30 30	45 45	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	$\overline{\text{U/D}}$ to TC		21 22	33 33	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	$\overline{\text{CE}}$ to $\overline{\text{RC}}$		21 22	33 33	ns	

## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>W</sub>	CP Pulse Width	25			ns	V <sub>CC</sub> = 5.0 V
t <sub>W</sub>	PL Pulse Width	35			ns	
t <sub>S</sub>	Data Setup Time	20			ns	
t <sub>H</sub>	Data Hold Time	5.0			ns	
t <sub>rec</sub>	Recovery Time	40			ns	

### DEFINITIONS OF TERMS

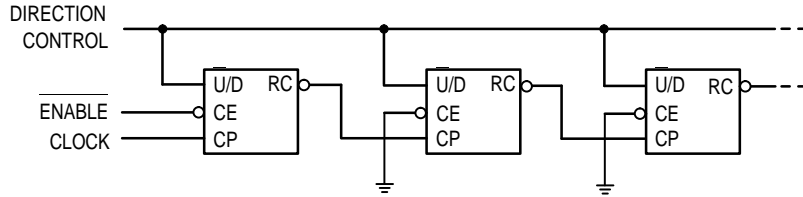
SETUP TIME (t<sub>S</sub>) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t<sub>H</sub>) is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recogni-

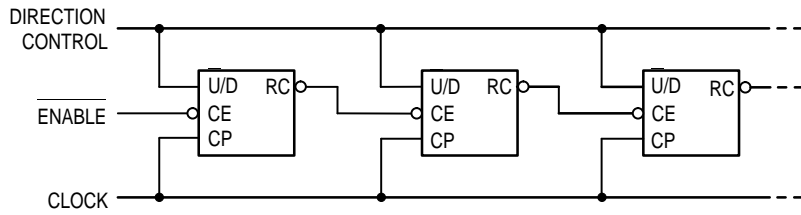
tion. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t<sub>rec</sub>) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.

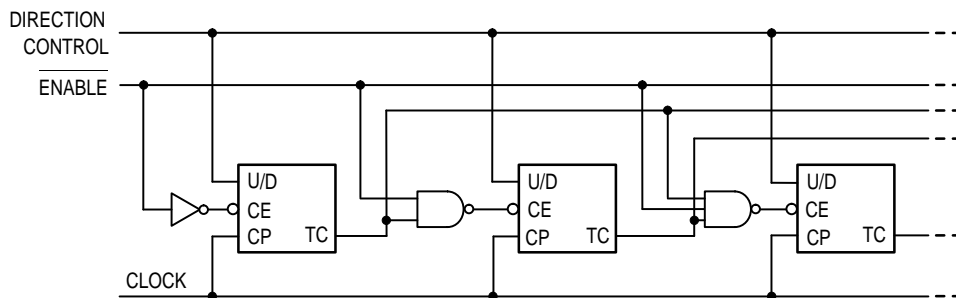
## SN54/74LS190 • SN54/74LS191



**Figure a. n-Stage Counter Using Ripple Clock**



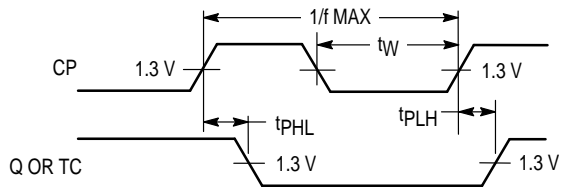
**Figure b. Synchronous n-Stage Counter Using Ripple Carry/Borrow**



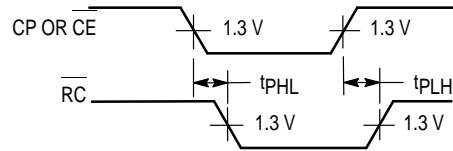
**Figure c. Synchronous n-Stage Counter with Parallel Gated Carry/Borrow**

# SN54/74LS190 • SN54/74LS191

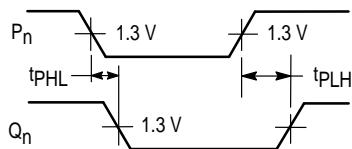
## AC WAVEFORMS



**Figure 1**

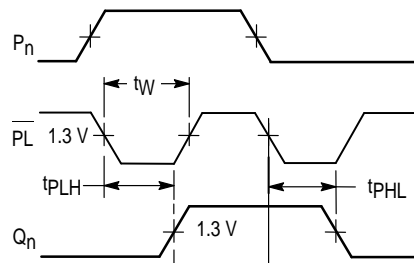


**Figure 2**

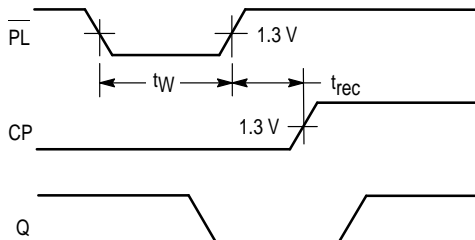


NOTE: PL = LOW

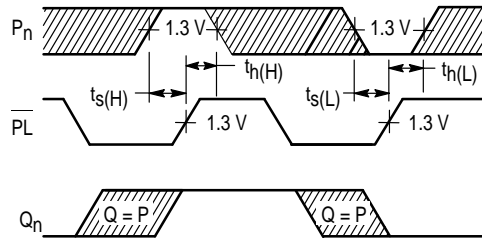
**Figure 3**



**Figure 4**

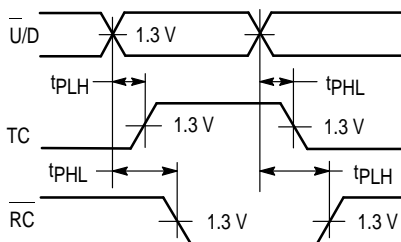


**Figure 5**

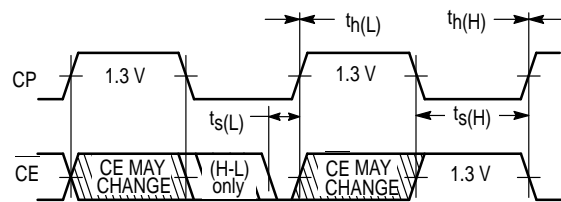


\* The shaded areas indicate when the input is permitted to change for predictable output performance

**Figure 6**



**Figure 7**



**Figure 8**