MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

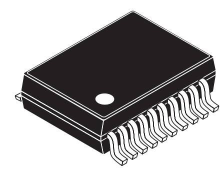
Document order number: MPC17529
Rev 1.0, 03/2004

Advance Information

17529

0.7 A Dual H-Bridge Motor Driver with 3.0 V/5.0 V Compatible Logic I/O

3.0 V/5.0 V LOGIC COMPATIBLE 0.7 A DUAL H-BRIDGE MOTOR DRIVER IC



EV (Pb-FREE) SUFFIX
CASE 1569-01
20-LEAD VMFP

The 17529 is a monolithic dual H-Bridge power IC ideal for portable electronic applications containing bipolar step motors and/or brush DC-motors (e.g., cameras and disk drive head positioners).

The 17529 operates from 2.0 V to 6.8 V, with independent control of each H-Bridge via parallel MCU interface (3.0 V- and 5.0 V-compatible logic). The device features on-board charge pump, as well as built-in shoot-through current protection and an undervoltage shutdown function.

The 17529 has four operating modes: Forward, Reverse, Brake, and Tri-Stated (High Impedance). The 17529 has a low total $R_{DS(ON)}$ of 1.2 Ω (max @ 25°C).

The 17529's low output resistance and high slew rates provide efficient drive for many types of micromotors.

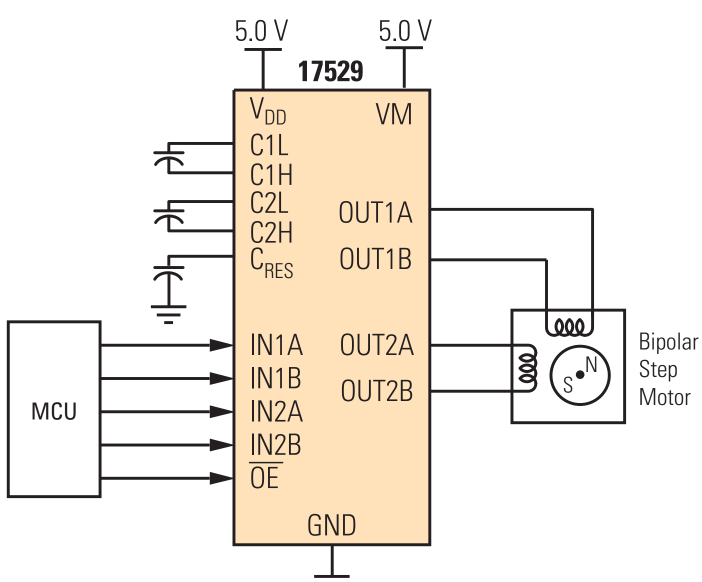
Features

- Low Total $R_{DS(ON)}$ 0.7 Ω (Typ), 1.2 Ω (Max) @ 25°C
- Output Current 0.7 A (DC), 1.4 A (Peak)
- Shoot-Through Current Protection Circuit
- 3.0 V/5.0 V CMOS-Compatible Inputs
- PWM Control Input Frequency up to 200 kHz
- Built-In Charge Pump Circuit
- Low Power Consumption
- Undervoltage Detection and Shutdown Circuit
- Pb-Free Packaging Designated by Suffix Code EV

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MPC17529EV/EL	-20°C to 65°C	20 VMFP

17529 Simplified Application Diagram



This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

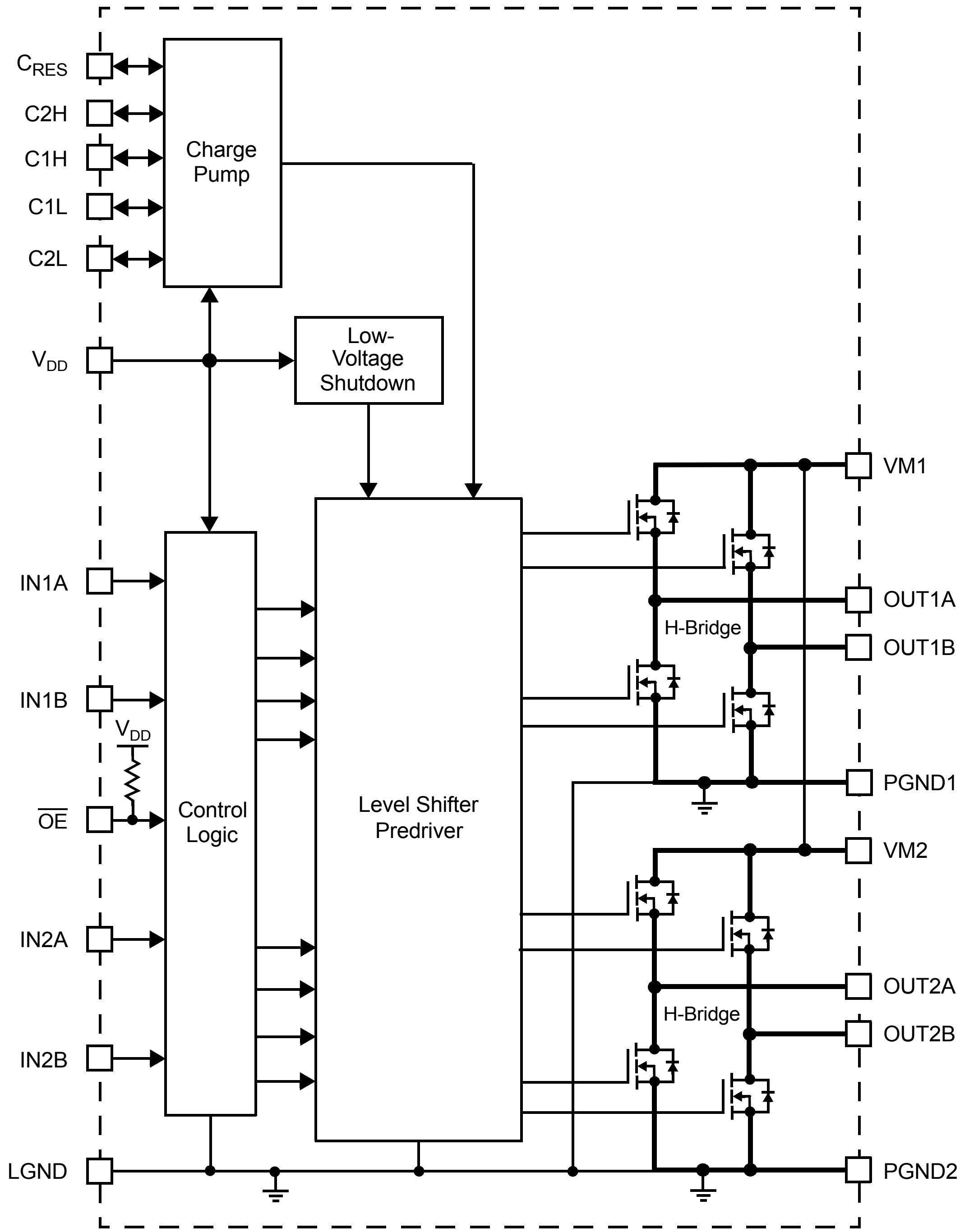
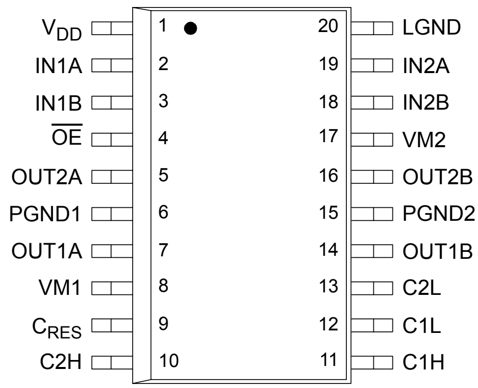


Figure 1. 17529 Simplified Internal Block Diagram



TERMINAL FUNCTION DESCRIPTION

Terminal	Terminal Name	Formal Name	Definition
1	V_{DD}	Control Circuit Power Supply	Positive power source connection for control circuit.
2	IN1A	Logic Input Control 1A	Logic input control of OUT1A (refer to Table 1, Truth Table, page 7).
3	IN1B	Logic Input Control 1B	Logic input control of OUT1B (refer to Table 1, Truth Table, page 7).
4	$\overline{OE}$	Output Enable	Logic output Enable control of H-Bridges (Low = True).
5	OUT2A	H-Bridge Output 2A	Output A of H-Bridge channel 2.
6	PGND1	Power Ground 1	High-current power ground 1.
7	OUT1A	H-Bridge Output 1A	Output A of H-Bridge channel 1.
8	VM1	Motor Drive Power Supply 1	Positive power source connection for H-Bridge 1 (Motor Drive Power Supply).
9	C_{RES}	Predriver Power Supply	Internal triple charge pump output as predriver power supply.
10	C2H	Charge Pump 2H	Charge pump bucket capacitor 2 (positive pole).
11	C1H	Charge Pump 1H	Charge pump bucket capacitor 1 (positive pole).
12	C1L	Charge Pump 1L	Charge pump bucket capacitor 1 (negative pole).
13	C2L	Charge Pump 2L	Charge pump bucket capacitor 2 (negative pole).
14	OUT1B	H-Bridge Output 1B	Output B of H-Bridge channel 1.
15	PGND2	Power Ground 2	High-current power ground 2.
16	OUT2B	H-Bridge Output 2B	Output B of H-Bridge channel 2.
17	VM2	Motor Drive Power Supply 2	Positive power source connection for H-Bridge 2 (Motor Drive Power Supply).
18	IN2B	Logic Input Control 2B	Logic input control of OUT2B (refer to Table 1, Truth Table, page 7).
19	IN2A	Logic Input Control 2A	Logic input control of OUT2A (refer to Table 1, Truth Table, page 7).
20	LGND	Logic Ground	Low-current logic signal ground.

MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted. Exceeding the ratings may cause a malfunction or permanent damage to the device.

Rating	Symbol	Value	Unit
Motor Supply Voltage	V_M	-0.5 to 8.0	V
Charge Pump Output Voltage	$V_{C_{RES}}$	-0.5 to 14	V
Logic Supply Voltage	V_{DD}	-0.5 to 7.0	V
Signal Input Voltage	V_{IN}	-0.5 to V_{DD}+0.5	V
Driver Output Current Continuous Peak (Note 1)	 I_O I_{OPK}	 0.7 1.4	A
ESD Voltage Human Body Model (Note 2) Machine Model (Note 3)	 V_{ESD1} V_{ESD2}	 ±1500 ±200	V
Operating Junction Temperature	T_J	-20 to 150	°C
Operating Ambient Temperature	T_A	-20 to 65	°C
Storage Temperature Range	T_{STG}	-65 to 150	°C
Thermal Resistance (Note 4)	$R_{\theta JA}$	120	°C/W
Power Dissipation (Note 5)	P_D	1040	mW
Soldering Temperature (Note 6)	T_{SOLDER}	260	°C

Notes

1. T_A = 25°C, 10 ms pulse at 200 ms interval.
2. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
3. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
4. Mounted on 37 x 50 Cu area (1.6 mm FR-4 PCB).
5. T_A = 25°C.
6. Soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions T_A = 25°C, V_{DD} = V_M = 5.0 V, GND = 0 V unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER					
Motor Supply Voltage	V_M	2.0	5.0	6.8	V
Logic Supply Voltage	V_{DD}	2.7	5.0	5.6	V
Driver Quiescent Supply Current (No Signal Input)	I_{QM}	–	–	1.0	µA
Logic Quiescent Supply Current (No Signal Input) (Note 7)	I_{QVDD}	–	–	1.0	mA
Operating Power Supply Current					mA
Logic Supply Current (Note 8)	I_{VDD}	–	–	3.0	
Charge Pump Circuit Supply Current (Note 9)	I_{CRES}	–	–	0.7	
Low V_{DD} Detection Voltage (Note 10)	V_{DD} DET	1.5	2.0	2.5	V
Driver Output ON Resistance (Note 11)	$R_{DS(ON)}$	–	0.7	1.2	Ω
GATE DRIVE					
Gate Drive Voltage	V_{CRES}	12	13	13.5	V
Recommended External Capacitance (C1L–C1H, C2L–C2H, C_{RES}–GND)	C_{CP}	0.01	0.1	1.0	µF
CONTROL LOGIC					
Logic Input Voltage	V_{IN}	0	–	V_{DD}	V
Logic Inputs (2.7 V < V_{DD} < 5.7 V)					
High-Level Input Voltage	V_{IH}	V_{DD} x 0.7	–	–	V
Low-Level Input Voltage	V_{IL}	–	–	V_{DD} x 0.3	V
High-Level Input Current	I_{IH}	–	–	1.0	µA
Low-Level Input Current	I_{IL}	-1.0	–	–	µA
$\overline{OE}$ Terminal Input Current Low	I_{IL}-$\overline{OE}$	–	50	100	µA

Notes

7. I_{QVDD} includes the current to predriver circuit.
8. I_{VDD} includes the current to predriver circuit at f_{IN} = 100 kHz.
9. At f_{IN} = 20 kHz.
10. Detection voltage is defined as when the output becomes high-impedance after V_{DD} drops below the detection threshold. When the gate voltage V_{CRES} is applied from an external source, V_{CRES} = 7.5 V.
11. Source + sink at I_O = 0.7 A.

DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions T_A = 25°C, V_{DD} = V_M = 5.0 V, GND = 0 V unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT					
Pulse Input Frequency	f_{IN}	–	–	200	kHz
Input Pulse Rise Time (Note 12)	t_R	–	–	1.0 (Note 13)	µs
Input Pulse Fall Time (Note 14)	t_F	–	–	1.0 (Note 13)	µs
OUTPUT					
Propagation Delay Time (Note 15)					µs
Turn-ON Time	t_{PLH}	–	0.1	0.5	
Turn-OFF Time	t_{PHL}	–	0.1	0.5	
Charge Pump Wake-Up Time (Note 16)	t_{VGON}	–	1.0	3.0	ms
Low-Voltage Detection Time	$t_{V_{DD}\,DET}$	–	–	10	ms

Notes
12. Time is defined between 10% and 90%.
13. That is, the input waveform slope must be steeper than this.
14. Time is defined between 90% and 10%.
15. Load of Output is 8.0 Ω resistance.
16. C_{CP} = 0.1 µF.

Timing Diagrams

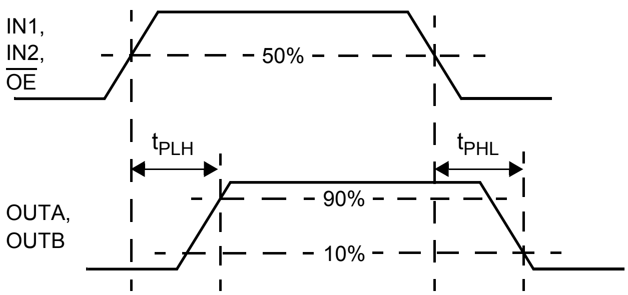


Figure 2. t_{PLH}, t_{PHL}, and t_{PZH} Timing

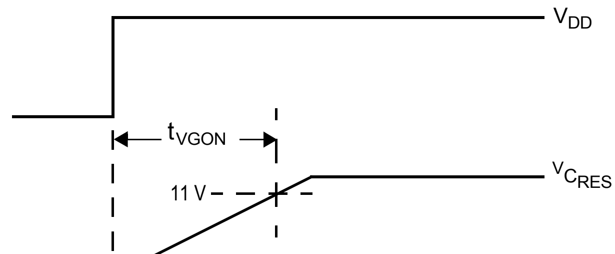


Figure 4. Charge Pump Timing Diagram

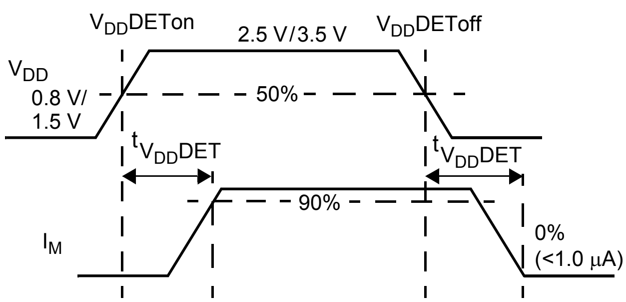


Figure 3. Low-Voltage Detection Timing Diagram

Table 1. Truth Table

INPUT			OUTPUT	
$\overline{OE}$	IN1A IN2A	IN1B IN2B	OUT1A OUT2A	OUT1B OUT2B
L	L	L	L	L
L	H	L	H	L
L	L	H	L	H
L	H	H	Z	Z
H	X	X	Z	Z

H = High.
L = Low.
Z = High impedance.
X = Don't care.
$\overline{OE}$ terminal is pulled up to V_{DD} with internal resistance.

SYSTEM/APPLICATION INFORMATION

INTRODUCTION

The 17529 is a monolithic dual H-Bridge ideal for portable electronic applications to control bipolar step motors and brush DC motors such as those found in camera len assemblies, camera shutters, optical disk drives, etc. The 17529 operates from 2.0 V to 6.8 V, providing dual H-bridge motor drivers with parallel 3.0 V- or 5.0 V-compatible I/O. The device features an on-board charge pump, as well as built-in shoot-through current protection and undervoltage shutdown.

The 17529 has four operating modes: Forward, Reverse, Brake, and Tri-Stated (High Impedance). The MOSFETs comprising the output bridge have a total source + sink $R_{DS(ON)}$ $\leq 1.2\ \Omega$.

The 17529 can simultaneously drive two brush DC motors or, as shown in the simplified application diagram on page 1, one bipolar step motor. The drivers are designed to be PWM'ed at frequencies up to 200 kHz.

FUNCTIONAL TERMINAL DESCRIPTION

V_{DD}

The V_{DD} terminal carries the logic supply voltage and current into the logic sections of the IC. V_{DD} has an undervoltage threshold. If the supply voltage drops below the undervoltage threshold, the output power stage switches to a tri-state condition. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input terminals.

IN1A, IN1B, IN2A, and IN2B

These logic input terminals control each H-Bridge output. IN1A logic HIGH = OUT1A HIGH. However, if all inputs are taken HIGH, the outputs bridges are both tri-stated (refer to Table 1, Truth Table, page 7).

$\overline{OE}$

The $\overline{OE}$ terminal is a LOW = TRUE enable input. When $\overline{OE}$ = HIGH, all H-Bridge outputs (OUT1A, OUT1B, OUT2A, and OUT2B) are tri-stated (high-impedance), regardless of logic inputs (IN1A, IN1B, IN2A, and IN2B) states.

OUT1A, OUT1B, OUT2A, and OUT2B

These terminals provide connection to the outputs of each of the internal H-Bridges (see Figure 1, 17529 Simplified Internal Block Diagram, page 2).

VM1 and VM2

The VM terminals carry the main supply voltage and current into the power sections of the IC. This supply then becomes controlled and/or modulated by the IC as it delivers the power to the loads attached between the output terminals. All VM terminals must be connected together on the printed circuit board.

C1L and C1H, C2L and C2H

These two pairs of terminals, the C1L and C1H and the C2L and C2H, connect to the external bucket capacitors required by the internal charge pump. The typical value for the bucket capacitors is 0.1 μF.

C_{RES}

The C_{RES} terminal is the output of the internal charge pump. Its output voltage is approximately three times the V_{DD} voltage. The $V_{C_{RES}}$ voltage is power supply for internal predriver circuit of H-Bridges.

PGND

Power ground terminals. They must be tied together on the PCB.

LGND

Logic ground terminal.

APPLICATIONS

Typical Application

Figure 5 shows a typical application for the 17529. When applying the gate voltage to the C_{RES} terminal from an external source, be sure to connect it via a resistor equal to, or greater than, $R_G = V_{C_{RES}}/0.02\ \Omega$.

The internal charge pump of this device is generated from the V_{DD} supply; therefore, care must be taken to provide sufficient gate-source voltage for the high-side MOSFETs when $V_M >> V_{DD}$ (e.g., V_M = 5.0 V, V_{DD} = 3.0 V), in order to ensure full enhancement of the high-side MOSFET channels.

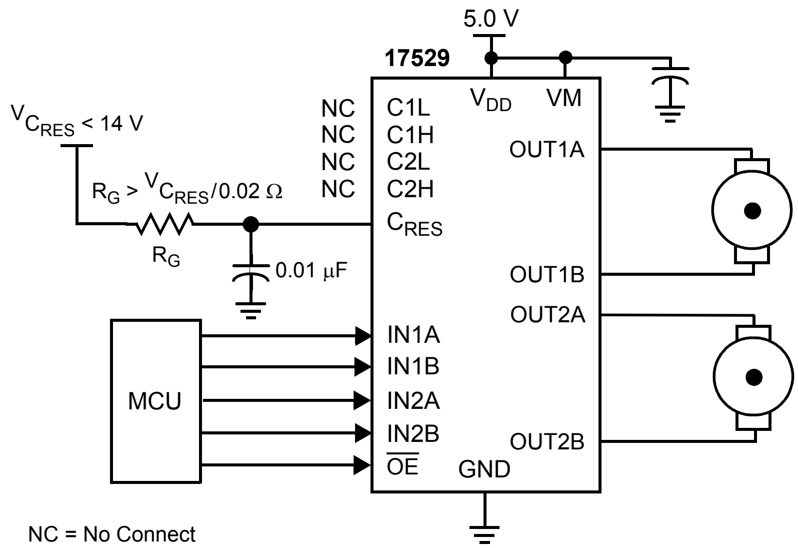


Figure 5. 17529 Typical Application Diagram

CEMF Snubbing Techniques

Care must be taken to protect the IC from potentially damaging CEMF spikes induced when commutating currents in inductive loads. Typical practice is to provide snubbing of voltage transients by placing a capacitor or zener at the supply terminal (VM) (see Figure 6).

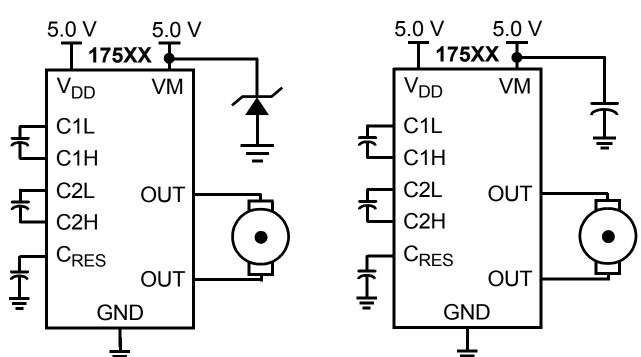


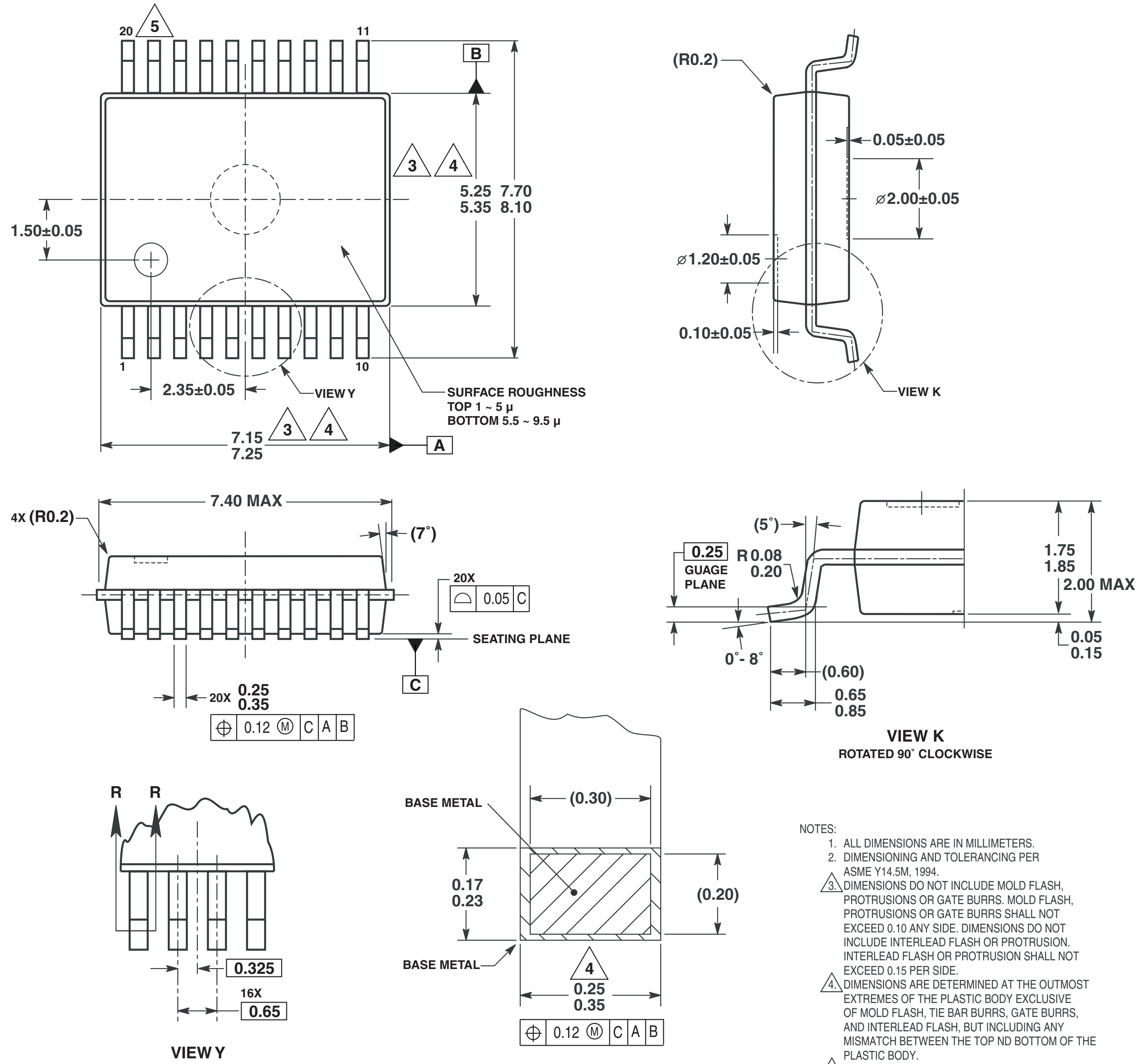
Figure 6. CEMF Snubbing Techniques

PCB Layout

When designing the printed circuit board (PCB), connect sufficient capacitance between power supply and ground terminals to ensure proper filtering from transients. For all high-current paths, use wide copper traces and shortest possible distances.

PACKAGE DIMENSIONS

EV (Pb-FREE) SUFFIX
20-LEAD VMFP
PLASTIC PACKAGE
CASE 1569-01
ISSUE O



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.10 ANY SIDE. DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSIONS ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS, AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP ND BOTTOM OF THE PLASTIC BODY.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

NOTES

HOW TO REACH US:

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