3.3 VOLT DUAL MULTIMEDIA FIFO
DUAL 256 x 8, DUAL 512 x 8
DUAL 1,024 x 8, DUAL 2,048 x 8
DUAL 4,096 x 8

PRELIMINARY
IDT72V10071, IDT72V11071
IDT72V12071, IDT72V13071
IDT72V14071

FEATURES:

- **Memory organization:**
  - **IDT72V10071 — Dual 256 x 8**
  - **IDT72V11071 — Dual 512 x 8**
  - **IDT72V12071 — Dual 1,024 x 8**
  - **IDT72V13071 — Dual 2,048 x 8**
  - **IDT72V14071 — Dual 4,096 x 8**
- **Offers optimal combination of large capacity, high speed, design flexibility and small footprint**
- **15 ns read/write cycle time**
- **5V input tolerant**
- **Separate control lines and data lines for each FIFO**
- **Separate Empty and Full flags for each FIFO**
- **Enable puts output data lines in high-impedance state**
- **Space-saving 64-pin plastic Thin Quad Flat Pack (STQFP)**
- **Industrial temperature range (–40°C to +85°C)**

DESCRIPTION:

The IDT72V10071/72V11071/72V12071/72V13071/72V14071 are dual Multimedia FIFOs. The device is functionally equivalent to two independent FIFOs in a single package with all associated control, data, and flag lines assigned to separate pins.

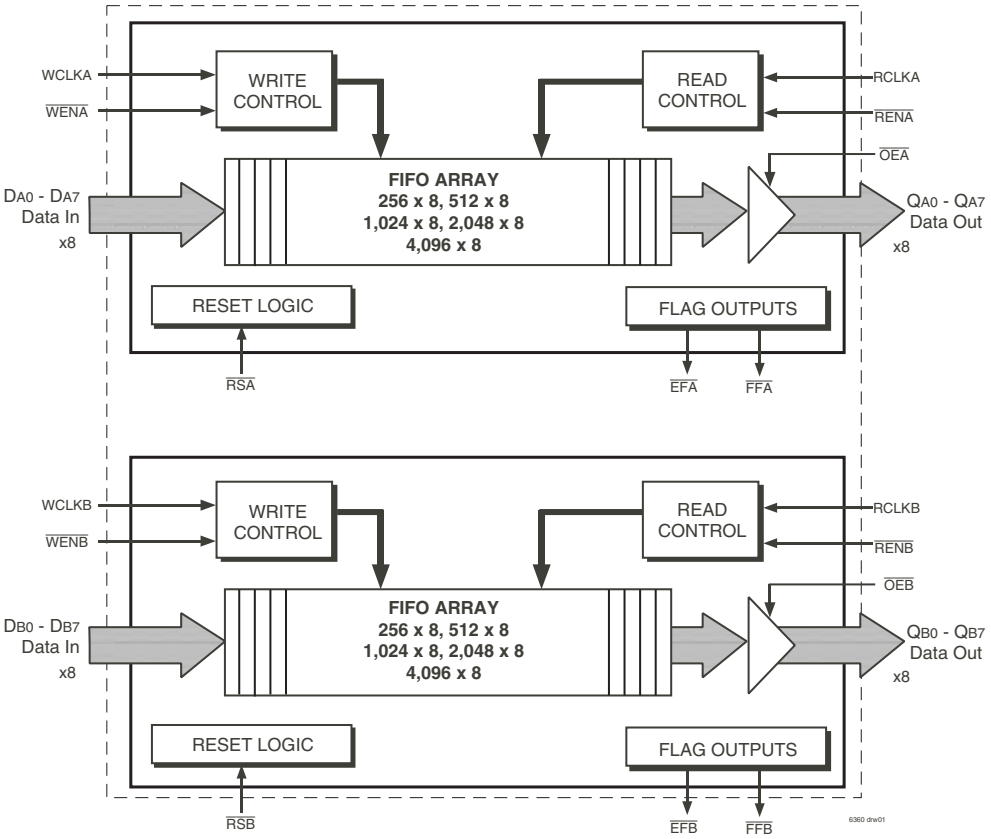
Each of the two FIFOs (designated FIFO A and FIFO B) has a 8-bit input data port (DA0 - DA7, DB0 - DB7) and a 8-bit output data port (QA0 - QA7, QB0 - QB7). Each input port is controlled by a free-running clock (WCLKA, WCLKB), and a Write Enable pin ($\overline{WENA}$, $\overline{WENB}$). Data is written into each of the two arrays on every rising clock edge of the Write Clock (WCLKA, WCLKB) when the appropriate Write Enable pin is asserted.

The output port of each FIFO bank is controlled by its associated clock pin (RCLKA, RCLKB) and Read Enable pin ($\overline{RENA}$, $\overline{RENB}$). The Read Clock can be tied to the Write Clock for single clock operation or the two clocks can run asynchronous of one another for dual clock operation. An Output Enable pin ($\overline{OEA}$, $\overline{OEB}$) is provided on the read port of each FIFO for three-state output control.

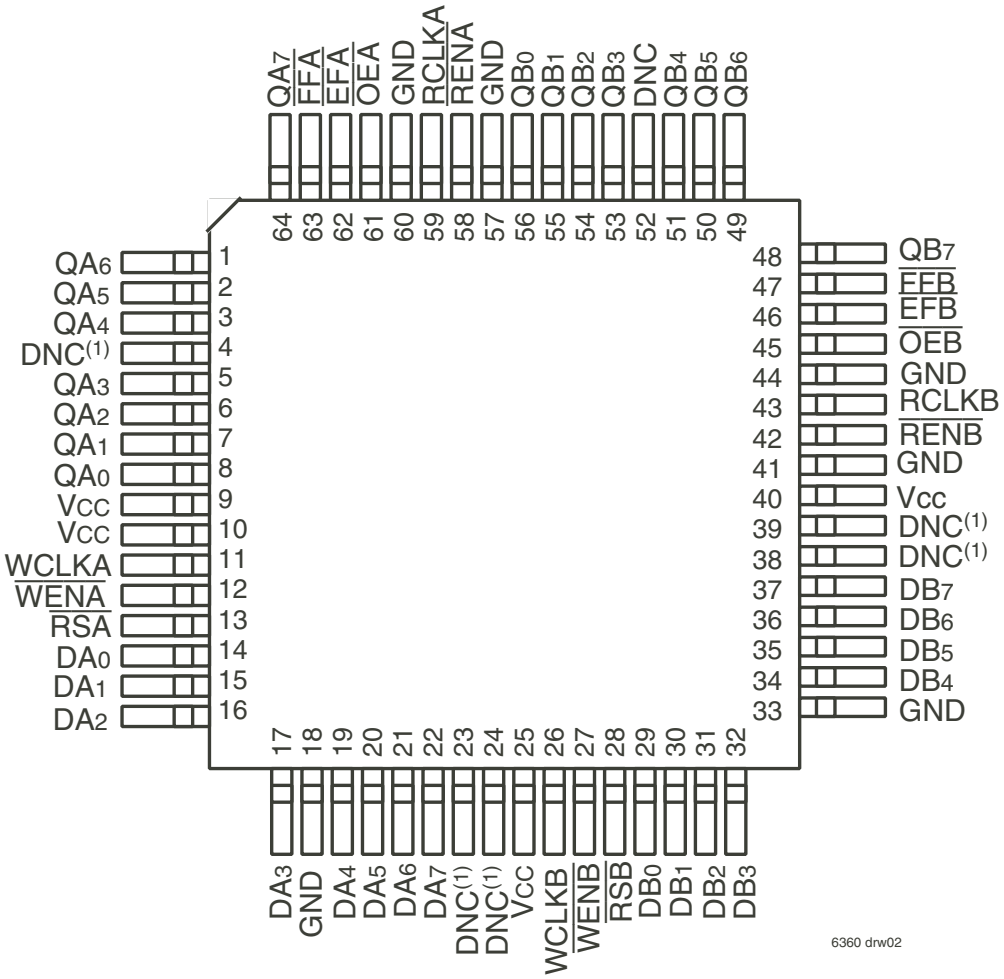
Each of the two FIFOs has two fixed flags, Empty ($\overline{EFA}$, $\overline{EFB}$) and Full ($\overline{FFA}$, $\overline{FFB}$).

This FIFO is fabricated using IDT's high-performance submicron CMOS technology.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



NOTE:
1. DNC = Do Not Connect.

STQFP (PP64-1, order code: TF)
TOP VIEW

PIN DESCRIPTIONS

The IDT72V10071/72V11071/72V12071/72V13071/72V14071's two FIFOs, referred to as FIFO A and FIFO B, are identical in every respect. FIFO A and FIFO B operate completely independent from each other.

Symbol	Name	I/O	Description
DA0-DA7	A Data Inputs	I	8-bit data inputs to FIFO array A.
DB0-DB7	B Data Inputs	I	8-bit data inputs to FIFO array B.
$\overline{RSA}$, $\overline{RSB}$	Reset	I	When $\overline{RSA}$ ($\overline{RSB}$) is set LOW, the associated internal read and write pointers of array A (B) are set to the first location; $\overline{FFA}$ ($\overline{FFB}$) go as HIGH and $\overline{EFA}$ ($\overline{EFB}$) go as LOW. After power-up, a reset of both FIFOs A and B is required before an initial WRITE.
WCLKA WCLKB	Write Clock	I	Data is written into the FIFO A (B) on a LOW-to-HIGH transition of WCLKA (WCLKB) when the write enable is asserted.
$\overline{WENA}$ $\overline{WENB}$	Write Enable	I	When $\overline{WENA}$ ($\overline{WENB}$) is LOW, data A (B) is written into the FIFO on every LOW-to-HIGH transition WCLKA (WCLKB). Data will not be written into the FIFO if $\overline{FFA}$ ($\overline{FFB}$) is LOW.
QA0-QA7	A Data Outputs	O	8-bit data outputs from FIFO array A.
QB0-QB7	B Data Outputs	O	8-bit data outputs from FIFO array B.
RCLKA RCLKB	Read Clock	I	Data is read from FIFO A (B) on a LOW-to-HIGH transition of RCLKA (RCLKB) when $\overline{RENA}$ ($\overline{RENB}$) is asserted.
$\overline{RENA}$ $\overline{RENB}$	Read Enable	I	When $\overline{RENA}$ ($\overline{RENB}$) is LOW, data is read from FIFO A (B) on every LOW-to-HIGH transition of RCLKA (RCLKB). Data will not be read from Array A (B) if $\overline{EFA}$ ($\overline{EFB}$) is LOW.
$\overline{OEA}$ $\overline{OEB}$	Output Enable	I	When $\overline{OEA}$ ($\overline{OEB}$) is LOW, outputs DA0-DA7 (DB0-DB7) are active. If $\overline{OEA}$ ($\overline{OEB}$) is HIGH, outputs DA0-DA7 (DB0-DB7) will be in a high-impedance state.
$\overline{EFA}$ $\overline{EFB}$	Empty Flag	O	When $\overline{EFA}$ ($\overline{EFB}$) is LOW, FIFO A (B) is empty and further data reads from the output are inhibited. When $\overline{EFA}$ ($\overline{EFB}$) is HIGH, FIFO A (B) is not empty. $\overline{EFA}$ ($\overline{EFB}$) is synchronized to RCLKA (RCLKB).
$\overline{FFA}$ $\overline{FFB}$	Full Flag	O	When $\overline{FFA}$ ($\overline{FFB}$) is LOW, FIFO A (B) is full and further data writes into the input are inhibited. When $\overline{FFA}$ ($\overline{FFB}$) is HIGH, FIFO A (B) is not full. $\overline{FFA}$ ($\overline{FFB}$) is synchronized to WCLKA (WCLKB).
V_{CC}	Power		+3.3V power supply pin.
GND	Ground		0V ground pin.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Industrial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +5	V
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	–50 to +50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ.	Max	Unit
V_{CC}	Supply Voltage(Industrial)	3.0	3.3	3.6	V
GND	Supply Voltage(Industrial)	0	0	—	V
V_{IH}	Input High Voltage (Industrial)	2.0	—	5.0	V
V_{IL}	Input Low Voltage (Industrial)	—	—	0.8	V
T_A	Operating Temperature Industrial	-40	—	85	°C

NOTE:
1. Outputs are not 5V tolerant.

DC ELECTRICAL CHARACTERISTICS

(Industrial :V_{CC} = 3.3V ± 0.3V, TA = -40°C to +85°C)

Symbol	Parameter	IDT72V10071 IDT72V11071 IDT72V12071 IDT72V13071 IDT72V14071 Industrial t_{CLK} = 15 ns			Unit
		Min.	Typ.	Max.	
I_{LI}(1)	Input Leakage Current (Any Input)	–1	—	–1	µA
I_{LO}(2)	Output Leakage Current	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = –2 mA	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8 mA	—	—	0.4	V
I_{CC1}(3,4,5)	Active Power Supply Current (both FIFOs)	—	—	40	mA
I_{CC2}(2,6)	Standby Current	—	—	10	mA

NOTES:
1. Measurements with $0.4 \leq V_{IN} \leq V_{CC}$.
2. $\overline{OEA}$, $\overline{OEB} \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$.
3. Tested with outputs disabled (I_{OUT} = 0).
4. RCLK and WCLK toggle at 20 MHz and data inputs switch at 10 MHz.
5. Typical I_{CC1} = 2[0.17 + 0.48*fs + 0.02*C_L*fs] (in mA).
   These equations are valid under the following conditions:
   V_{CC} = 3.3V, T_A = 25°C, fs = WCLK frequency = RCLK frequency (in MHz, using TTL levels), data switching at fs/2, C_L = capacitive load (in pF).
6. All Inputs = V_{CC} - 0.2V or GND + 0.2V, except RCLK and WCLK, which toggle at 20 MHz.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}(2)	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}(1,2)	Output Capacitance	V_{OUT} = 0V	10	pF

NOTE:
1. With output deselected ($\overline{OEA}$, $\overline{OEB} \geq V_{IH}$).
2. Characterized values, not currently tested.

AC ELECTRICAL CHARACTERISTICS[1]

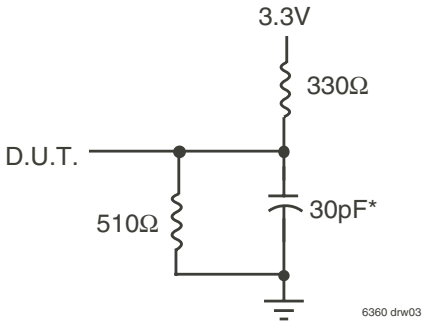
(Industrial: Vcc = 3.3V± 0.3V, TA = -40°C to +85°C)

Symbol	Parameter	Industrial IDT72V10071L15 IDT72V11071L15 IDT72V12071L15 IDT72V13071L15 IDT72V14071L15 Min.	Max.	Unit
fS	Clock Cycle Frequency	—	66.7	MHz
tA	Data Access Time	2	10	ns
tCLK	Clock Cycle Time	15	—	ns
tCLKH	Clock High Time	6	—	ns
tCLKL	Clock Low Time	6	—	ns
tDS	Data Set-up Time	4	—	ns
tDH	Data Hold Time	1	—	ns
tENS	Enable Set-up Time	4	—	ns
tENH	Enable Hold Time	1	—	ns
tRS	Reset Pulse Width[1]	15	—	ns
tRSS	Reset Set-up Time	10	—	ns
tRSR	Reset Recovery Time	10	—	ns
tRSF	Reset to Flag Time and Output Time	—	15	ns
tOLZ	Output Enable to Output in Low-Z[2]	0	—	ns
tOE	Output Enable to Output Valid	3	8	ns
tOHZ	Output Enable to Output in High-Z[2]	3	8	ns
tWFF	Write Clock to Full Flag	—	10	ns
tREF	Read Clock to Empty Flag	—	10	ns
tSKEW1	Skew Time Between Read Clock and Write Clock for Empty Flag and Full Flag	6	—	ns

NOTES:
1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1



or equivalent circuit

Figure 1. Output Load

*Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS

FIFO A and FIFO B are identical in every respect. The following description explains the interaction of input and output signals for FIFO A. The corresponding signal names for FIFO B are provided in parentheses.

INPUTS:

Data In ($D_{A0} - D_{A7}$, $D_{B0} - D_{B7}$) — D_{A0} - D_{A7} are the eight data inputs for memory array A. D_{B0} - D_{B7} are the eight data inputs for memory array B.

CONTROLS:

Reset ($\overline{RSA}$, $\overline{RSB}$) — Reset of FIFO A (B) is accomplished whenever $\overline{RSA}$ ($\overline{RSB}$) input is taken to a LOW state. During reset, the internal read and write pointers associated with the FIFO are set to the first location. A reset is required after power-up before a write operation can take place. The Full Flag, $\overline{FFA}$ ($\overline{FFB}$) will be reset to HIGH after t_{RSF}. The Empty Flag, $\overline{EFA}$ ($\overline{EFB}$) will be reset to LOW after t_{RSF}. During reset, the output register is initialized to all zeros.

Write Clock (WCLKA, WCLKB) — A write cycle to Array A (B) is initiated on the LOW-to-HIGH transition of WCLKA (WCLKB). Data set-up and hold times must be met with respect to the LOW-to-HIGH transition of WCLKA (WCLKB). The Full Flag, $\overline{FFA}$ ($\overline{FFB}$) is synchronized with respect to the LOW-to-HIGH transition of the Write Clock, WCLKA (WCLKB).

The Write and Read clock can be asynchronous or coincident.

Write Enable ($\overline{WENA}$, $\overline{WENB}$) — When $\overline{WENA}$ ($\overline{WENB}$) is LOW, data can be loaded into the input register of RAM Array A (B) on the LOW-to-HIGH transition of every Write Clock, WCLKA (WCLKB). Data is stored in Array A (B) sequentially and independently of any on-going read operation.

When $\overline{WENA}$ ($\overline{WENB}$) is HIGH, the input register holds the previous data and no new data is allowed to be loaded into the register.

To prevent data overflow, $\overline{FFA}$ ($\overline{FFB}$) will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, the $\overline{FFA}$ ($\overline{FFB}$) will go HIGH after t_{WFF}, allowing a valid write to begin. $\overline{WENA}$ ($\overline{WENB}$) is ignored when FIFO A (B) is full.

Read Clock (RCLKA, RCLKB) —

Data can be read from Array A (B) on the LOW-to-HIGH transition of RCLKA (RCLKB). The Empty Flag, $\overline{EFA}$ ($\overline{EFB}$) is synchronized with respect to the LOW-to-HIGH transition of RCLKA (RCLKB).

The Write and Read Clock can be asynchronous or coincident.

Read Enable ($\overline{RENA}$, $\overline{RENB}$) — When Read Enable, $\overline{RENA}$, ($\overline{RENB}$) is LOW, data is read from Array A (B) to the output register on the LOW-to-HIGH transition of the Read Clock, RCLKA (RCLKB).

When Read Enable, $\overline{RENA}$, ($\overline{RENB}$) for FIFO A (B) is HIGH, the output register holds the previous data and no new data is allowed to be loaded into the register.

When all the data has been read from FIFO A (B), the Empty Flag, $\overline{EFA}$ ($\overline{EFB}$) will go LOW, inhibiting further read operations. Once a valid write operation has been accomplished, $\overline{EFA}$ ($\overline{EFB}$) will go HIGH after t_{REF} and a valid read can begin. The Read Enable, $\overline{RENA}$, ($\overline{RENB}$) is ignored when FIFO A (B) is empty.

Output Enable ($\overline{OEA}$, $\overline{OEB}$) — When Output Enable, $\overline{OEA}$ ($\overline{OEB}$) is enabled (LOW), the parallel output buffers of FIFO A (B) receive data from their respective output register. When Output Enable, $\overline{OEA}$ ($\overline{OEB}$) is disabled (HIGH), the QA (QB) output data bus is in a high-impedance state.

OUTPUTS:

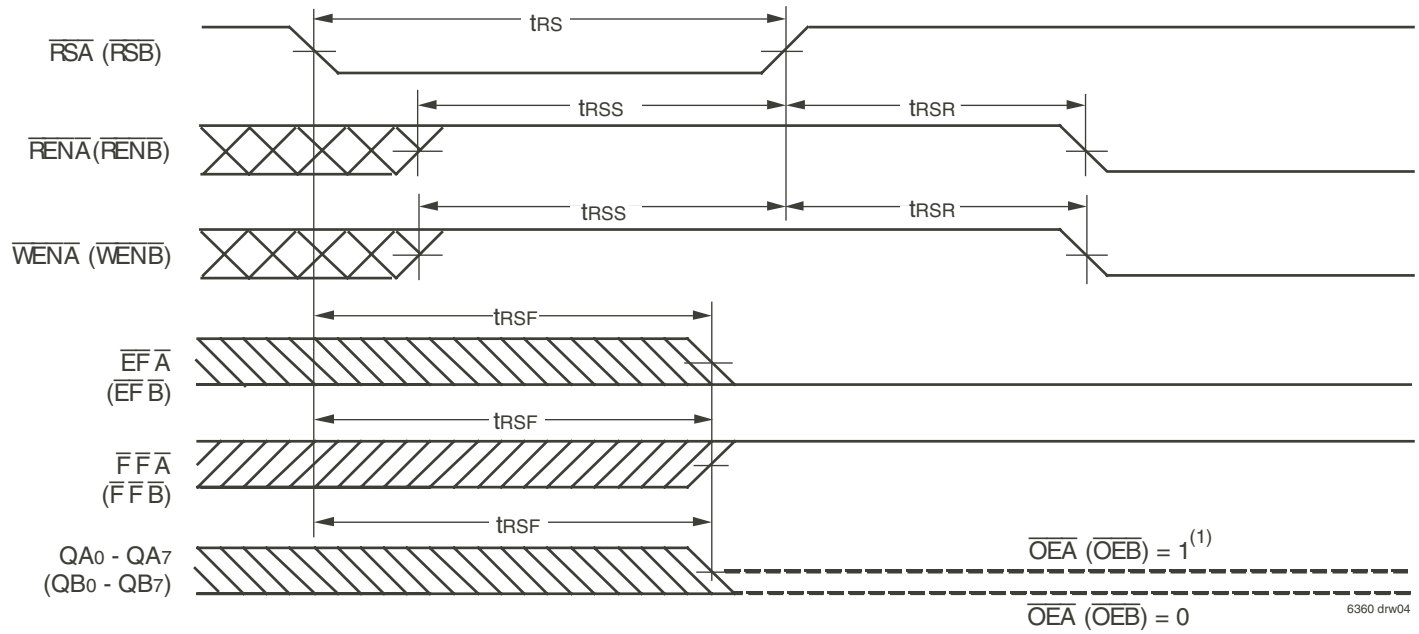
Full Flag ($\overline{FFA}$, $\overline{FFB}$) — $\overline{FFA}$ ($\overline{FFB}$) will go LOW, inhibiting further write operations, when Array A (B) is full. If no reads are performed after reset, $\overline{FFA}$ ($\overline{FFB}$) will go LOW after 256 writes to the IDT72V10071's FIFO A (B), 512 writes to the IDT72V11071's FIFO A (B), 1,024 writes to the IDT72V12071's FIFO A (B), 2,048 writes to the IDT72V13071's FIFO A (B), and 4,096 writes to the IDT72V14071's FIFO A (B).

$\overline{FFA}$ ($\overline{FFB}$) is synchronized with respect to the LOW-to-HIGH transition of the Write Clock WCLKA (WCLKB).

Empty Flag ($\overline{EFA}$, $\overline{EFB}$) — $\overline{EFA}$ ($\overline{EFB}$) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that Array A (B) is empty.

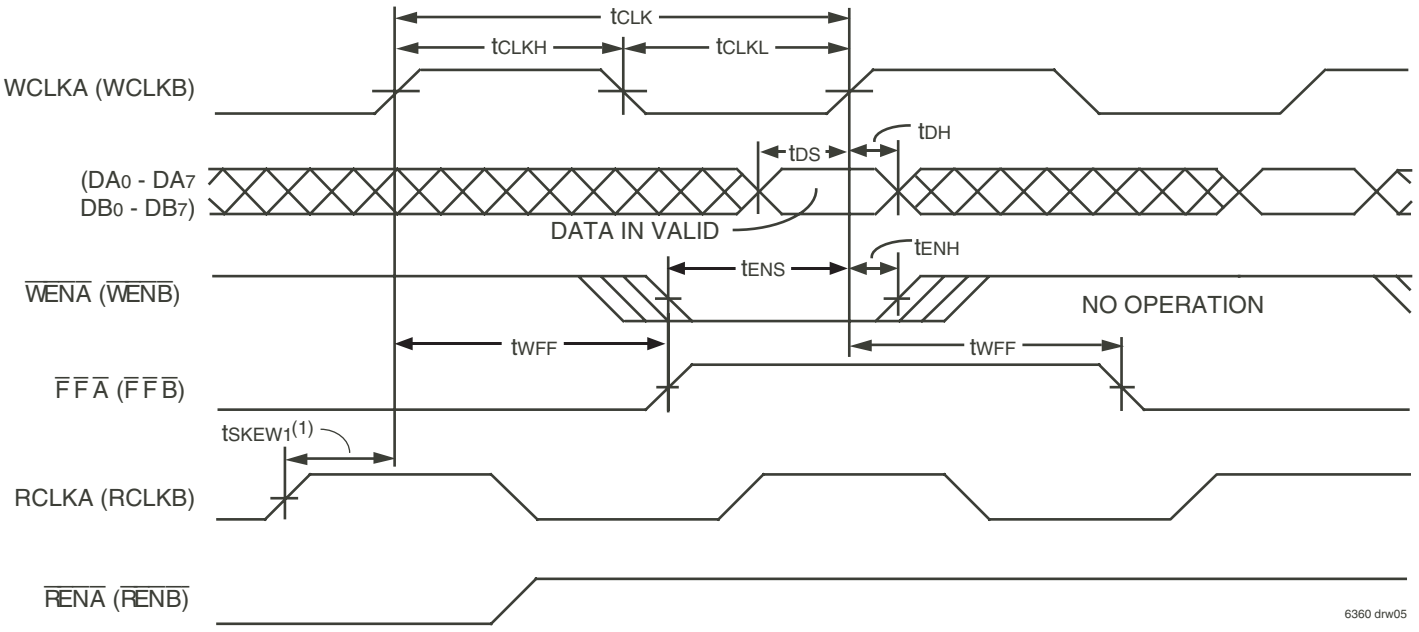
$\overline{EFA}$ ($\overline{EFB}$) is synchronized with respect to the LOW-to-HIGH transition of the Read Clock RCLKA (RCLKB).

Data Outputs ($QA_0 - QA_7$, $QB_0 - QB_7$) — QA_0 - QA_7 are the eight data outputs for memory array A, QB_0 - QB_7 are the eight data outputs for memory array B.



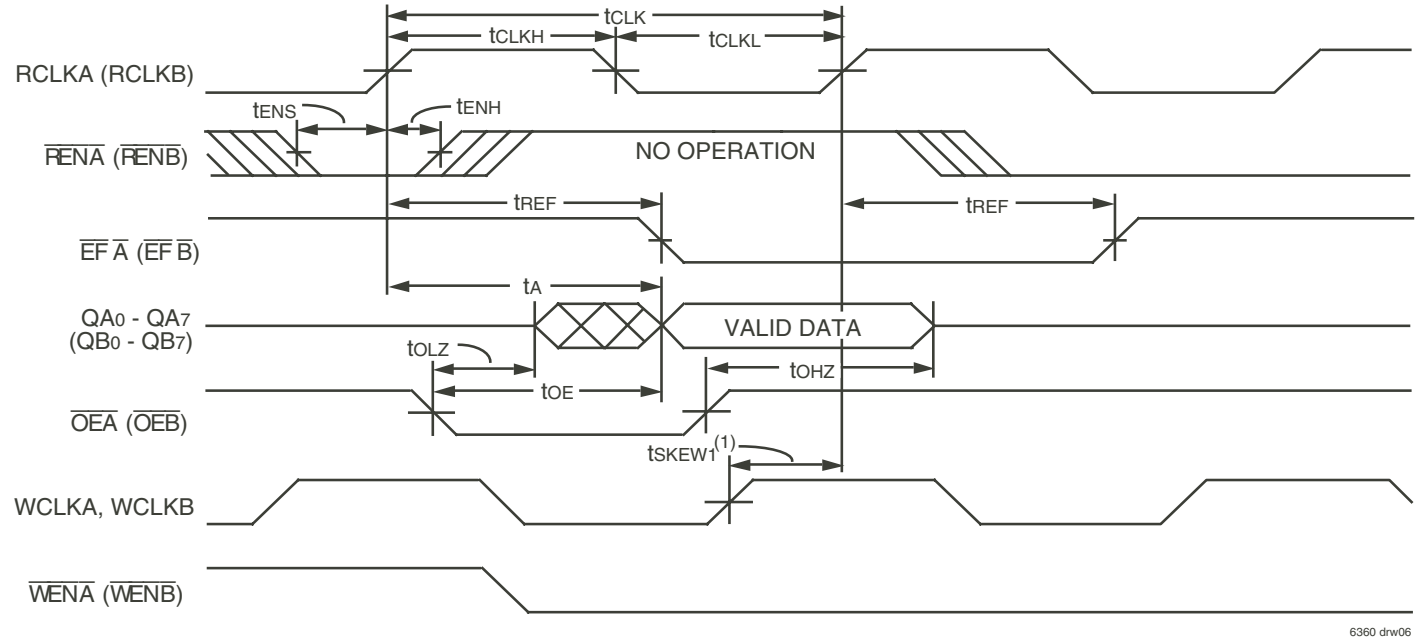
NOTES:
1. After reset, QA_0 - QA_7 (QB_0 - QB_7) will be LOW if $\overline{OEA}$ ($\overline{OEB}$) = 0 and tri-state if $\overline{OEA}$ ($\overline{OEB}$) = 1.
2. The clocks RCLKA, WCLKA (RCLKB, WCLKB) can be free-running during reset.

Figure 2. Reset Timing



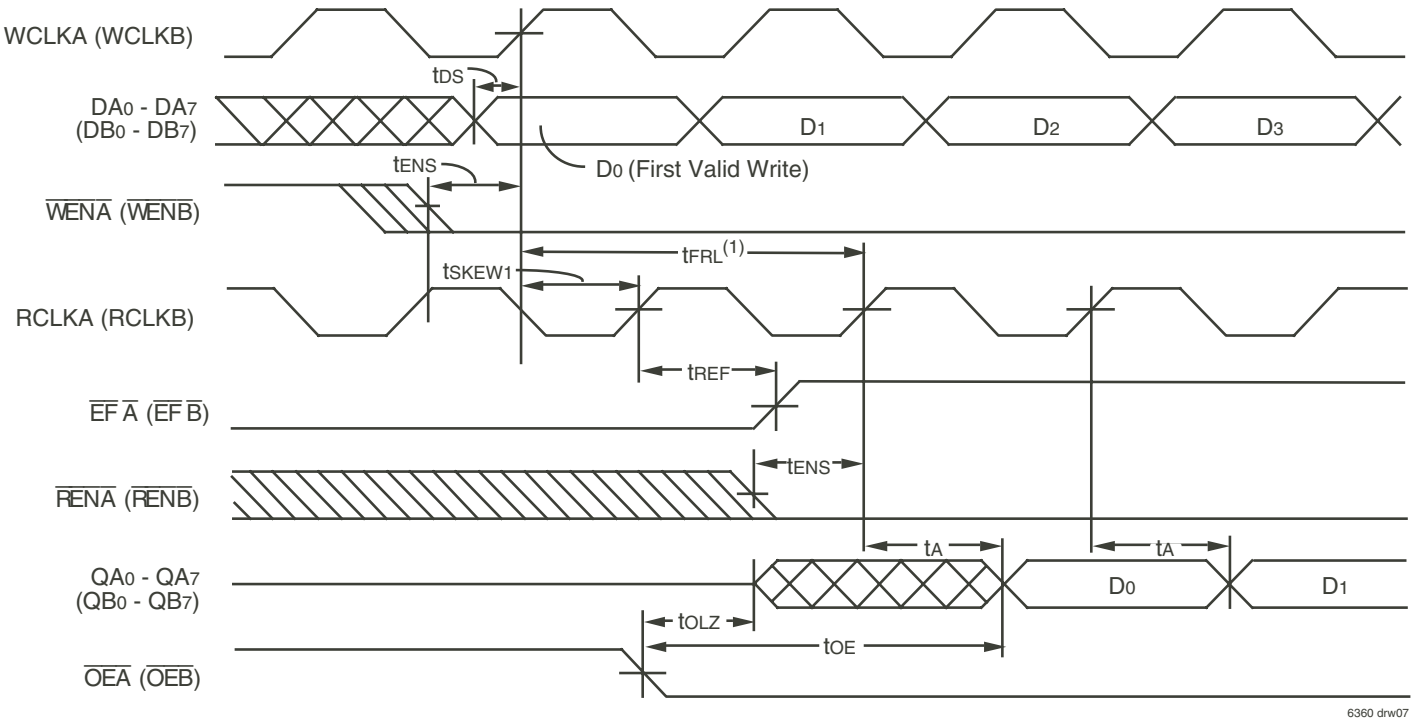
NOTE:
1. t_{SKEW1} is the minimum time between a rising RCLKA (RCLKB) edge and a rising WCLKA (WCLKB) edge for $\overline{FFA}$ ($\overline{FFB}$) to change during the current clock cycle. If the time between the rising edge of RCLKA (RCLKB) and the rising edge of WCLKA (WCLKB) is less than t_{SKEW1}, then $\overline{FFA}$ ($\overline{FFB}$) may not change state until the next WCLKA (WCLKB) edge.

Figure 3. Write Cycle Timing



NOTE:
1. t_{SKEW1} is the minimum time between a rising WCLKA (WCLKB) edge and a rising RCLKA (RCLKB) edge for $\overline{EFA}$ ($\overline{EFB}$) to change during the current clock cycle. If the time between the rising edge of RCLKA (RCLKB) and the rising edge of WCLKA (WCLKB) is less than t_{SKEW1}, then $\overline{EFA}$ ($\overline{EFB}$) may not change state until the next RCLKA (RCLKB) edge.

Figure 4. Read Cycle Timing



NOTE:
1. When $t_{SKEW1} \geq$ minimum specification, $t_{FRL} = t_{CLK} + t_{SKEW1}$
   $t_{SKEW1} <$ minimum specification, $t_{FRL} = 2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timings apply only at the Empty Boundary ($\overline{EFA}$, $\overline{EFB}$ = LOW).

Figure 5. First Data Word Latency Timing

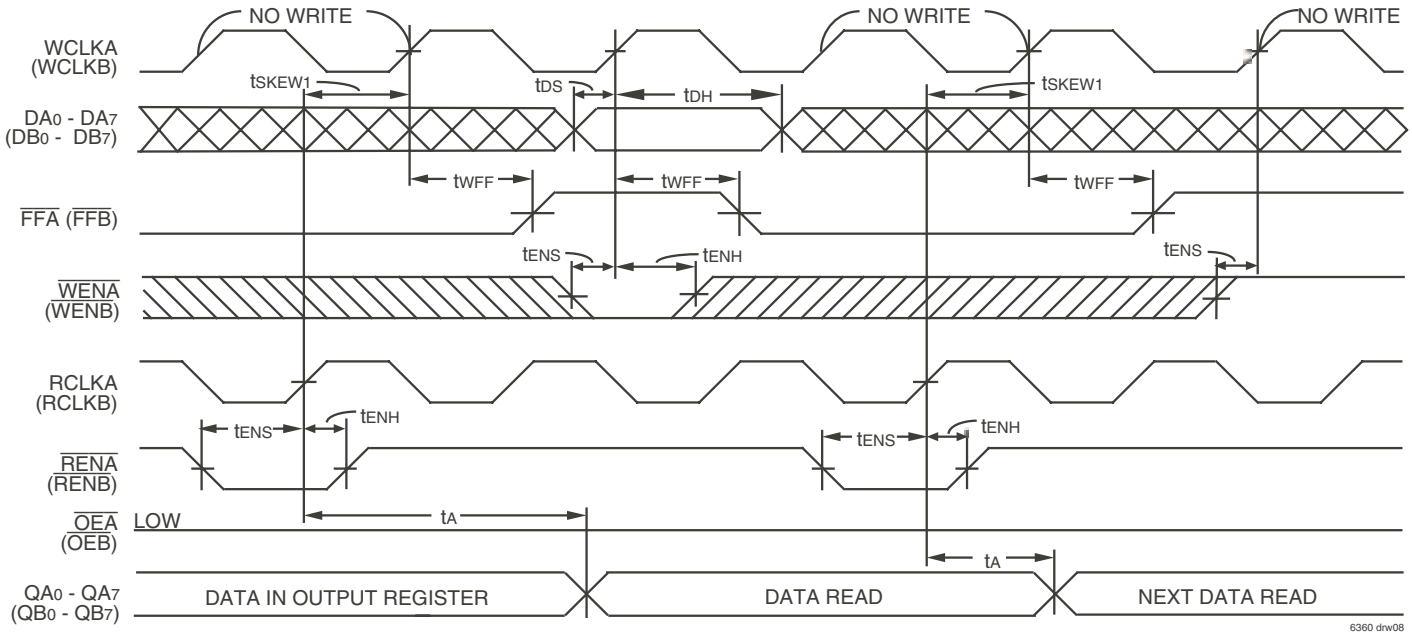
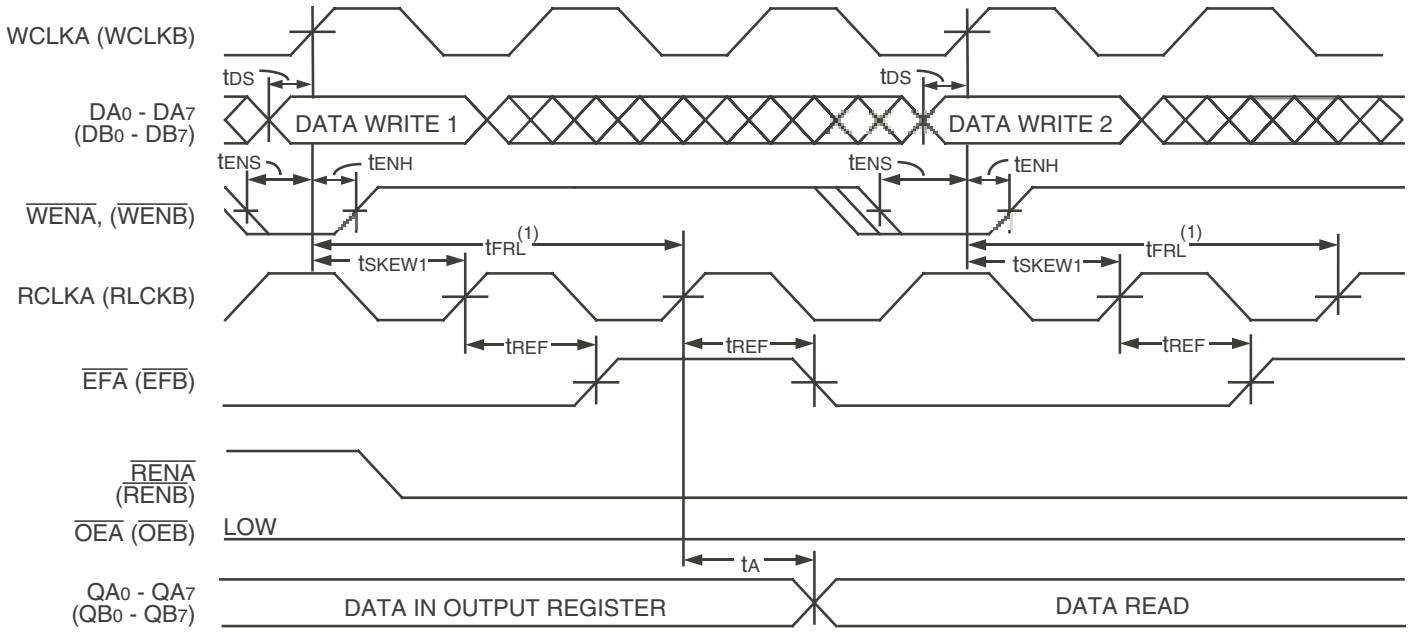


Figure 6. Full Flag Timing

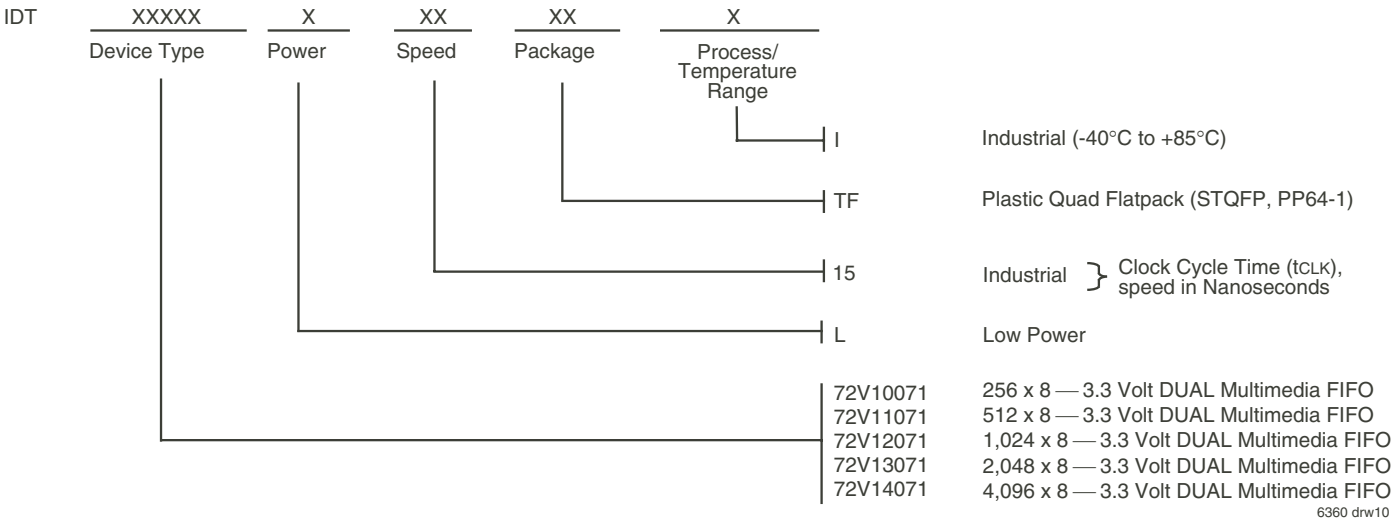


NOTE:

1. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} maximum = $t_{CLK} + t_{SKEW1}$
   t_{SKEW1} < minimum specification, t_{FRL} maximum = $2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timings apply only at the Empty Boundary ($\overline{EFA}$, $\overline{EFB}$ = LOW).

Figure 7. Empty Flag Timing

ORDERING INFORMATION



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