
HM62W1664HB Series

65536-word × 16-bit High Speed CMOS Static RAM

HITACHI

ADE-203-415A (Z)
Rev. 1.0
Dec. 25, 1996

Description

The HM62W1664HB is an asynchronous high speed static RAM organized as 64-kword × 16-bit. It realize high speed access time (25/30 ns) with employing 0.8 μm CMOS process and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. The HM62W1664HB is packaged in 400-mil 44-pin SOJ for high density surface mounting.

Features

- Single 3.3 V supply (3.3 V ± 0.3V)
- Access time: 25/30 ns (max)
- Completely static memory
 - No clock or timing strobe required
- Equal access and cycle times
- Directly LV-TTL compatible
 - All inputs and outputs
- 400-mil 44-pin SOJ package
- Center V_{CC} and V_{SS} type pinout

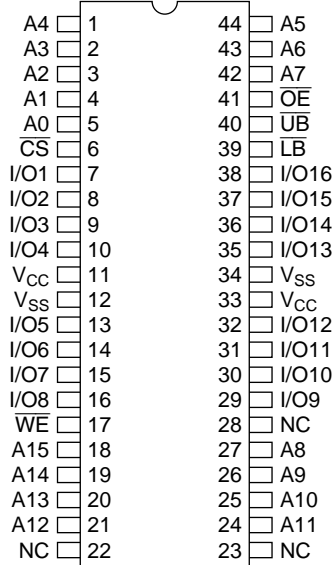
Ordering Information

| Type No. | Access time | Package |
|-------------------|-------------|-------------------------------------|
| HM62W1664HBJP-25 | 25 ns | 400-mil 44-pin plastic SOJ (CP-44D) |
| HM62W1664HBJP-30 | 30 ns | |
| HM62W1664HBLJP-25 | 25 ns | |
| HM62W1664HBLJP-30 | 30 ns | |

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Pin Arrangement

HM62W1664HBJP/HBLJP Series

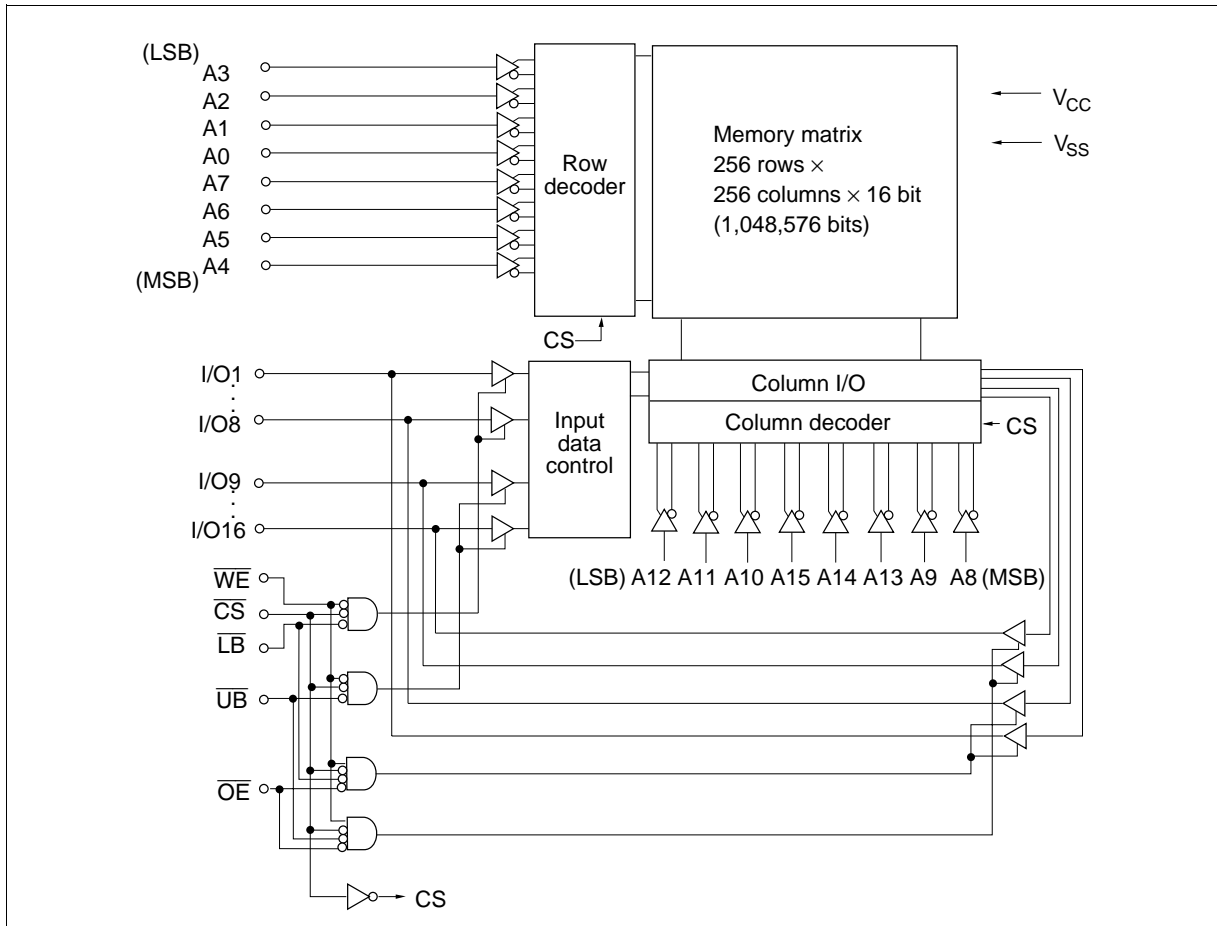


(Top View)

Pin Description

| Pin name | Function |
|-----------------|-------------------|
| A0 – A15 | Address input |
| I/O1 – I/O16 | Data input/output |
| \overline{CS} | Chip select |
| \overline{OE} | Output enable |
| \overline{WE} | Write enable |
| \overline{UB} | Upper byte select |
| \overline{LB} | Lower byte select |
| V _{CC} | Power supply |
| V _{SS} | Ground |
| NC | No connection |

Block Diagram



Function Table

| \overline{CS} | \overline{OE} | \overline{WE} | \overline{LB} | \overline{UB} | Mode | V _{CC} current | I/O1-I/O8 | I/O9-I/O16 | Ref. cycle |
|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------------------------|-----------|------------|-------------|
| H | x | x | x | x | Standby | I _{SB} , I _{SB1} | High-Z | High-Z | — |
| L | H | H | x | x | Output disable | I _{CC} | High-Z | High-Z | — |
| L | L | H | L | L | Read | I _{CC} | Output | Output | Read cycle |
| L | L | H | L | H | Lower byte read | I _{CC} | Output | High-Z | Read cycle |
| L | L | H | H | L | Upper byte read | I _{CC} | High-Z | Output | Read cycle |
| L | L | H | H | H | — | I _{CC} | High-Z | High-Z | — |
| L | x | L | L | L | Write | I _{CC} | Input | Input | Write cycle |
| L | x | L | L | H | Lower byte write | I _{CC} | Input | High-Z | Write cycle |
| L | x | L | H | L | Upper byte write | I _{CC} | High-Z | Input | Write cycle |
| L | x | L | H | H | — | I _{CC} | High-Z | High-Z | — |

Note: x: H or L

Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|------------|--------------------------------------|------|
| Supply voltage relative to V_{SS} | V_{CC} | -0.5 to +4.6 | V |
| Voltage on any pin relative to V_{SS} | V_T | -0.5* ¹ to $V_{CC} + 0.5$ | V |
| Power dissipation | P_T | 1.0 | W |
| Operating temperature | T_{opr} | 0 to +70 | °C |
| Storage temperature | T_{stg} | -55 to +125 | °C |
| Storage temperature under bias | T_{bias} | -10 to +85 | °C |

Notes: 1. V_T (min) = -2.5 V for pulse width (under shoot) ≤ 10 ns

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

| Parameter | Symbol | Min | Typ | Max | Unit |
|----------------|-------------------------|--------------------|-----|----------------|------|
| Supply voltage | V_{CC} * ² | 3.0 | 3.3 | 3.6 | V |
| | V_{SS} * ³ | 0 | 0 | 0 | V |
| Input voltage | V_{IH} | 2.0 | — | $V_{CC} + 0.3$ | V |
| | V_{IL} | -0.3* ¹ | — | 0.8 | V |

Notes: 1. -2.0 V for pulse width (under shoot) ≤ 10 ns

2. The supply voltage with all V_{CC} pins must be on the same level.

3. The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{SS} = 0 \text{ V}$)

| Parameter | | Symbol | Min | Typ* ¹ | Max | Unit | Test conditions |
|--------------------------------------|-------------|-----------------|-----------------|--------------------|-----|---------------|--|
| Input leakage current | | $ I_{LI} $ | — | — | 2 | μA | $V_{in} = V_{SS}$ to V_{CC} |
| Output leakage current* ¹ | | $ I_{LO} $ | — | — | 2 | μA | $V_{in} = V_{SS}$ to V_{CC} |
| Operating power supply current | 25 ns cycle | I_{CC} | — | — | 100 | mA | $\overline{CS} = V_{IL}$, $I_{out} = 0 \text{ mA}$ Other inputs = V_{IH}/V_{IL} |
| | 30 ns cycle | I_{CC} | — | — | 90 | | |
| Standby power supply current | 25 ns cycle | I_{SB} | — | — | 40 | mA | $\overline{CS} = V_{IH}$, Other inputs = V_{IH}/V_{IL} |
| | 30 ns cycle | I_{SB} | — | — | 35 | | |
| | | I_{SB1} | — | — | 1 | mA | $V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2 \text{ V}$, (1) $0 \text{ V} \leq V_{in} \leq 0.2 \text{ V}$ or (2) $V_{CC} \geq V_{in} \geq V_{CC} - 0.2 \text{ V}$ |
| | | —* ² | —* ² | 0.15* ² | | | |
| Output voltage | | V_{OL} | — | — | 0.2 | V | $I_{OL} = 0.1 \text{ mA}$ |
| | | | — | — | 0.4 | V | $I_{OL} = 2 \text{ mA}$ |
| | | V_{OH} | $V_{CC} - 0.2$ | — | — | V | $I_{OH} = -0.1 \text{ mA}$ |
| | | | 2.4 | — | — | V | $I_{OH} = -2 \text{ mA}$ |

- Note: 1. Typical values are at $V_{CC} = 3.3 \text{ V}$, $T_a = +25^\circ\text{C}$ and not guaranteed.
2. This characteristics is guaranteed only for L-version.

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1.0 \text{ MHz}$)

| Parameter | | Symbol | Min | Typ | Max | Unit | Test conditions |
|--|--|-----------|-----|-----|-----|------|-------------------------|
| Input capacitance* ¹ | | C_{in} | — | — | 6 | pF | $V_{in} = 0 \text{ V}$ |
| Input/output capacitance* ¹ | | $C_{I/O}$ | — | — | 8 | pF | $V_{I/O} = 0 \text{ V}$ |

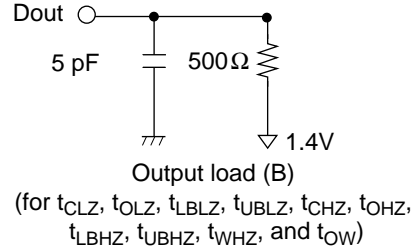
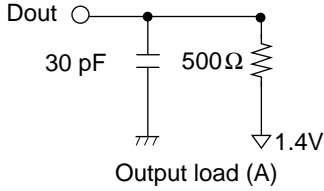
- Note: 1. This parameter is sampled and not 100% tested.

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AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, unless otherwise noted.)

Test Conditions

- Input pulse levels: 2.4 V/0.4 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.4 V
- Output load: See figures (Including scope and jig)



Read Cycle

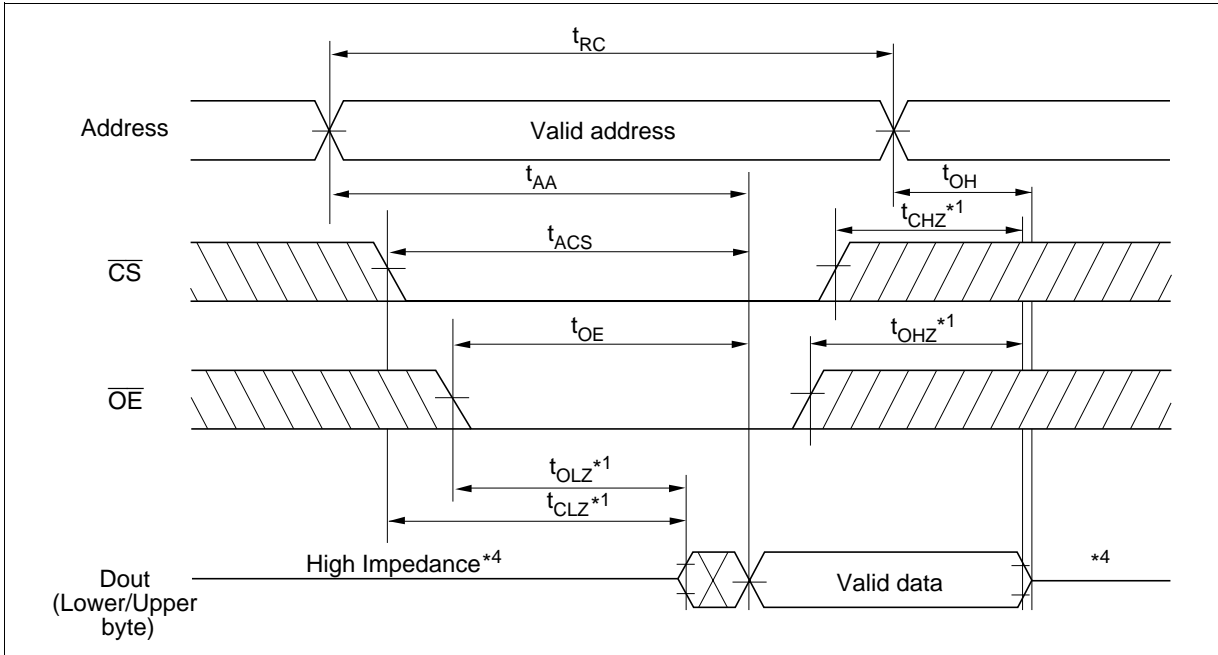
| Parameter | Symbol | HM62W1664HB -25 HM62W1664HB -30 | | | | Unit | Notes |
|------------------------------------|-------------------------|---------------------------------|-----|-----|-----|------|-------|
| | | Min | Max | Min | Max | | |
| Read cycle time | t_{RC} | 25 | — | 30 | — | ns | |
| Address access time | t_{AA} | — | 25 | — | 30 | ns | |
| Chip select access time | t_{ACS} | — | 25 | — | 30 | ns | |
| Output enable to output valid | t_{OE} | — | 15 | — | 15 | ns | |
| Byte select to output valid | t_{LB} , t_{UB} | — | 15 | — | 15 | ns | |
| Output hold from address change | t_{OH} | 5 | — | 5 | — | ns | |
| Chip select to output in low-Z | t_{CLZ} | 5 | — | 5 | — | ns | 1 |
| Output enable to output in low-Z | t_{OLZ} | 1 | — | 1 | — | ns | 1 |
| Byte select to output in low-Z | t_{LBLZ} , t_{UBLZ} | 1 | — | 1 | — | ns | 1 |
| Chip deselect to output in high-Z | t_{CHZ} | — | 12 | — | 12 | ns | 1 |
| Output disable to output in high-Z | t_{OHZ} | — | 12 | — | 12 | ns | 1 |
| Byte deselect to output in high-Z | t_{LBHZ} , t_{UBHZ} | — | 12 | — | 12 | ns | 1 |

Write Cycle

| Parameter | Symbol | HM62W1664HB -25 | | HM62W1664HB -30 | | Unit | Notes |
|------------------------------------|--------------------|-----------------|-----|-----------------|-----|------|-------|
| | | Min | Max | Min | Max | | |
| Write cycle time | t_{WC} | 25 | — | 30 | — | ns | |
| Address valid to end of write | t_{AW} | 20 | — | 20 | — | ns | |
| Chip select to end of write | t_{CW} | 20 | — | 20 | — | ns | 8 |
| Write pulse width | t_{WP} | 20 | — | 20 | — | ns | 7 |
| Byte select to end of write | t_{LBW}, t_{UBW} | 20 | — | 20 | — | ns | 9, 10 |
| Address setup time | t_{AS} | 0 | — | 0 | — | ns | 5 |
| Write recovery time | t_{WR} | 0 | — | 0 | — | ns | 6 |
| Data to write time overlap | t_{DW} | 15 | — | 15 | — | ns | |
| Data hold from write time | t_{DH} | 0 | — | 0 | — | ns | |
| Write disable to output in low-Z | t_{OW} | 5 | — | 5 | — | ns | 1 |
| Output disable to output in high-Z | t_{OHZ} | — | 12 | — | 12 | ns | 1 |
| Write enable to output in high-Z | t_{WHZ} | — | 12 | — | 12 | ns | 1 |

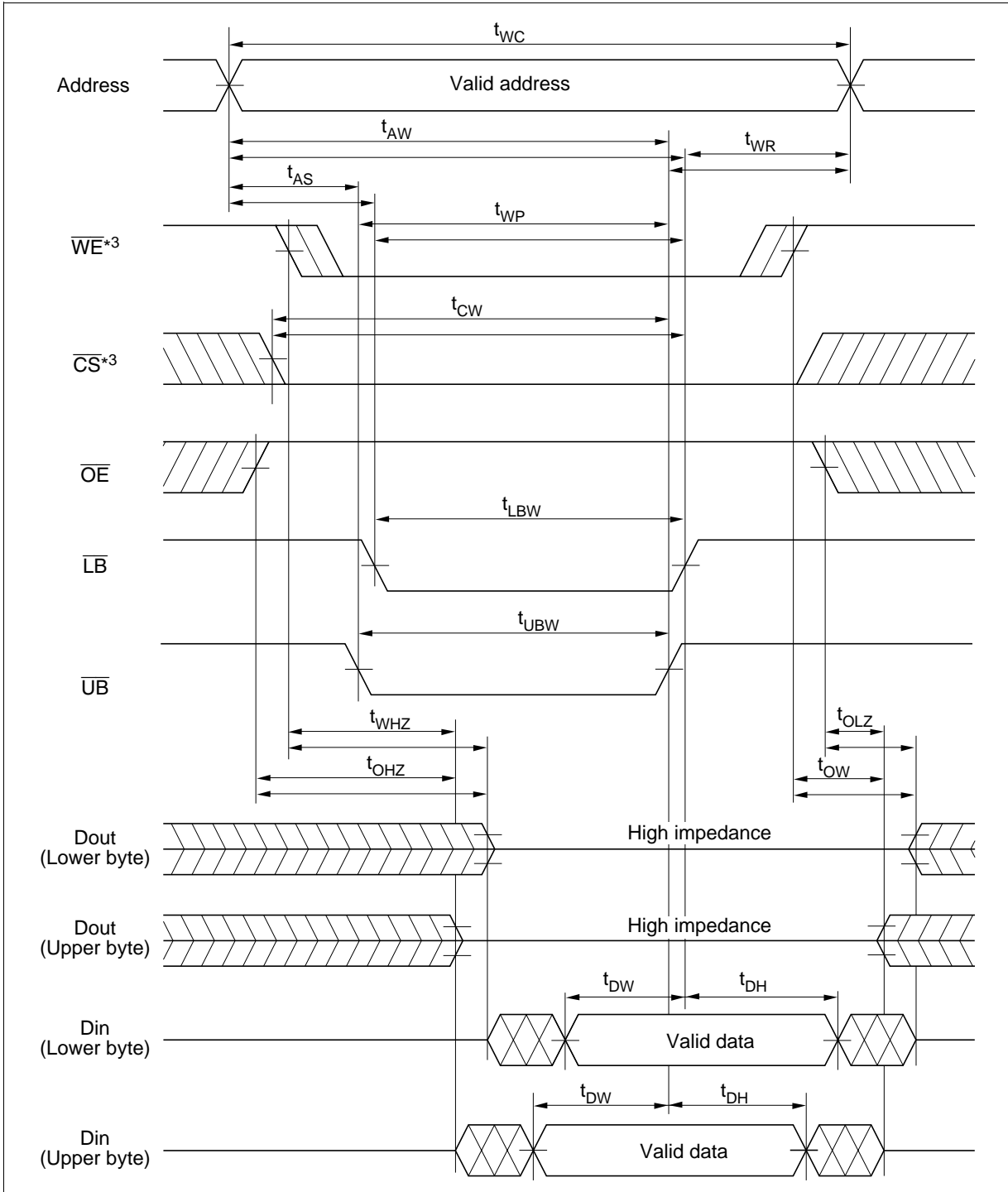
- Notes:
1. Transition is measured ± 200 mV from steady voltage with Load (B). This parameter is sampled and not 100% tested.
 2. If the \overline{CS} or \overline{LB} or \overline{UB} low transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} transition, output remains a high impedance state.
 3. \overline{WE} and/or \overline{CS} must be high during address transition time.
 4. If \overline{CS} , \overline{OE} , \overline{LB} and \overline{UB} are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
 5. t_{AS} is measured from the latest address transition to the latest of \overline{CS} , \overline{WE} , \overline{LB} or \overline{UB} going low.
 6. t_{WR} is measured from the earliest of \overline{CS} , \overline{WE} , \overline{LB} or \overline{UB} going high to the first address transition.
 7. A write occurs during the overlap of low \overline{CS} , low \overline{WE} and low \overline{LB} or low \overline{UB} .
 8. t_{CW} is measured from the later of \overline{CS} going low to the end of write.
 9. t_{LBW} is measured from the later of \overline{LB} going low to the end of write.
 10. t_{UBW} is measured from the later of \overline{UB} going low to the end of write.

Read Timing Waveform (2) ($\overline{WE} = V_{IH}$, $\overline{LB} = V_{IL}$, $\overline{UB} = V_{IL}$)

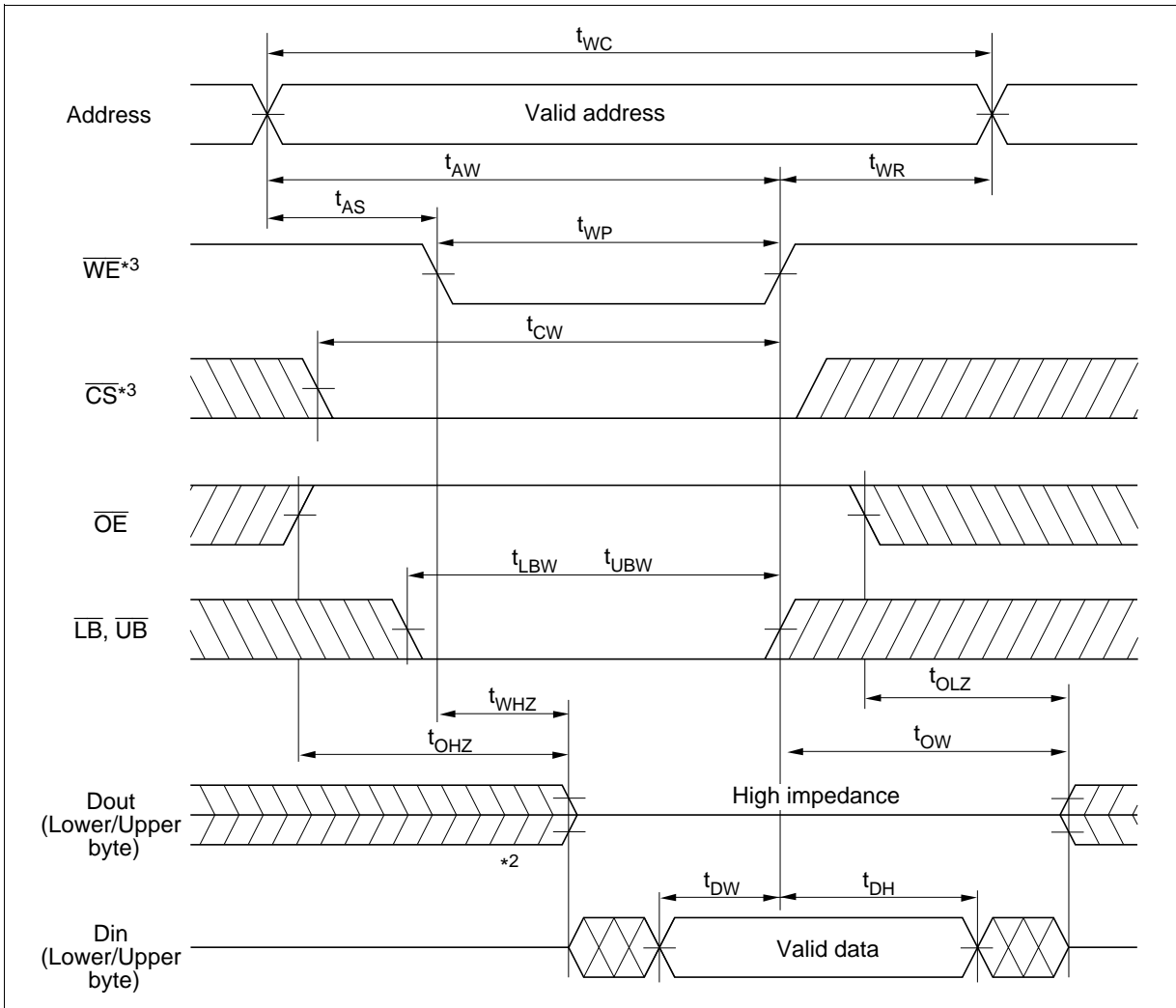


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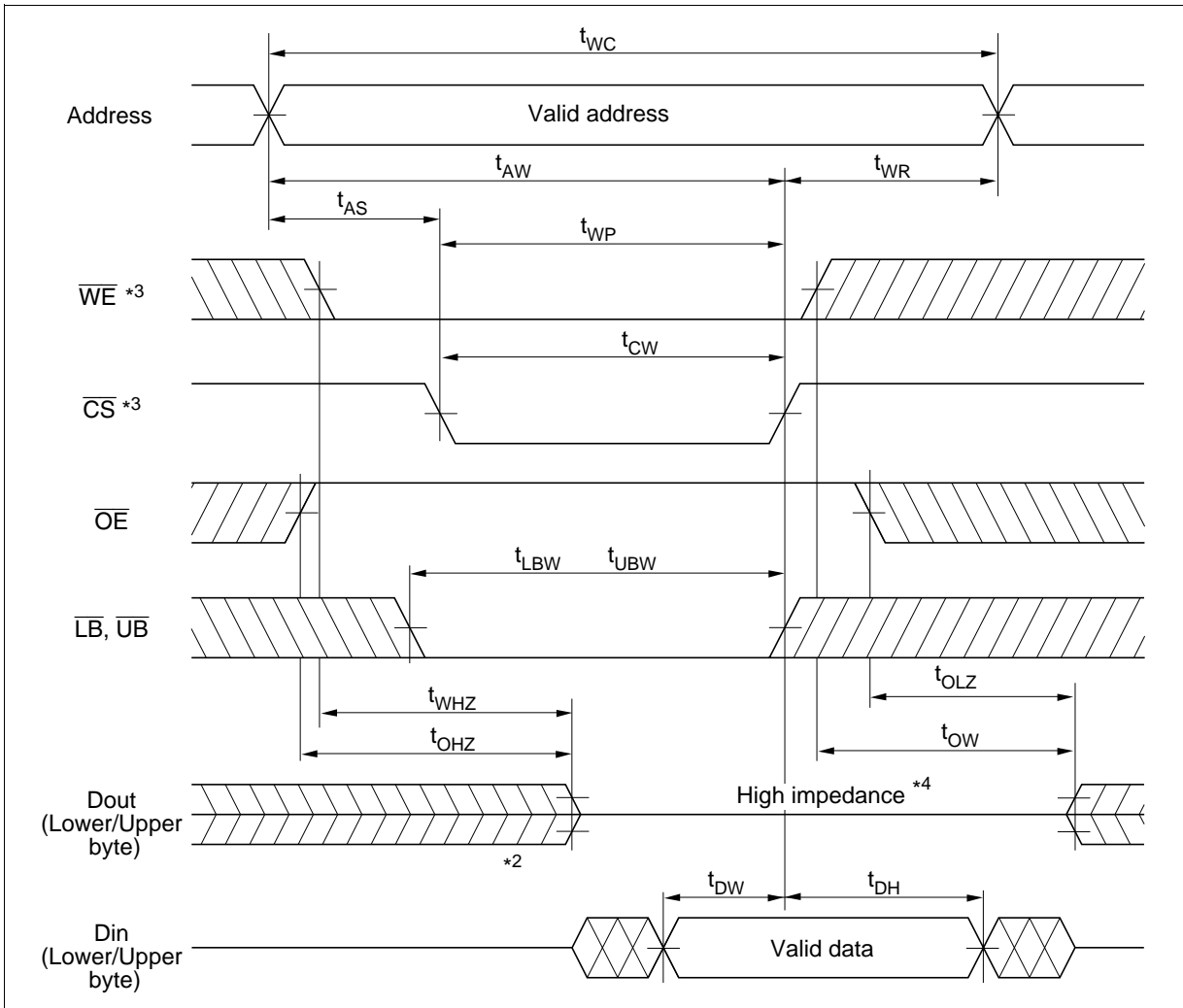
Write Timing Waveform (1) ($\overline{\text{LB}}$, $\overline{\text{UB}}$ Controlled)



Write Timing Waveform (2) (\overline{WE} Controlled)



Write Timing Waveform (3) (\overline{CS} Controlled)



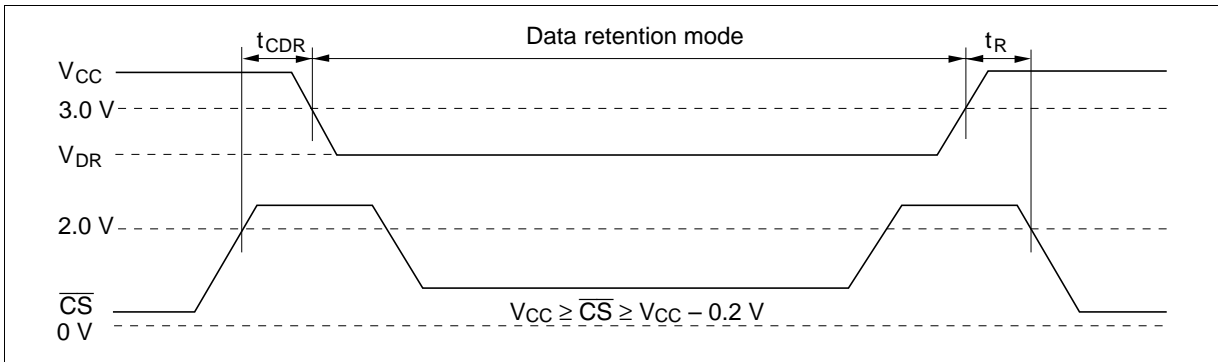
Low V_{CC} Data Retention Characteristics ($T_a = 0$ to $+70^\circ\text{C}$)

This characteristics is guaranteed only for L-version.

| Parameter | Symbol | Min | Typ*1 | Max | Unit | Test conditions |
|--------------------------------------|------------|-----|-------|-----|---------------|---|
| V_{CC} for data retention | V_{DR} | 2.0 | — | — | V | $V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2$ V, (1) $0 \text{ V} \leq V_{in} \leq 0.2 \text{ V}$ or (2) $V_{CC} \geq V_{in} \geq V_{CC} - 0.2 \text{ V}$ |
| Data retention current | I_{CCDR} | — | 2 | 80 | μA | $V_{CC} = 3 \text{ V}$ $V_{CC} \geq \overline{CS} \geq V_{CC} - 0.2$ V, (1) $0 \text{ V} \leq V_{in} \leq 0.2 \text{ V}$ or (2) $V_{CC} \geq V_{in} \geq V_{CC} - 0.2 \text{ V}$ |
| Chip deselect to data retention time | t_{CDR} | 0 | — | — | ns | See retention waveform |
| Operation recovery time | t_R | 5 | — | — | ms | |

Note: 1. Typical values are at $V_{CC} = 3.0 \text{ V}$, $T_a = 25^\circ\text{C}$, and not guaranteed.

Low V_{CC} Data Retention Timing Waveform

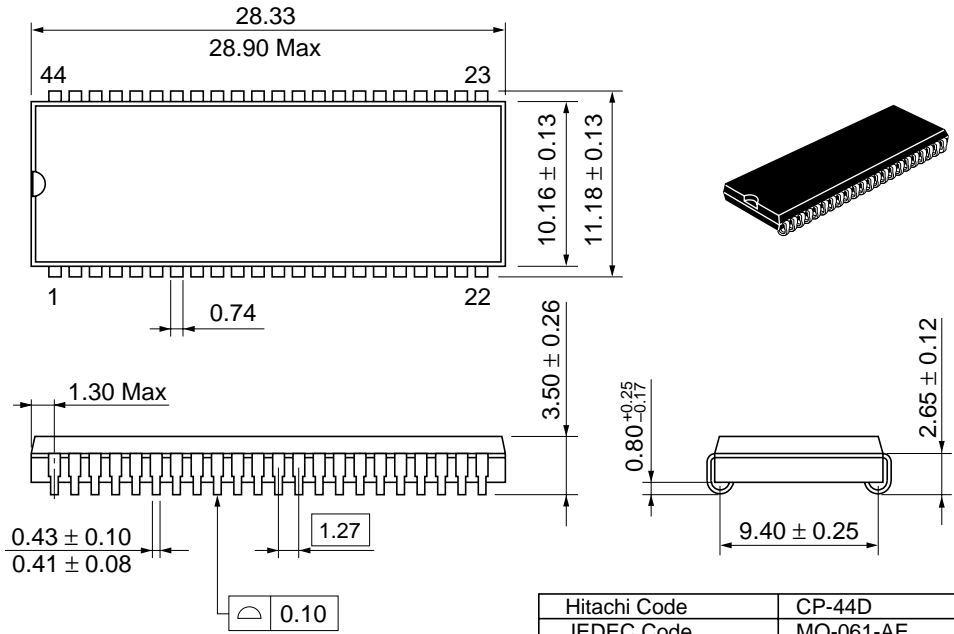


HM62W1664HB Series

Package Dimensions

HM62W1664HBJP/HBLJP Series (CP-44D)

Unit: mm



| | |
|--------------|-----------|
| Hitachi Code | CP-44D |
| JEDEC Code | MO-061-AE |
| EIAJ Code | — |
| Weight | 1.8 g |

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Revision Record

| Rev. | Date | Contents of Modification | Drawn by | Approved by |
|------|---------------|--|-----------|--------------|
| 0.0 | Aug. 3, 1995 | Initial issue | T. Nojiri | K. Yoshizaki |
| 0.1 | Jul. 18, 1996 | Change of format Change of Block Diagram Function Table Addition of Mode Parameter Recommended DC Operating Conditions Change of note 2. Addition of note 3. DC Characteristics Addition of note 2 AC Characteristics Change order of notes t_{OE} (max) : 12/15 ns to 15/15 ns t_{AW} (min) : 15/20 ns to 20/20 ns t_{CW} (min) : 15/20 ns to 20/20 ns t_{WP} (min) : 15/20 ns to 20/20 ns t_{LBW}, t_{UBW} (min) : 15/20 ns to 20/20 ns t_{DW} (min) : 12/15 ns to 15/15 ns t_{WHZ} (max) : 10/10 ns to 12/12 ns Addition of t_{OE} (Write Cycle) Change of Timing Waveform Addition of Read Timing Waveform (2) | Y. Saito | A. Ide |
| 1.0 | Dec. 25, 1996 | Deletion of Preliminary | | |