DATA SHEET

CBT3126
Quadruple FET bus switch

Product data

2001 Dec 12

File under Integrated Circuits — ICL03

Philips
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Quadruple FET bus switch CBT3126

DESCRIPTION

The CBT3126 quadruple FET bus switch features independent line switches. Each switch is disabled when the associated Output Enable (OE) input is LOW.

FEATURES

- Standard ’126-type pinout (D, DB, and PW packages)
- 5 Ω switch connection between two ports
- TTL-compatible input levels
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 500 mA
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101

PIN CONFIGURATION

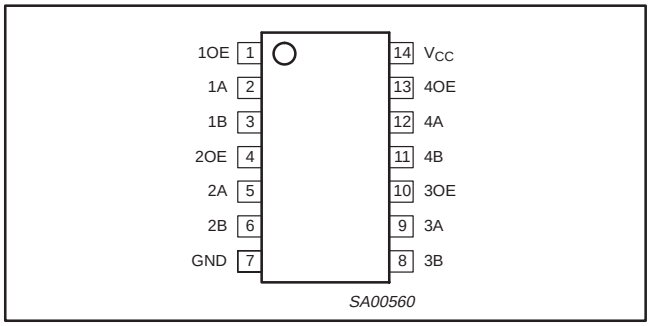
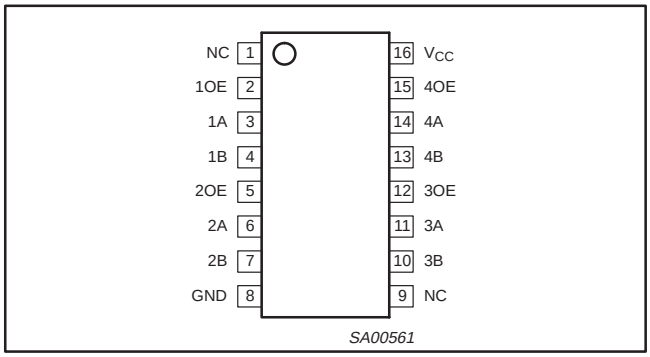


Figure 1. SO14, SSOP14, and TSSOP14



NC = no internal connection

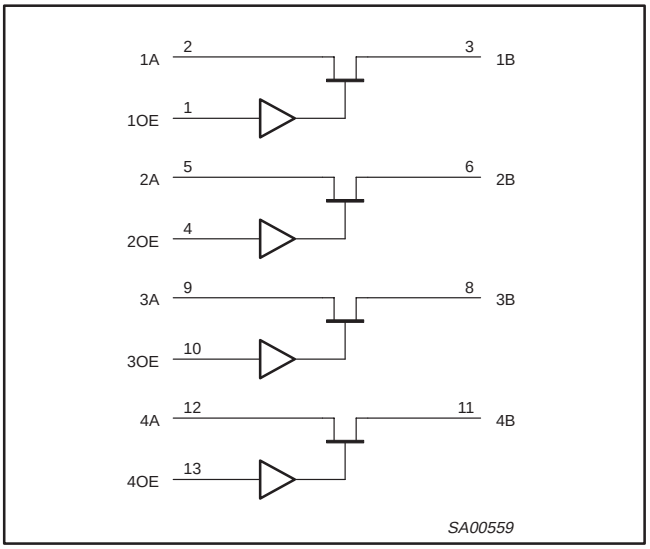
Figure 2. SSOP(QSOP)16

ORDERING INFORMATION

PACKAGE	TEMPERATURE RANGE	ORDER CODE	PACKAGE DWG. #
14-Pin Plastic SO	–40 to +85 °C	CBT3126D	SOT108-1
14-Pin Plastic SSOP	–40 to +85 °C	CBT3126DB	SOT337-1
16-Pin Plastic SSOP(QSOP)	–40 to +85 °C	CBT3126DS	SOT519-1
14-Pin Plastic TSSOP	–40 to +85 °C	CBT3126PW	SOT402-1

Standard packing quantities and other packaging data is available at www.philipslogic.com/packaging.

LOGIC DIAGRAM



Pin numbers shown are for 14-pin package-types.

Figure 3. CBT3126 logic diagram (positive logic)

FUNCTION TABLE (each bus switch)

INPUT OE	FUNCTION
L	disconnect
H	A = B

ABSOLUTE MAXIMUM RATINGS[1]

Over operating free-air temperature range, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage range		–0.5	7	V
V_I	input voltage range	see Note 2	–0.5	7	V
	continuous channel current		—	128	mA
I_K	input clamp current	$V_{I/O} < 0$	—	–50	mA
T_{stg}	storage temperature range		–65	+150	°C

NOTES:

1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS[1]

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		4.5	5.5	V
V_{IH}	high-level control input voltage		2		V
V_{IL}	low-level control input voltage		—	0.8	V
T_{amb}	operating ambient temperature in free-air		–40	+85	°C

NOTE:

1. All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range, unless otherwise noted.

SYMBOL	PARAMETER		CONDITIONS	MIN.	TYP.[1]	MAX.	UNIT
V_{IK}	Input clamp voltage		V_{CC} = 4.5 V; I_I = –18 mA	—	—	–1.2	V
I_I	Input leakage current		V_{CC} = 5.5 V; V_I = 5.5 V or GND	—	—	±1	μA
I_{CC}	Quiescent supply current		V_{CC} = 5.5 V; I_O = 0; V_I = V_{CC} or GND	—	—	3	μA
ΔI_{CC}	Additional supply current per input pin (Note 2)	control inputs	V_{CC} = 5.5 V; one input at 3.4 V, other inputs at V_{CC} or GND	—	—	2.5	mA
C_I	Input capacitance	control inputs	V_I = 3 V or 0	—	1.7	—	pF
$C_{IO(OFF)}$	Power-off leakage current		V_O = 3 V or 0; OE = GND	—	3.4	—	pF
V_P	Pass gate voltage		V_{CC} = 5.0 V; V_I = 5.0 V	—	3.8	—	V
r_{on}	On-resistance (Note 3)		V_{CC} = 4 V; TYP at V_{CC} = 4 V; V_I = 2.4 V; I_I = 15 mA	—	16	22	Ω
			V_{CC} = 4.5 V; V_I = 0 V; I_I = 64 mA	—	5	7	Ω
			V_{CC} = 4.5 V; V_I = 0 V; I_I = 30 mA	—	5	7	Ω
			V_{CC} = 4.5 V; V_I = 2.4 V; I_I = 15 mA	—	10	15	Ω

NOTES:

1. All typical values are at V_{CC} = 5 V, unless otherwise noted. T_{amb} = 25 °C.
2. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
3. Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

AC CHARACTERISTICS

T_{amb} = –40 to +85 °C; C_L = 50 pF, unless otherwise noted.

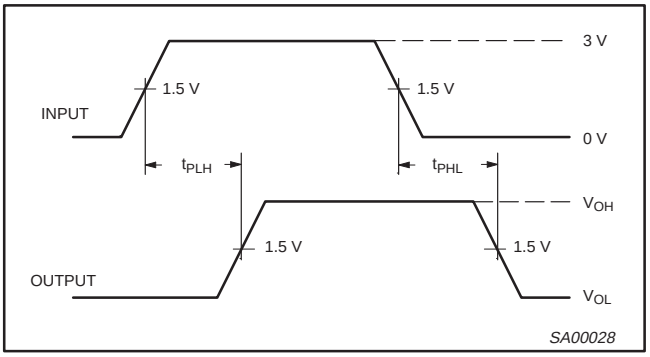
SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V ± 0.5 V		UNIT
				Min	Max	
t_{pd}	Propagation delay[1]	A or B	B or A		0.25	ns
t_{en}	Output enable time to High and Low level	OE	A or B	1.6	4.5	ns
t_{dis}	Output disable time from High and Low level	OE	A or B	1	4.0	ns

NOTE:

1. This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

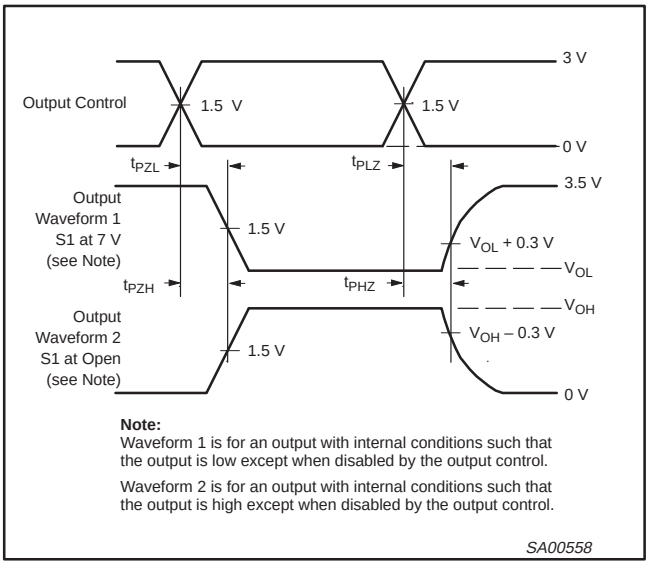
AC WAVEFORMS

V_M = 1.5 V, V_{IN} = GND to 3.0V



t_{PLH} and t_{PHL} are the same as t_{pd}.

Waveform 1. Input to Output Propagation Delays

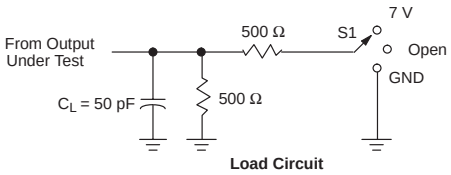


t_{PLZ} and t_{PHZ} are the same as t_{dis}.

t_{PZL} and t_{PZH} are the same as t_{en}.

Waveform 2. Output Enable and Disable Times

TEST CIRCUIT



TEST	S1
t_{pd}	open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	open

DEFINITIONS

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

SA00012

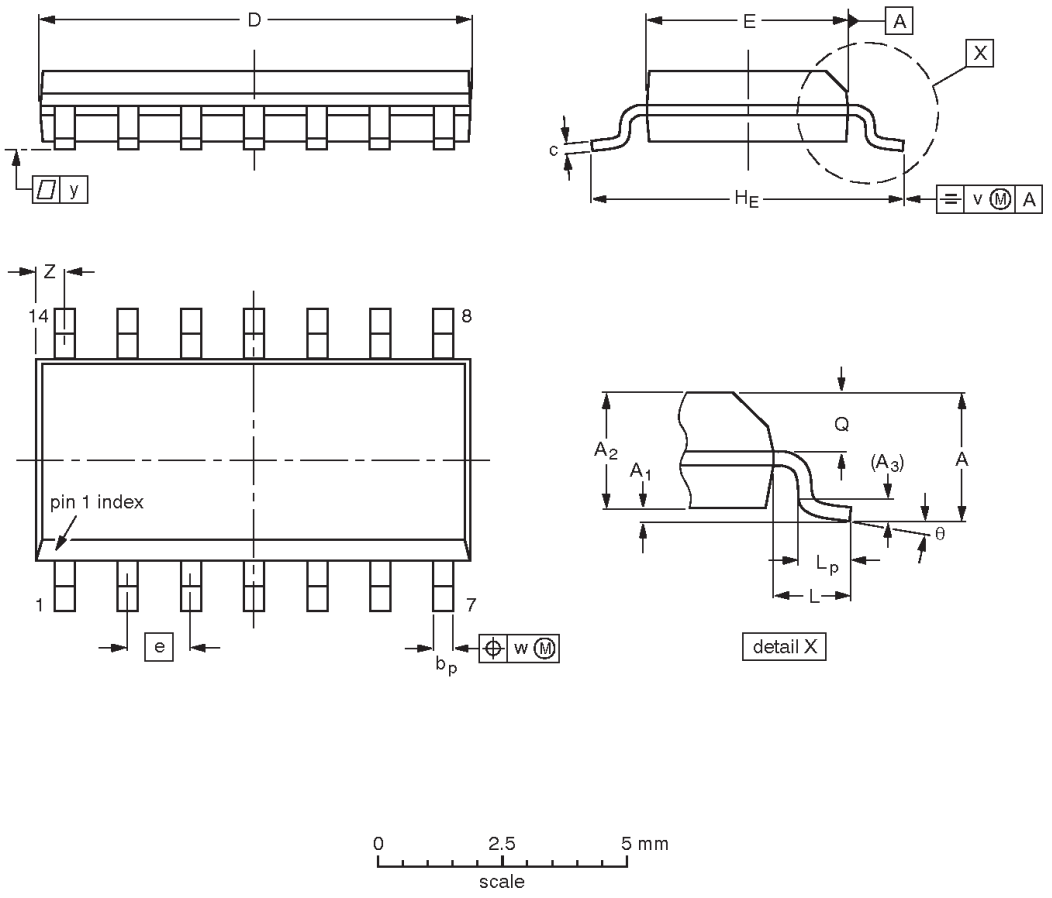
t_{PLZ} and t_{PHZ} are the same as t_{dis}.

t_{PZL} and t_{PZH} are the same as t_{en}.

NOTES:

1. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
2. The outputs are measured one at a time with one transition per measurement.

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

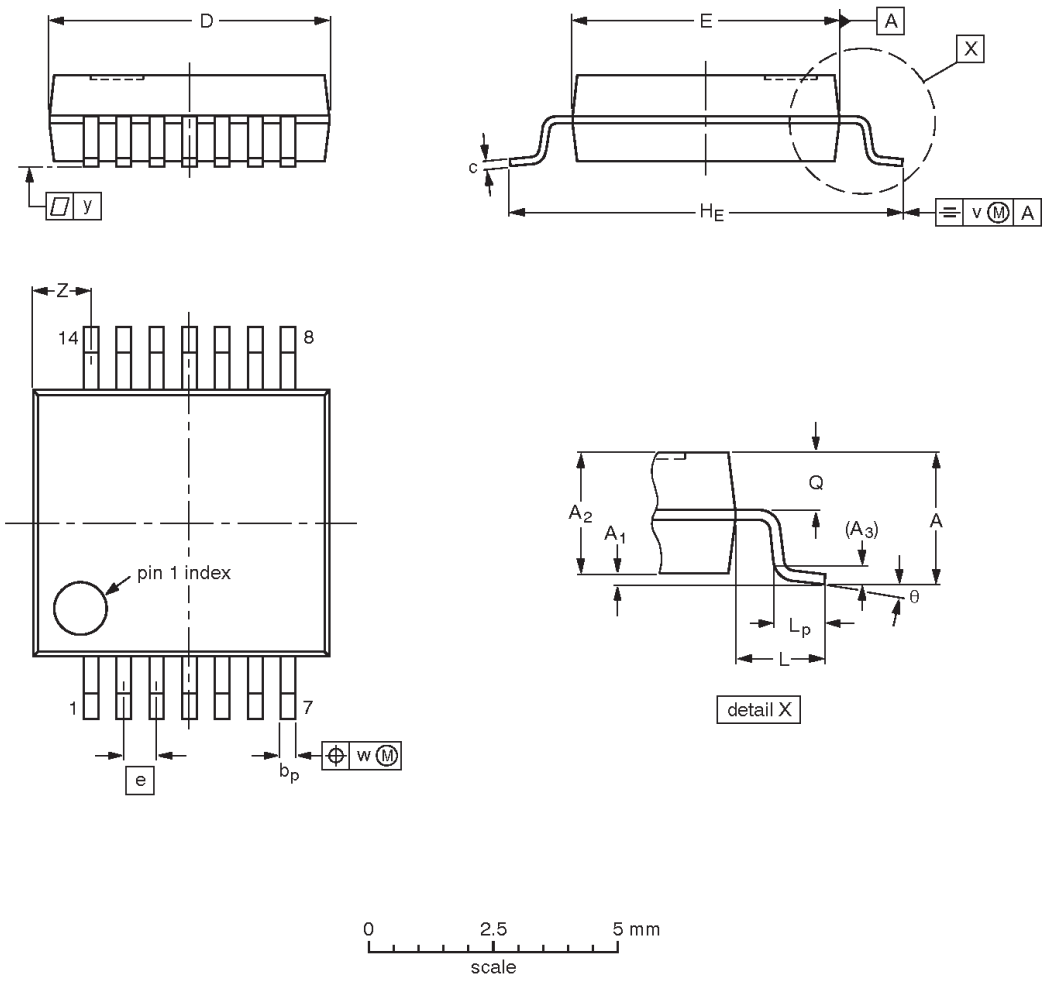
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06	MS-012				~~97-05-22~~ 99-12-27

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

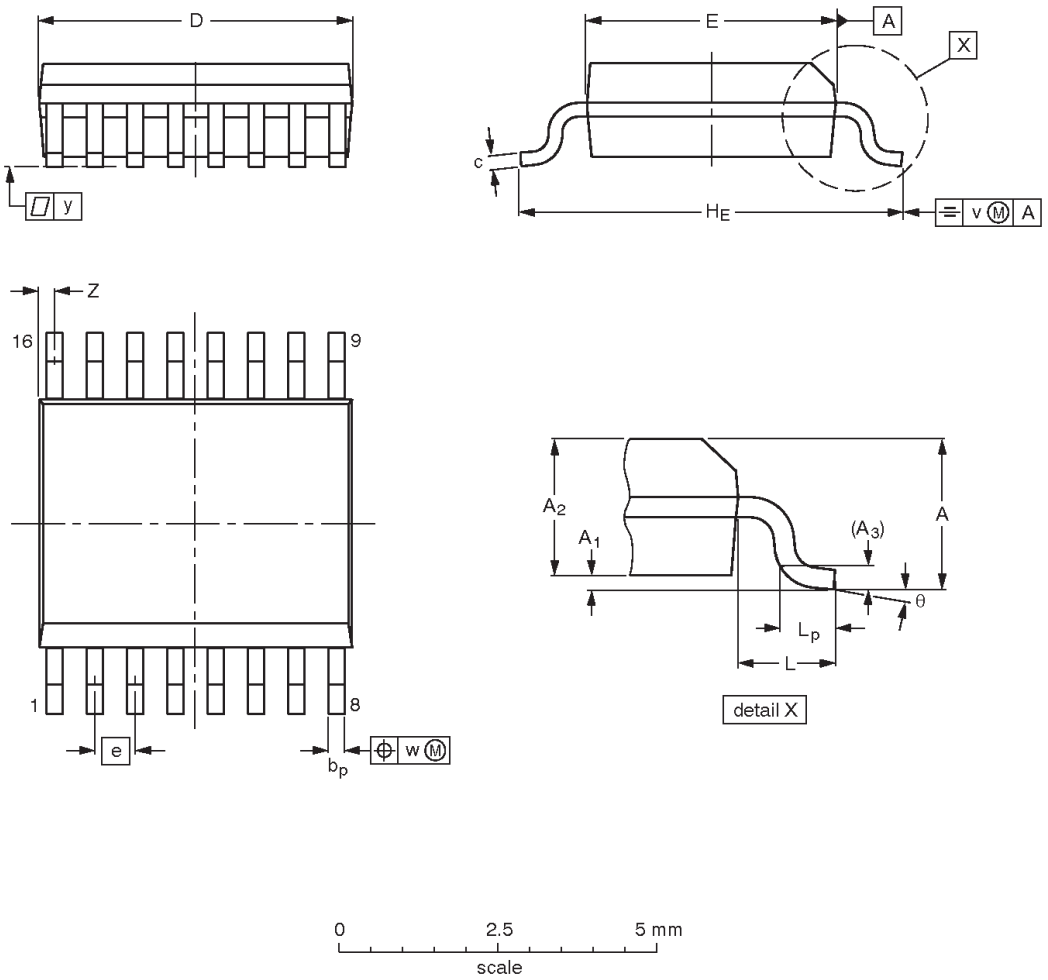
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150				~~96-01-18~~ 99-12-27

SSOP16: plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm **SOT519-1**



DIMENSIONS (mm are the original dimensions)

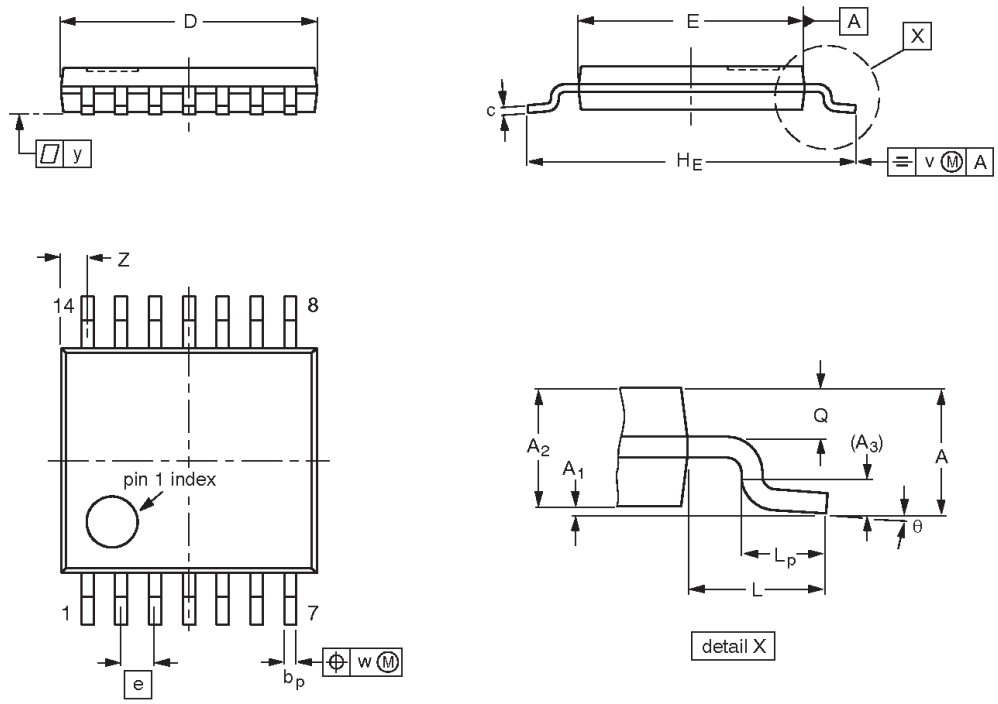
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	v	w	y	Z (1)	θ
mm	1.73	0.25 0.10	1.55 1.40	0.25	0.31 0.20	0.25 0.18	5.0 4.8	4.0 3.8	0.635	6.2 5.8	1.0	0.89 0.41	0.2	0.18	0.09	0.18 0.05	8^o 0^o

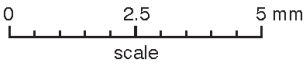
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT519-1						99-05-04

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				~~95-04-04~~ 99-12-27

Data sheet status

Data sheet status [1]	Product status [2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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Date of release: 12-01

Document order number: 9397 750 09219

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