TEA1532(A)P; TEA1532(A)T

GreenChip™II SMPS control IC

Rev. 02 — 4 February 2005 Product data sheet

1. General description

The GreenChip™II is the second generation of green Switched Mode Power Supply (SMPS) controller ICs. Its high level of integration allows the design of a cost effective power supply with a very low number of external components.

The TEA1532(A)P; TEA1532(A)T can also be used in fixed frequency, Continuous Conduction Mode (CCM) converter designs for low voltage, high current applications. At low power (standby) levels, the system operates in cycle skipping mode which minimizes the switching losses during standby.

The special built-in green functions allow the efficiency to be optimum at all power levels. This holds for quasi-resonant operation at high power levels, as well as fixed frequency operation with valley switching at medium power levels. At low power (standby) levels, the system operates in cycle skipping mode with valley detection.

The proprietary high voltage BCD800 process makes direct start-up possible from the rectified universal mains voltage in an effective and green way. A second low voltage BICMOS IC is used for accurate, high speed protection functions and control.

The TEA1532(A)P; TEA1532(A)T enables highly efficient and reliable supplies to be designed easily.

2. Features

2.1 Distinctive features

- Universal mains supply operation (70 V to 276 V AC)
- High level of integration, resulting in a very low external component count
- Fixed frequency Continuous Conduction Mode (CCM) operation capability
- Quasi-Resonant (QR) Discontinuous Conduction Mode (DCM) operation capability.

2.2 Green features

- Valley or zero voltage switching for minimum switching losses in QR operation
- Cycle skipping mode at very low loads; input power < 300 mW at no-load operation for a typical adapter application
- On-chip start-up current source.

2.3 Protection features

- Safe restart mode for system fault conditions
- Zero current switch-on in QR mode

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- Undervoltage protection (foldback during overload)
- IC OverTemperature Protection (OTP) (latched)
- Low and adjustable OverCurrent Protection (OCP) trip level
- Soft (re)start
- Mains voltage-dependent operation-enabling level
- TEA1532AP and TEA1532AT: General purpose input for latched or safe restart protection and timing, e.g. to be used for overvoltage protection (OVP), output short-circuit protection or system OTP.
- TEA1532P and TEA1532T: General purpose input for latched protection and timing, e.g. to be used for OVP, output short-circuit protection or system OTP.
- Brown-out protection.

3. Applications

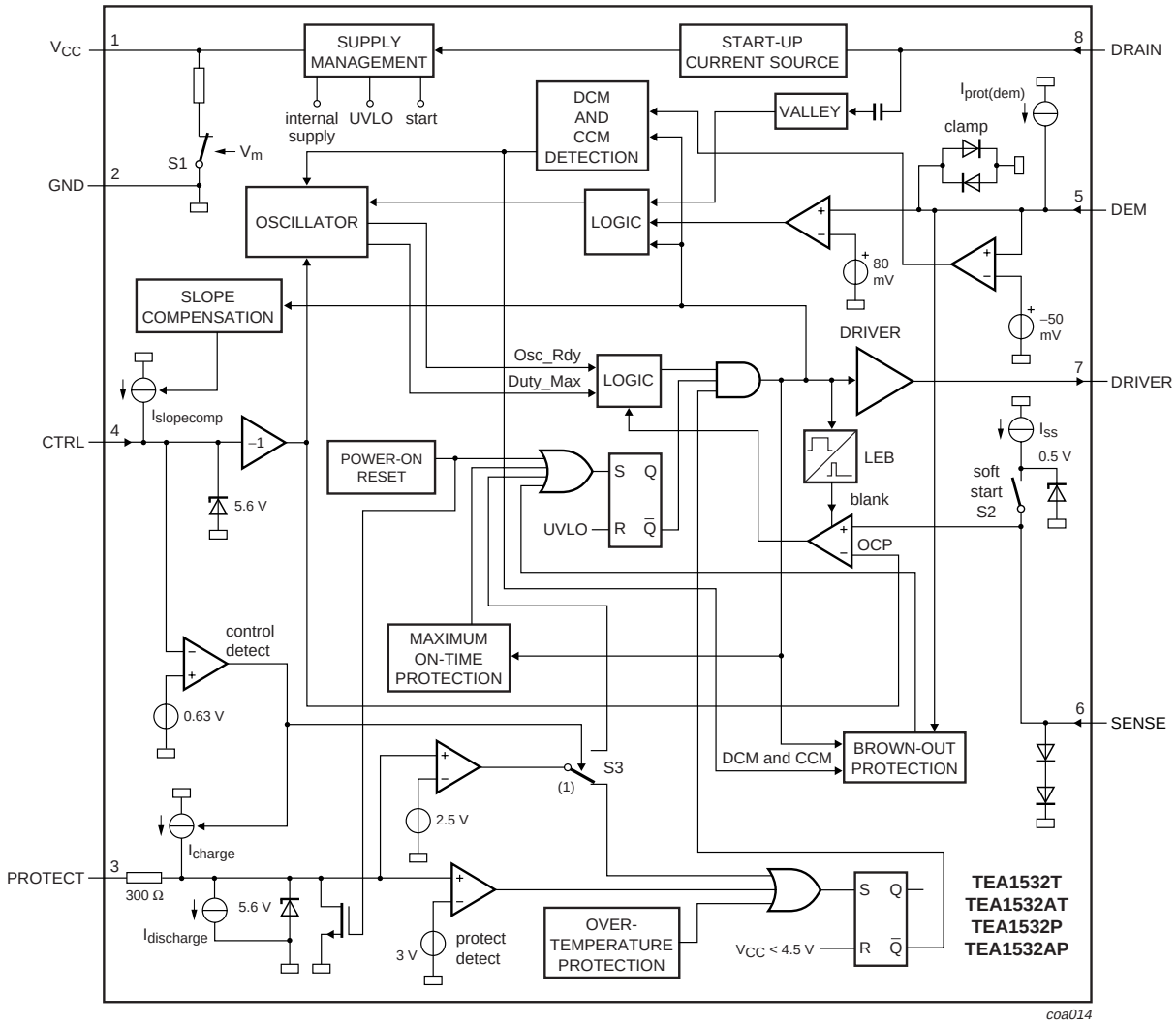
- Printer adapters and chargers. The device can also be used in all applications that demand an efficient and cost-effective solution up to 250 W.

4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
TEA1532T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TEA1532AT			
TEA1532P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
TEA1532AP			

5. Block diagram



(1) Switch S3 is not controlled in the TEA1532T and TEA1532P (fixed as drawn).

Fig 1. Block diagram

6. Pinning information

6.1 Pinning

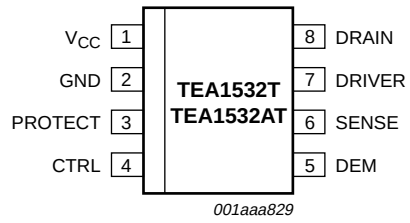


Fig 2. Pin configuration: TEA1532(A)T (SOT96-1)

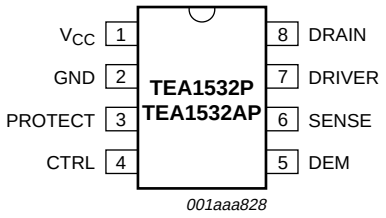


Fig 3. Pin configuration: TEA1532(A)P (SOT97-1)

6.2 Pin description

Table 2: Pin description

Symbol	Pin	Description
V_{CC}	1	supply voltage
GND	2	ground
PROTECT	3	protection and timing input
CTRL	4	control input
DEM	5	input from auxiliary winding for demagnetization timing
SENSE	6	programmable current sense input
DRIVER	7	MOSFET gate driver output
DRAIN	8	drain of the external MOS switch, input for start-up current and valley sensing

7. Functional description

The TEA1532(A)P; TEA1532(A)T is the controller of a compact flyback converter, with the IC situated at the primary side. An auxiliary winding of the transformer provides demagnetization detection and powers the IC after start-up; see Figure 4.

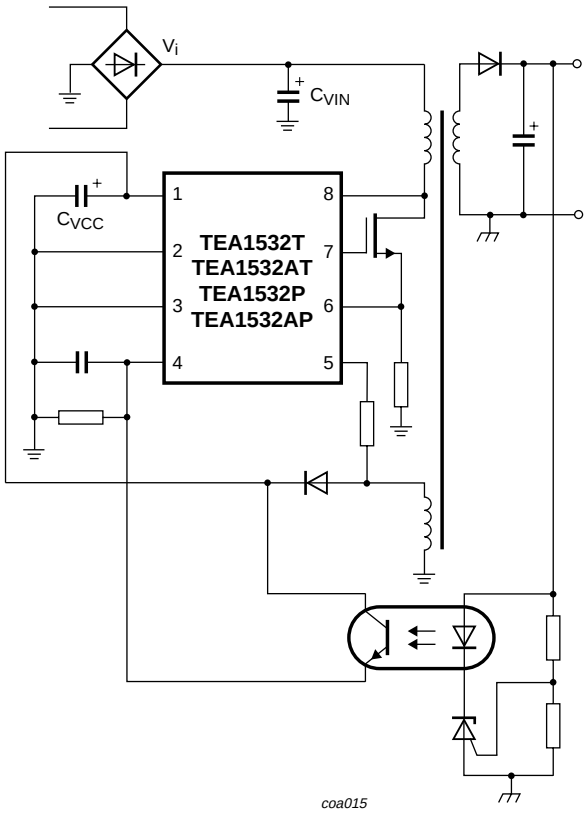


Fig 4. Typical configuration

The TEA1532(A)P; TEA1532(A)T can operate in multi modes; see Figure 5.

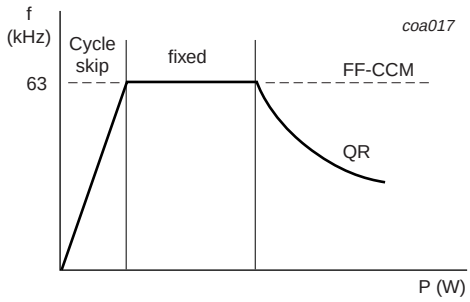


Fig 5. Multi mode and FF-CCM operation

In QR mode, the next converter stroke is started only after demagnetization of the transformer current (zero current switching), while the drain voltage has reached the lowest voltage to minimize switching losses (green function). The primary resonant circuit of primary inductance and drain capacitor ensures this quasi-resonant operation. The design can be optimized in such a way that zero voltage switching can extend over most of the universal mains range.

To prevent very high frequency operation at lower loads, the quasi-resonant operation changes smoothly in fixed frequency Pulse Width Modulation (PWM) control.

In fixed frequency continuous conduction mode, which can be activated by grounding pin DEM, the internal oscillator determines the start of the next converter stroke.

In both operating modes, a cycle skipping mode is activated at very low power (standby) levels.

7.1 Start-up, mains enabling operation level and undervoltage lock out

Refer to Figure 10 and Figure 11. Initially, the IC is self supplying from the rectified mains voltage via pin DRAIN. Supply capacitor C_{VCC} (at pin 1) is charged by the internal start-up current source to a level of about 4 V or higher, depending on the drain voltage. Once the drain voltage exceeds the V_m (mains-dependent operation-enabling level), the start-up current source will continue charging capacitor C_{VCC} (switch S1 will be opened); see Figure 1. The IC will activate the power converter as soon as the voltage on pin V_{CC} passes the V_{start} level. At this moment the IC supply from the high voltage pin is stopped (green function). The IC supply is taken over by the auxiliary winding of the flyback converter.

The moment the voltage on pin V_{CC} drops below V_{UVLO} (undervoltage lock out), the IC stops switching and performs a safe restart from the rectified mains voltage. In the safe restart mode the driver output is disabled and pin V_{CC} voltage is recharged via pin DRAIN.

7.2 Supply management

All (internal) reference voltages are derived from a temperature compensated, on-chip band gap circuit.

7.3 Current control mode

Current control mode is used for its good line regulation behavior.

The on-time is controlled by an internal control voltage, which is compared with the primary current information. The primary current is sensed across an external resistor. The driver output is latched in the logic, preventing multiple switch-on.

The internal control voltage is inversely proportional to the external pin CTRL voltage, with an offset of 1.5 V. This means that a voltage range from 1 V to approximately 1.5 V on pin CTRL will result in an internal control voltage range from 0.5 V to 0 V (a high external control voltage results in a low duty cycle).

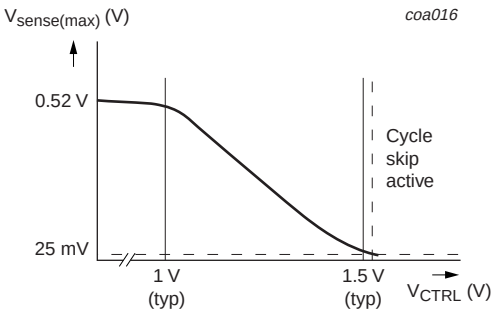


Fig 6. The $V_{sense(max)}$ voltage as a function of V_{CTRL}

7.4 Oscillator

The fixed frequency of the oscillator is set by an internal current source and capacitor.

7.5 Cycle skipping

At very low power levels, a cycle skipping mode activates. An internal control voltage ($V_{sense(max)}$) lower than 25 mV will inhibit switch-on of the external power MOSFET until this voltage increases to a higher value; see Figure 6.

7.6 Demagnetization (QR operation)

The system will be in Discontinuous Conduction Mode (DCM) (QR operation) when resistor R_{DEM} is applied. The oscillator will not start a new primary stroke until the previous secondary stroke has ended.

Demagnetization features a cycle-by-cycle output short-circuit protection which immediately reduces the frequency (longer off-time), thereby reducing the power level.

Demagnetization recognition is suppressed during the first t_{supp} time (typical 1.5 µs). This suppression may be necessary in applications where the transformer has a large leakage inductance and at low output voltages or start-up.

7.7 Continuous Conduction Mode (CCM)

It is also possible to operate the IC in the so-called Fixed Frequency Continuous Conduction Mode (FF CCM). This mode is activated by connecting pin DEM to ground and connecting pin DRAIN to the rectified V_i voltage; see Figure 13.

7.8 OverCurrent Protection (OCP)

The primary current in the transformer is measured accurately by the internal cycle-by-cycle source current limit circuit using the external sense resistor R_{sense}. The accuracy of the current limit circuit allows the transformer core to have a minimum specification for the output power required. The OCP circuit limits the ‘sense’ voltage to an internal level (the primary peak current in the transformer is also limited). The OCP detection is suppressed during the leading edge blanking period, t_{leb} generated by the Leading Edge Blanking (LEB) circuit, to prevent false triggering caused by the switch-on spikes.

7.9 Control pin protection

If pin CTRL becomes open-circuit or is disconnected, a fault condition is assumed and the converter will stop switching immediately. Operation recommences when the fault condition is removed.

7.10 Adjustable slope compensation

A slope compensation function has been added at pin CTRL; see Figure 7. The slope compensation function prevents sub-harmonic oscillation in CCM at duty cycles over 50 %. The CTRL voltage is modulated by sourcing a (non-constant) current out of pin CTRL and by adding externally a series resistor $R_{slopecomp}$. This increases the CTRL voltage proportionally with the on-time, which therefore limits the OCP level. A longer on-time results in a higher CTRL voltage, this increase in CTRL voltage will decrease the

on-time. Slope compensation can be adjusted by changing the value of $R_{slopecomp}$. Slope compensation prevents modulation of the on-time (duty cycle) while operating in FF CCM. A possible drawback of sub-harmonic oscillation can be output voltage ripple.

The source current of pin CTRL is always active. In QR mode, the $R_{slopecomp}$ resistor is replaced by a short, so the modulation of the CTRL voltage is almost negligible.

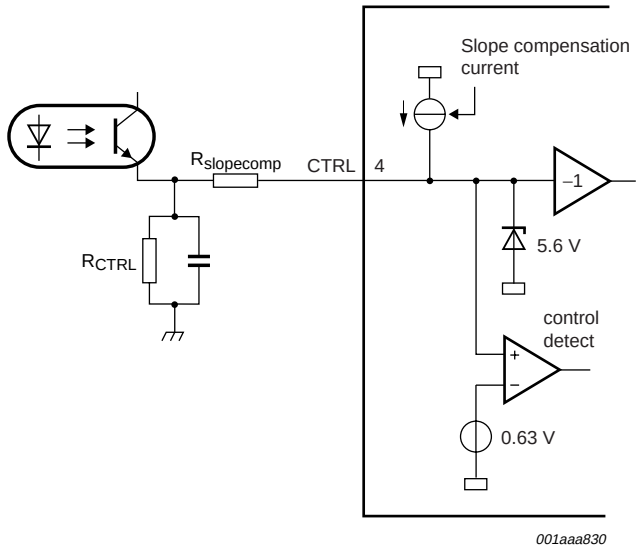


Fig 7. Slope compensation

7.11 Minimum and maximum on-time

The minimum on-time of the SMPS is determined by the LEB time (typical 400 ns). The IC limits the on-time to a maximum time which is dependent on the mode of operation:

QR mode: When the system requires an ‘on-time’ of more than 25 µs, a fault condition is assumed, the IC stops switching and enters the safe restart mode.

CCM: The driver duty cycle is limited to 70 %. So the maximum on-time is correlated to the oscillator time which results in an accurate limit of the minimum input voltage of the flyback converter.

7.12 PROTECT and timing input

The PROTECT input (pin 3) is a multi-purpose (high-impedance) input, which can be used to switch off the IC and create a relatively long timing function. As soon as the voltage on this pin rises above 2.5 V, switching stops immediately. For the timing function, a current of typically 50 µA flows out of pin PROTECT and charges an external capacitor until the activation level of 2.5 V is reached. This current source is only activated when the converter is not in regulation, which is detected by the voltage on pin CTRL (V_{CTRL} < 0.63 V). A (small) discharge current is also implemented to ensure that the capacitor is not charged, for example, by spikes A MOSFET switch is added to discharge the external capacitor and ensure a defined start situation. For the TEA1532AP and the TEA1532AT, the voltage on pin CTRL determines whether the IC enters latched protection mode, or safe restart protection mode:

- When the voltage on pin CTRL is below 0.63 V, the IC is assumed to be out of regulation (e.g. the control loop is open). In this case activating pin PROTECT ($V_{PROTECT}$ > 2.5 V) will cause the converter to stop switching. Once V_{CC} drops below V_{UVLO}, capacitor C_{VCC} will be recharged and the supply will restart. This cycle will be repeated until the fault condition is removed (safe restart mode).
- When the voltage on pin CTRL is above 0.63 V, the output is assumed to be in regulation. In this case activating pin PROTECT ($V_{PROTECT}$ > 2.5 V), by external means, will activate the latch protection of the IC: The voltage on pin V_{CC} will cycle between V_{start} and V_{UVLO}, but the IC will not start switching again until the latch protection is reset. The latch is reset as soon as V_{CC} drops below 4.5 V (typical value) (this only occurs when the mains has been disconnected). The internal overtemperature protection will also trigger this latch; see also Figure 1.

For the TEA1532P and the TEA1532T the IC always enters the latched mode protection independent of the voltage on pin CTRL.

A voltage higher than 3 V on pin PROTECT will always latch the IC. This is independent of the state of the IC.

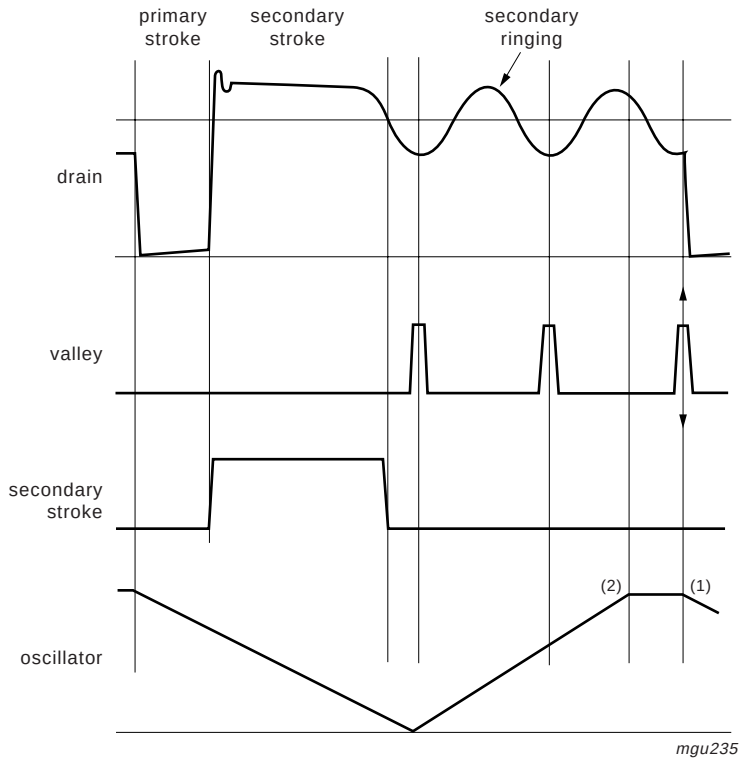
7.13 Valley switching

Refer to Figure 8. A new cycle starts when the power switch is activated. After the on-time (determined by the sense voltage and the internal control voltage), the switch is opened and the secondary stroke starts. After the secondary stroke, the drain voltage shows an oscillation with a frequency of approximately $\frac{1}{2 \times \pi \times \sqrt{L_p \times C_d}}$

where L_p is the primary self inductance of the transformer and C_d is the capacitance on the drain node.

As soon as the oscillator voltage is high again and the secondary stroke has ended, the circuit waits for the lowest drain voltage before starting a new primary stroke. This method is called valley detection. Figure 8 shows the drain voltage, valley signal, secondary stroke signal and the oscillator signal.

In an optimum design, the reflected secondary voltage on the primary side will force the drain voltage to zero. Thus, zero voltage switching is possible, preventing large capacitive switching losses $\left(P = \frac{1}{2} \times C \times V^2 \times f\right)$, and allowing high frequency operation, which results in small and cost effective magnetics.



(1) Start of new cycle at lowest drain voltage.

(2) Start of new cycle in a classical PWM system at high drain voltage.

Fig 8. Signals for valley switching

7.14 Brown-out protection

During the so called brown-out test, the input voltage is slowly decreased. Since the on-time depends on V_i, long on-times at low V_i can damage the (external) power device. This is prevented by stopping the converter when the input voltage drops too low.

When the voltage on pin DEM drops below –50 mV during the on-time (QR mode), the maximum on-time is set to 25 µs. The maximum on-time will be reached while V_i is low. Subsequently, the IC stops switching and V_{CC} drops below V_{UVLO}. Capacitor C_{VCC} will only be recharged and the supply will restart only when voltage V_i is high enough (V_m, also see Section 7.1). In addition to this, a V_i level at which the converter has to enter a safe restart can be set with a demagnetization resistor. During the primary stroke, the rectified mains input voltage is measured by sensing the current drawn from pin DEM. This current depends on the mains voltage, according to the following formula:

$$I_{(DEM)} \approx \frac{V_{aux}}{R_{DEM}} \approx \frac{N \times V_{mains}}{R_{DEM}}$$

Where: $N = \frac{N_{aux}}{N_p}$

The latter function requires an on-time of at least 2 µs. This on-time ensures that a reliable demagnetization current can be measured.

When pin DEM is grounded (CCM), the brown-out protection is disabled. In this case the duty cycle is limited to 0.7, so at low mains voltage the on-time is limited and therefore the dissipation in the FET is limited.

7.15 OverTemperature protection (OTP)

The IC provides accurate OTP. The IC will stop switching when the junction temperature exceeds the thermal shutdown temperature. When V_{CC} drops to V_{UVLO}, capacitor C_{VCC} will be recharged to the V_{start} level, however switching will not restart. Subsequently, V_{CC} will drop again to V_{UVLO}, etc.

Operation only recommences when V_{CC} drops below a level of about 4.5 V (typically, when V_{mains} is disconnected for a short period).

7.16 Soft start-up (pin SENSE)

To prevent transformer rattle at start-up or during hiccup, the transformer peak current is slowly increased by the soft start function. This can be achieved by inserting a resistor and a capacitor between pin SENSE (pin 6) and sense resistor R_{sense}. An internal current source charges the capacitor to $V_{sense} = I_{ss} \times R_{ss}$ (about 0.5 V maximum).

The start level and the time constant of the increasing primary current level can be adjusted externally by changing the values of R_{ss} and C_{ss}.

$$I_{primary(max)} = \frac{V_{ocp} - (I_{ss} \times R_{ss})}{R_{sense}}$$

$$\tau = R_{ss} \times C_{ss}$$

During the start-up phase, the charging current I_{ss} will flow as long as the voltage on pin SENSE is below approximately 0.5 V. If the voltage on pin SENSE exceeds 0.5 V, the soft start current source will start limiting current I_{ss}. At V_{start}, the I_{ss} current source is completely switched off; see Figure 9.

Since the soft start current I_{ss} is subtracted from pin V_{CC} charging current, the R_{ss} value will affect V_{CC} charging current level by a maximum of 60 μA (typical).

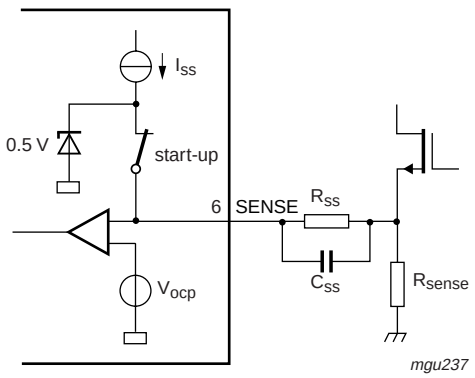


Fig 9. Soft start-up

7.17 Driver

The driver circuit to the gate of the power MOSFET has a current sourcing capability of typically 170 mA and a current sink capability of typically 700 mA at V_{CC} of 9.5 V. At V_{CC} = 15 V, the current sourcing capability is typically 300 mA and the current sink capability typically 1.2 A. This permits fast turn-on and turn-off of the power MOSFET for efficient operation.

A low driver source current has been chosen to limit the $\Delta V/\Delta t$ at switch-on. This reduces Electro Magnetic Interference (EMI) and also limits the current spikes across R_{sense}.

8. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to ground (pin 2); positive currents flow into the chip; pin V_{CC} may not be current driven. The voltage ratings are valid provided other ratings are not violated; current ratings are valid provided the maximum power rating is not violated.

Symbol	Parameter	Conditions		Min	Max	Unit
Voltages						
V_{CC}	supply voltage	continuous		–0.4	+20	V
$V_{PROTECT}$	voltage on pin PROTECT	continuous		–0.4	+5	V
V_{CTRL}	voltage on pin CTRL			–0.4	+5	V
V_{DEM}	voltage on pin DEM	current limited		-	-	V
V_{SENSE}	voltage on pin SENSE	current limited		–0.4	-	V
V_{DRAIN}	voltage on pin DRAIN			–0.4	+650	V
Currents						
I_{CTRL}	current on pin CTRL	d < 10 %		-	50	mA
I_{DEM}	current on pin DEM			–1000	+250	µA
I_{SENSE}	current on pin SENSE			–1	+10	mA
I_{DRIVER}	current on pin DRIVER	d < 10 %		–0.8	+2	A
I_{DRAIN}	current on pin DRAIN			-	5	mA
General						
P_{tot}	total power dissipation	T_{amb} < 70 °C				
		SO8 package		-	0.5	W
		DIP8 package		-	0.75	W
T_{stg}	storage temperature			–55	+150	°C
T_j	junction temperature			–20	+145	°C
ESD						
V_{ESD}	electrostatic discharge voltage	class 1				
	human body model	pins 1 to 7	[1]	-	2000	V
		pin 8 (DRAIN)	[1]	-	1500	V
	machine model		[2]	-	200	V

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[2] Equivalent to discharging a 200 pF capacitor through a 0.75 µH coil and a 10 Ω resistor.

9. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; SO8 package	150	K/W
		in free air; DIP8 package	95	K/W

10. Characteristics

Table 5: Characteristics

T_{amb} = 25 °C; V_{CC} = 15 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Start-up current source (pin DRAIN)						
I_{DRAIN}	supply current drawn from pin DRAIN	V_{DRAIN} > 100 V				
		V_{CC} = 0 V	1.0	1.2	1.4	mA
		with auxiliary supply	-	100	300	µA
V_B	breakdown voltage		650	-	-	V
V_m	mains-dependent operation-enabling level		60	-	100	V
Supply voltage management (pin V_{CC})						
V_{start}	start-up voltage		10.3	11	11.7	V
V_{UVLO}	lock-out undervoltage		8.1	8.7	9.3	V
V_{hys}	hysteresis voltage	$V_{start} - V_{UVLO}$	2.0	2.3	2.6	V
$I_{ch(h)}$	high charging current	V_{DRAIN} > 100 V; V_{CC} < 3 V	–1.2	–1	–0.8	mA
$I_{ch(l)}$	low charging current	V_{DRAIN} > 100 V; 3 V < V_{CC} < V_{UVLO}	–1.2	–0.75	–0.45	mA
$I_{restart}$	restart current	V_{DRAIN} > 100 V; V_{UVLO} < V_{CC} < V_{start}	–650	–550	–450	µA
I_{oper}	supply current under normal operation	no load on pin DRIVER	1.1	1.3	1.5	mA
Demagnetization management (pin DEM)						
$V_{th(DEM)}$	demagnetization comparator threshold voltage		50	80	110	mV
$V_{th(CCM)}$	continuous conduction mode detection threshold voltage		–80	–50	–20	mV
$V_{clamp(neg)}$	negative clamp voltage	I_{DEM} = –500 µA	–0.5	–0.45	–0.40	V
$V_{clamp(pos)}$	positive clamp voltage	I_{DEM} = 250 µA	0.5	0.7	0.9	V
t_{supp}	suppression of transformer ringing at start of secondary stroke		1.1	1.5	1.9	µs
Pulse width modulator						
$t_{on(min)}$	minimum on-time		-	t_{leb}	-	ns
$t_{on(max)}$	maximum on-time	QR mode	20	25	30	µs
δ_{max}	maximum duty-cycle		67	70	73	%

Table 5: Characteristics *...continued*

T_{amb} = 25 °C; V_{CC} = 15 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Oscillator							
f_{osc}	oscillator frequency (fixed frequency)	V_{CTRL} < 1 V		50	63	75	kHz
Duty cycle control (pin CTRL)							
V_{min}	minimum voltage for maximum duty cycle			-	1.0	-	V
V_{max}	maximum voltage for minimum duty cycle			-	1.5	-	V
$\Delta I_{slopecomp}/\Delta t$	slope compensation current			–1.2	–1	–0.8	µA/µs
$V_{CTRL(detect)}$	Control detect level			0.56	0.63	0.70	V
Protection and timing input (pin PROTECT)							
V_{trip}	trip level		[1]	2.37	2.5	2.63	V
$V_{trip(latch)}$	trip level for latch			2.85	3	3.15	V
$V_{CC(latch)(reset)}$	voltage level on pin V_{CC} which resets the latch	$V_{CC(latch)}$ < 2.3 V		-	4.5	-	V
I_{charge}	charge current	V_{CTRL} < 0.63 V		–57	–50	–43	µA
$I_{discharge}$	discharge current			-	100	-	nA
Valley switch (pin DRAIN)							
$\Delta V/\Delta t_{valley}$	valley recognition voltage change			–43	-	+43	V/µs
$t_{valley-swon}$	delay from valley recognition to switch-on		[2]	-	150	-	ns
Overcurrent and winding short-circuit protection (pin SENSE)							
$V_{sense(max)}$	maximum source voltage for OCP	$\Delta V/\Delta t$ = 0.1 V/µs		0.48	0.52	0.56	V
t_{PD}	propagation delay from detecting $V_{sense(max)}$ to switch-off	$\Delta V/\Delta t$ = 0.5 V/µs		-	140	185	ns
t_{leb}	blanking time for current and winding short-circuit protection			330	400	470	ns
I_{ss}	soft start current	V_{sense} < 0.5 V		45	60	75	µA
Brown-out protection (pin DEM)							
$I_{brown-out}$	brown-out protection current	A constant $I_{brown-out}$ is drawn from pin DEM.	[3]	–68	–60	–52	µA
$t_{on(min)(brown-out)}$	minimum on-time for enabling the brown-out protection.			1.5	2	2.5	µs
Driver (pin DRIVER)							
I_{source}	source current	V_{CC} = 9.5 V; V_{DRIVER} = 2 V		-	–170	–88	mA
I_{sink}	sink current	V_{CC} = 9.5 V					
		V_{DRIVER} = 2 V		-	300	-	mA
		V_{DRIVER} = 9.5 V		400	700	-	mA
$V_{o(max)}$	maximum output voltage	V_{CC} > 12 V		-	11.5	12	V

Table 5: Characteristics *...continued*

T_{amb} = 25 °C; V_{CC} = 15 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Temperature protection							
$T_{prot(max)}$	maximum temperature protection level			130	140	150	°C
$T_{prot(hyst)}$	hysteresis for the temperature protection level		[4]	-	8	-	°C

[1] TEA1532AP and TEA1532AT: safe restart; TEA1532P and TEA1532T: latch.

[2] Guaranteed by design.

[3] V_i detection level. Set by the demagnetization resistor R_{DEM}; see Section 7.14.

[4] Valid for V_{CC} > 2 V.

11. Application information

A converter with the TEA1532(A)P; TEA1532(A)T consists of an input filter, a transformer with a third winding (auxiliary), and an output stage with a feedback circuit.

Capacitor C_{VCC} buffers the IC supply voltage, which is powered via the internal current source, that is connected to the rectified mains, during start-up and via the auxiliary winding during operation.

A sense resistor R_{sense} converts the primary current into a voltage at pin SENSE. The value of R_{sense} defines the maximum primary peak current.

Figure 10 shows a flyback configuration using the discontinuous conduction mode. Pin PROTECT is used in this example for external overvoltage protection and open loop or output short-circuit protection. If this pin is not used, it must be tied to ground. Figure 13 shows a flyback configuration using the continuous conduction mode. Pin PROTECT is used in this example for external overtemperature protection and open loop or output short-circuit protection.

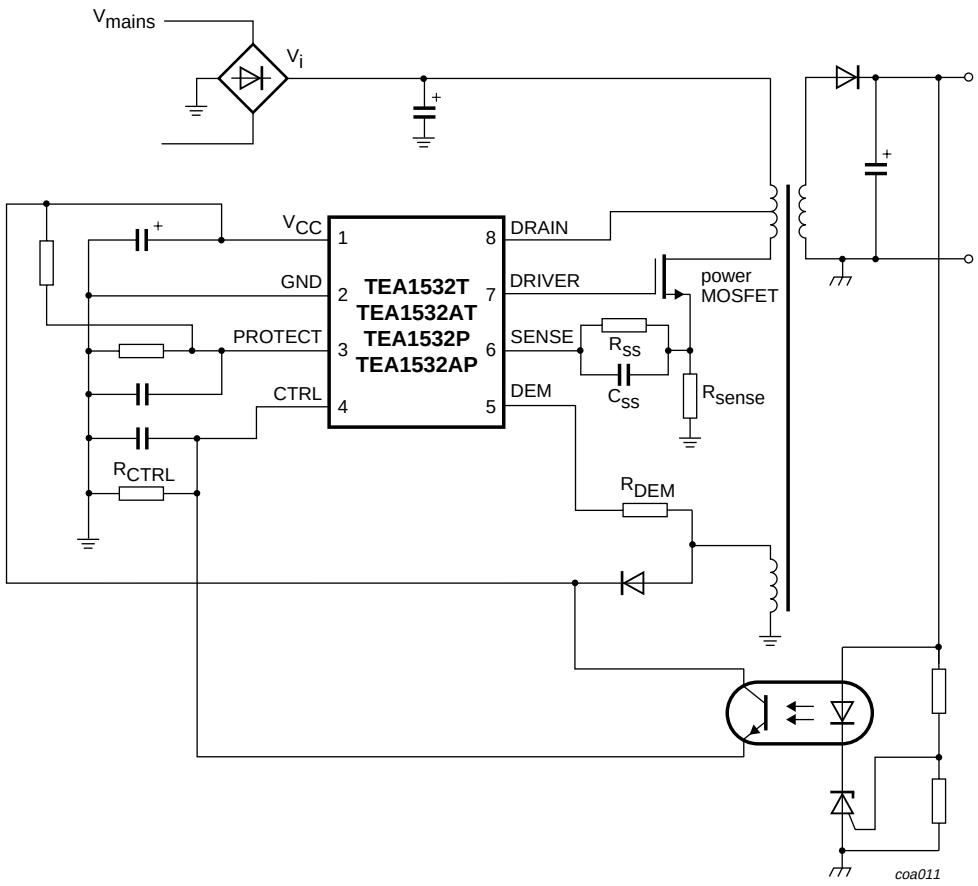
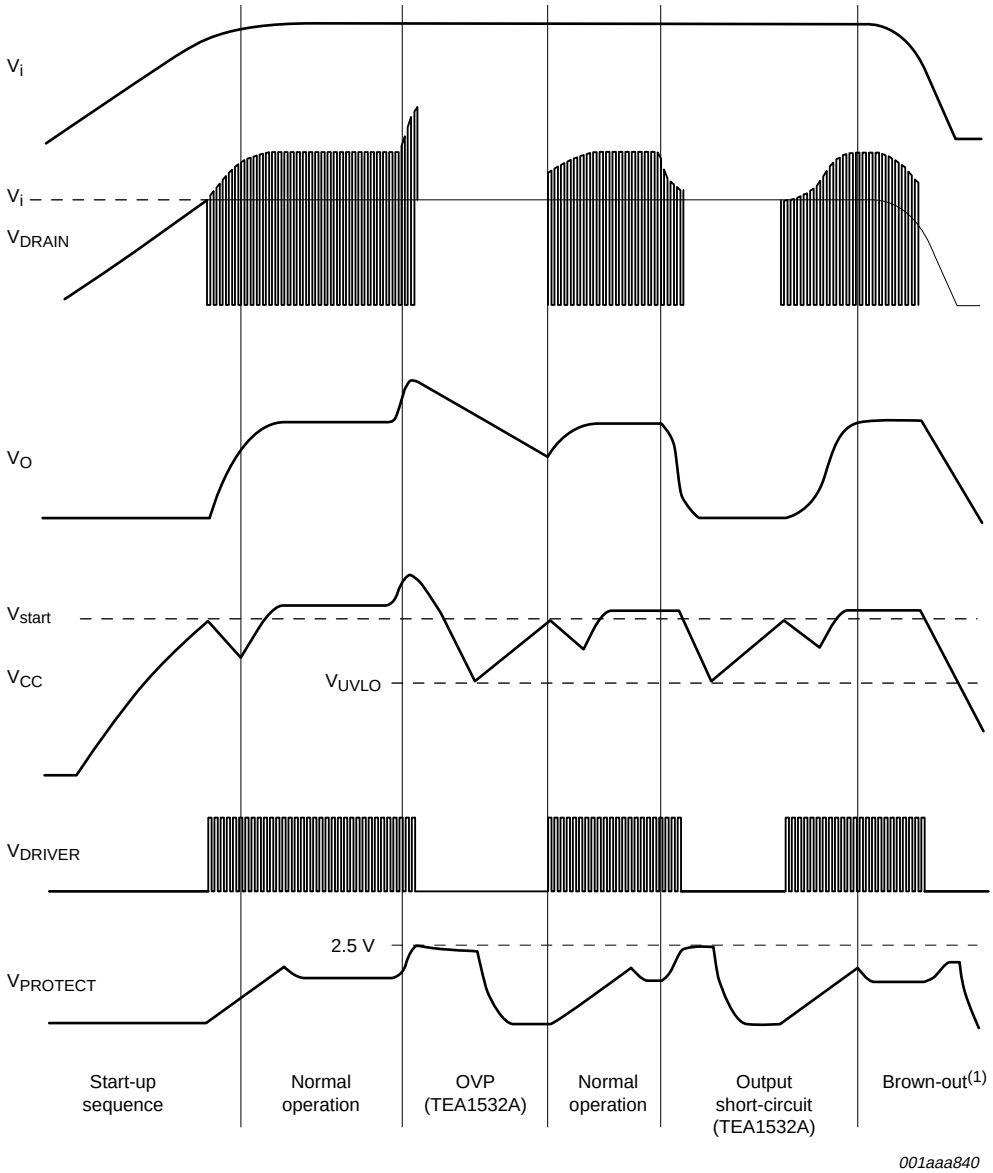
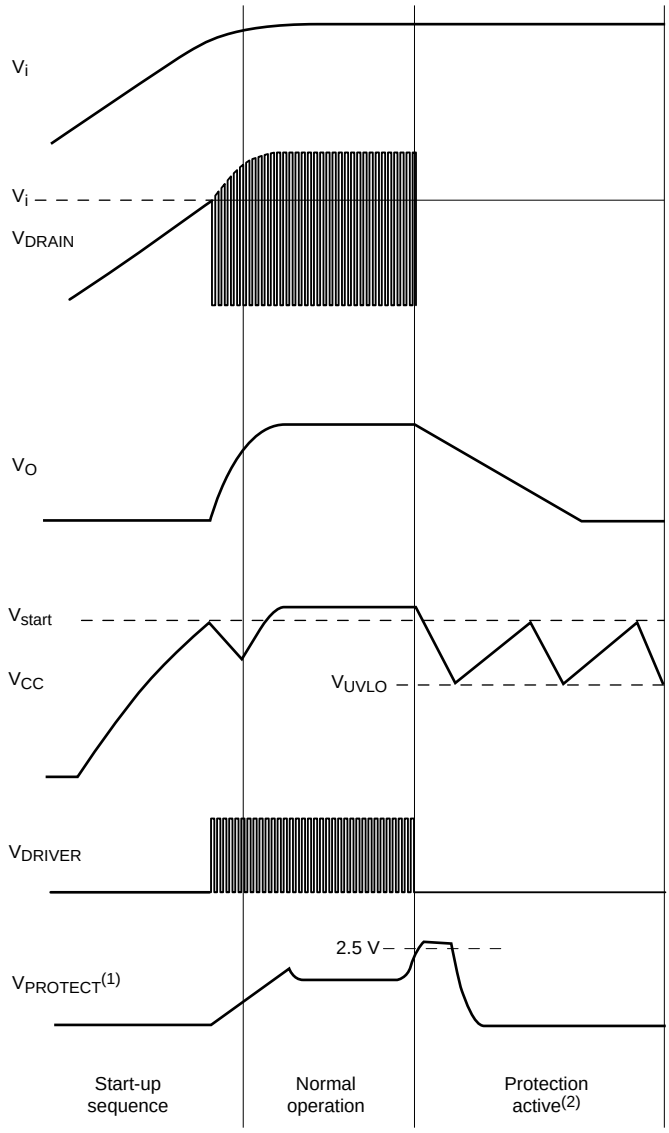


Fig 10. Flyback configuration using the discontinuous conduction mode



(1) In CCM, the brown-out protection is implemented by the maximum duty cycle in combination with pin PROTECT.

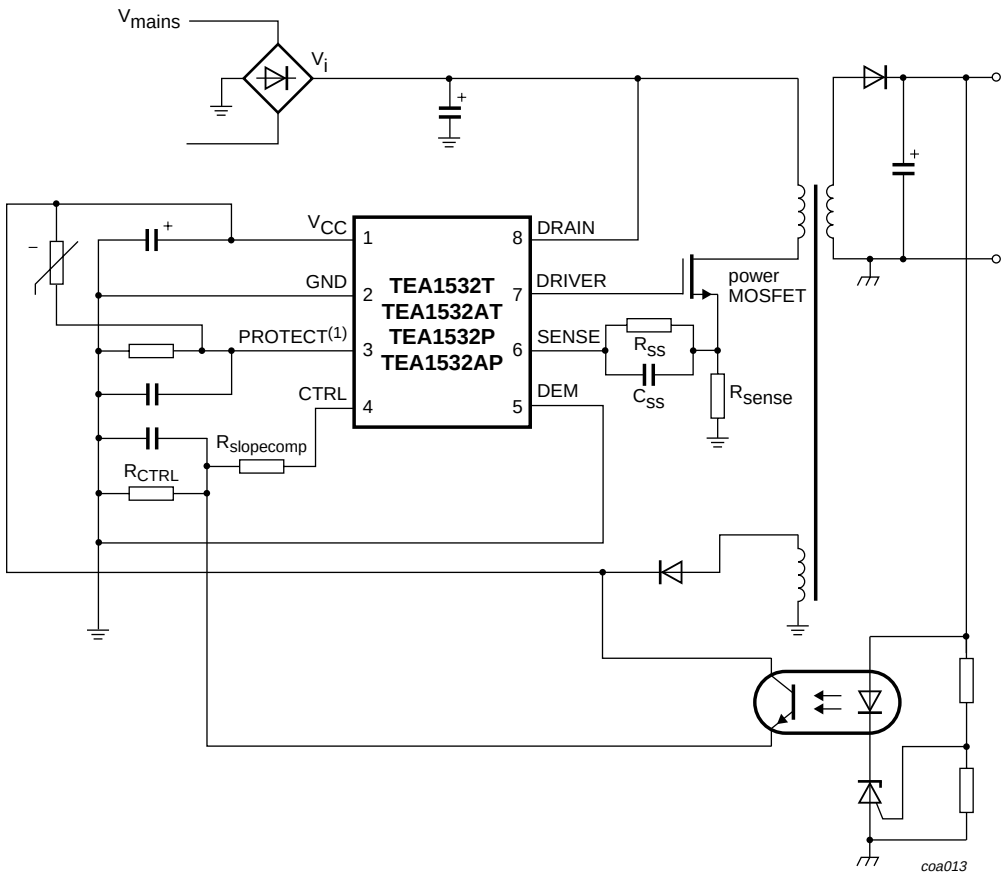
Fig 11. Typical waveforms 1



(1) When $V_{PROTECT}$ is forced above 3 V, the protection is always latched. So the IC is not started at V_{start} unless the V_{CC} voltage drops below the $V_{CC(reset)}$ level. This is the same action used for external OTP compensation described in Section 7.15.

(2) External OTP for TEA1532T, TEA1532P, TEA1532AT and TEA1532AP; OVP and output short circuit for TEA1532P and TEA1532T.

Fig 12. Typical waveforms 2



(1) Pin PROTECT is used in this example for external OTP and open loop or output short-circuit protection. Slope compensation is determined by the value of $R_{slopecomp}$.

Fig 13. Flyback configuration using the continuous conduction mode

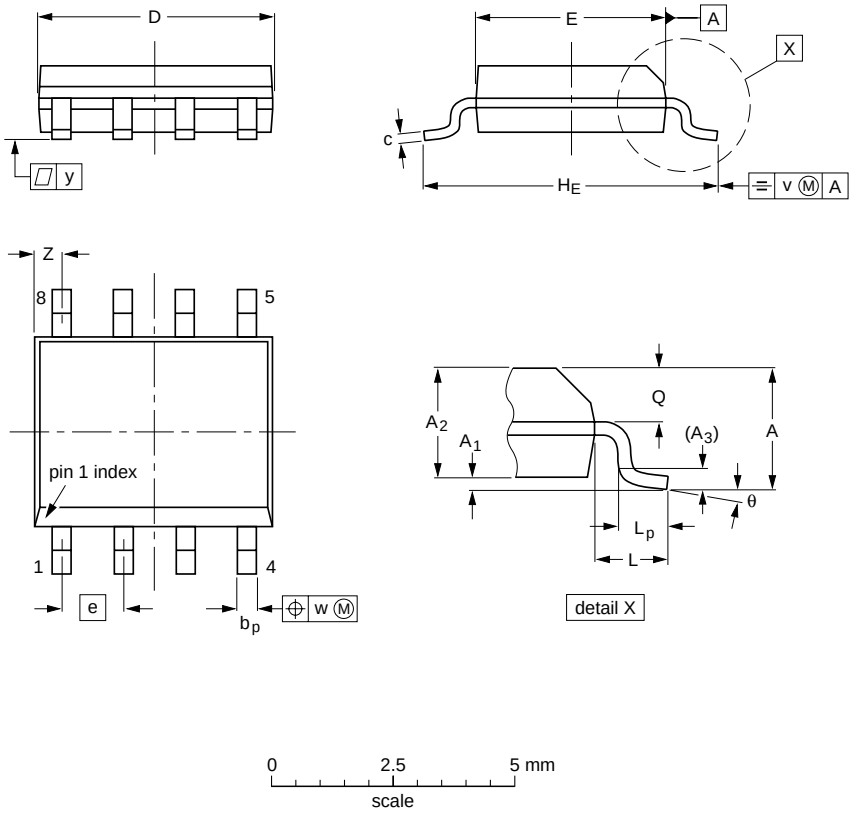
12. Test information

12.1 Quality information

The *General Quality Specification for Integrated Circuits, SNW-FQ-611* is applicable.

13. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

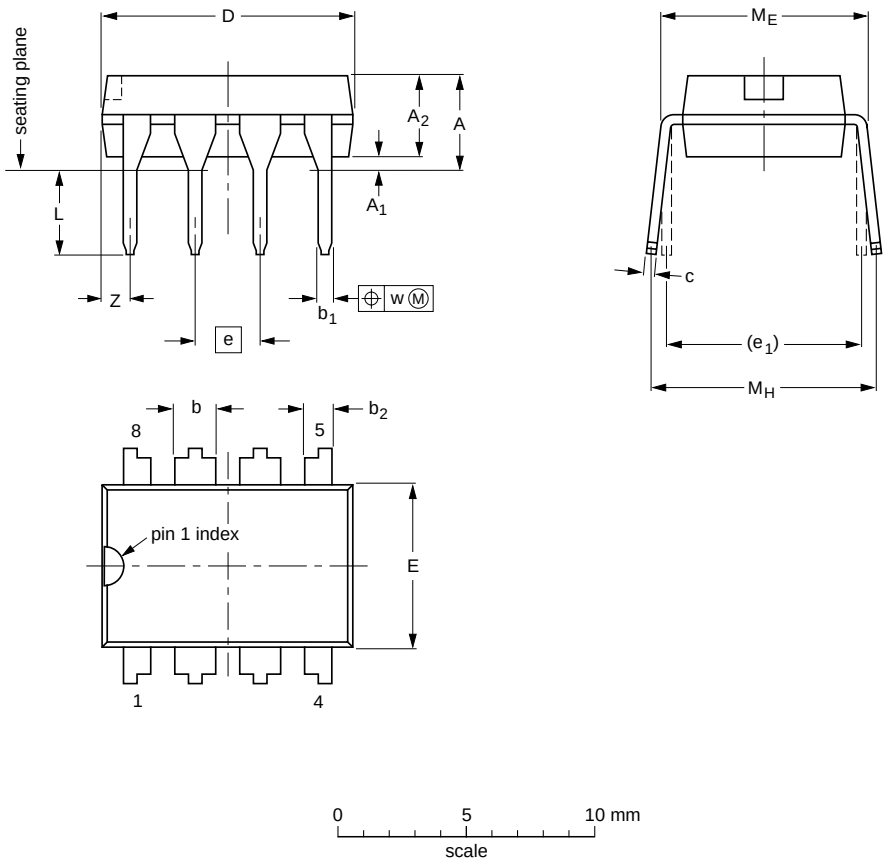
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 14. Package outline SOT96-1 (SO8)

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.02	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT97-1	050G01	MO-001	SC-504-8			~~99-12-27~~ 03-02-13

Fig 15. Package outline SOT97-1 (DIP8)

14. Soldering

14.1 Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

14.2 Through-hole mount packages

14.2.1 Soldering by dipping or by solder wave

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

14.2.2 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 °C and 400 °C, contact may be up to 5 seconds.

14.3 Surface mount packages

14.3.1 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages

- for packages with a thickness ≥ 2.5 mm
- for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.

- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

14.3.2 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.3.3 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

14.4 Package related soldering information

Table 6: Suitability of IC packages for wave, reflow and dipping soldering methods

Mounting	Package [1]	Soldering method		
		Wave	Reflow [2]	Dipping
Through-hole mount	CPGA, HCPGA	suitable	–	–
	DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable [3]	–	suitable
Through-hole-surface mount	PMFP [4]	not suitable	not suitable	–
Surface mount	BGA, HTSSON..T [5], LBGA, LFBGA, SQFP, SSOP..T [5], TFBGA, VFBGA, XSON	not suitable	suitable	–
	DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [6]	suitable	–
	PLCC [7], SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended [7] [8]	suitable	–
	SSOP, TSSOP, VSO, VSSOP	not recommended [9]	suitable	–
	CWQCCN..L [10], WQCCN..L [10]	not suitable	not suitable	–

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[4] Hot bar soldering or manual soldering is suitable for PMFP packages.

[5] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[6] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[7] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[8] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[9] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[10] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

15. Revision history

Table 7: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
TEA1532_2	20050204	Product data sheet	-	9397 750 14319	TEA1532_1
Modifications:	• Products TEA1532AT and TEA1532AP added: – Updated Section 4 “Ordering information” – Updated Section 6 “Pinning information” – Changed product numbers in Figure 1, Figure 4, Figure 7, Figure 10, and Figure 13 • Added note to Figure 1 • Modified Figure 6.				
TEA1532_1	20040528	Preliminary data sheet	-	9397 750 13113	-

16. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

17. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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21. Contents

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