STLC8201

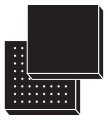
DUAL BAND WIRELESS LAN BASEBAND PROCESSOR

DATA BRIEF

1 FEATURES

- Tri Mode 802.11a 802.11g and 802.11b compliant.
- AgileRF allows fully automated roaming between different modes.
- Implements data rates of 6, 9, 12, 18, 24, 36, 48 and 54 Mbps in 802.11a and 802.11g modes, using an advanced OFDM processor with channel equalizer.
- Implements data rates of 1, 2, 5.5 and 11 Mbps in 802.11b mode, using advanced RAKE and decision feedback equalization.
- Improved PA efficiency using digital pre-distortion linearization and active bias control.
- Gain and Phase imbalance correction improves Rx sensitivity.
- Supports receive antenna diversity for both bands
- Supports 802.11b short preamble.
- On-chip 10 bit ADC and DAC converters for I/Q data.
- On-chip 10 bit DAC for analog AGC control.
- On-chip 10 bit DACs to support DC offset correction in Zero-IF systems.
- On-chip 10 bit DAC, and dedicated I/O to provide transmit power control (TPC).
- On-chip general purpose 10 bit ADC for power supply monitoring, PA output power monitoring or temperature sense.
- Hardware assisted 40 and 128 bit WEP and WEP2 (TKIP) engine. Hardware assisted AES encryption.
- A low frequency standby clock and advanced power management extend battery life in portable equipment.
- Powerful 32 bit CPU and protocol accelerator implement the MAC functionality.
- On-chip system memory removes the need for external FLASH or SRAM reducing complexity and cost.
- Firmware is loaded from the host processor allowing automated software upgrade.
- Supports UART, Cardbus32 and MiniPCI interfaces to host processor.
- Serial EEPROM memory interface to hold PCI/ CardBus32 configuration.
- JTAG interface for manufacturing test.
- Software drivers for Microsoft Windows 2000™, Windows XP™, Win98/Me.

Figure 1. Package



BGA256 (17x17x1.7mm)

Table 1. Order Codes

Part Number	Package
STLC8201	BGA256

2 APPLICATIONS

- Cardbus32 card wireless LAN adapters.
- MiniPCI card wireless LAN adapters.
- Wireless LAN access points and bridges.

3 DESCRIPTION

The STMicroelectronics STLC8201 wireless LAN baseband processor is an integrated Medium Access Controller and Physical Layer Processor. It is designed to directly interface with STMicroelectronics's STLC8100 RF transceiver, and with 3rd party power amplifiers to provide a complete wireless LAN solution compliant with IEEE802.11b, IEEE802.11g and IEEE802.11a.

The STLC8201 includes a unique technology to deliver dual band multi-mode Access Point with band interleaving. This allows supporting clients in both bands without duplicating baseband or RF functionality.

Powerful security features include WEP, WPA, WPA2 and AES encryption engines along with support for 802.1x authentication protocols.

High quality multimedia streaming is enabled with Quality of Service (QoS) protocols supported by an advanced DMA engine that delivers packet pri-

oritization.

The chip comprises three major blocks:

-Front End -Interface to the radio and PA

-Modem - OFDM and CCK digital signal processing for RX and TX

-MAC -CPU, protocol accelerator, memory, host and peripheral interfaces.

The flexible Front-End RF interface provides baseband I/Q receive inputs and transmit outputs along with a general purpose serial interface for configuration and testing of the STLC8100 and PA module. The host interface supports mini-PCI and CardBus32.

A powerful CPU is supported by the hardware accelerator that carries out the real time tasks of interpreting received packets then preparing and responding fast enough to deliver sustained 54MBits/sec throughput without losing the flexibility to future-proof the design. The embedded DMA engine increases efficiency by rapidly sorting data as it passes through the system without loading the processor core.

Ample on-chip memory is provided to run all MAC software with sufficient space capacity to accommodate future enhancements avoiding the need for external flash. A serial EEPROM memory interface is provided on which the PCI/CardBus configuration and MAC address is stored.

Figure 2. Block Diagram

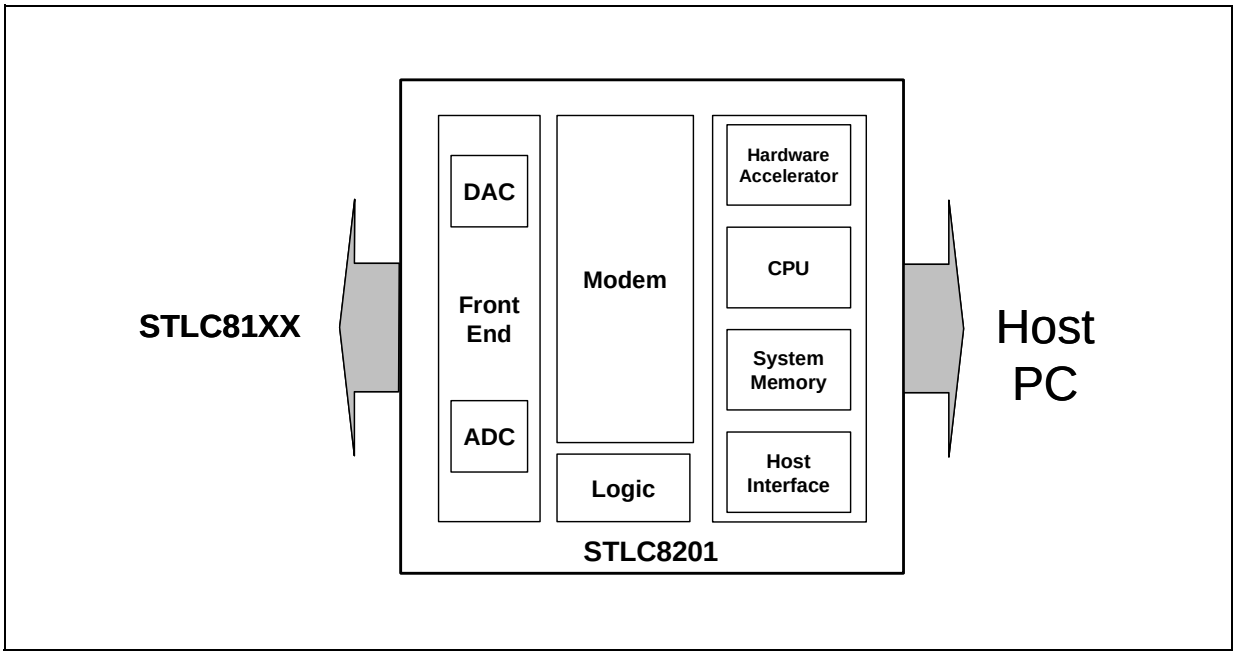
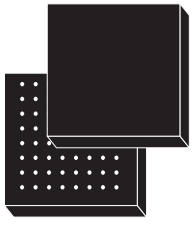


Figure 3. BGA256 (17x17x1.7mm) Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.210		1.700	0.047		0.067
A1	0.300			0.0118		
A2		1.120			0.044	
b	0.500	0.600	0.700	0.020	0.024	0.027
D	16.800	17.000	17.200	0.661	0.669	0.677
D1		15.000			0.590	
E	16.800	17.000	17.200	0.661	0.669	0.677
E1		15.000			0.590	
e	0.900	1.000	1.100	0.035	0.039	0.043
f	0.750	1.000	1.250	0.029	0.039	0.049
ddd			0.200			0.008

OUTLINE AND MECHANICAL DATA



Body: 17 x 17 x 1.7mm

LFBGA256
Low Profile Ball Grid Array

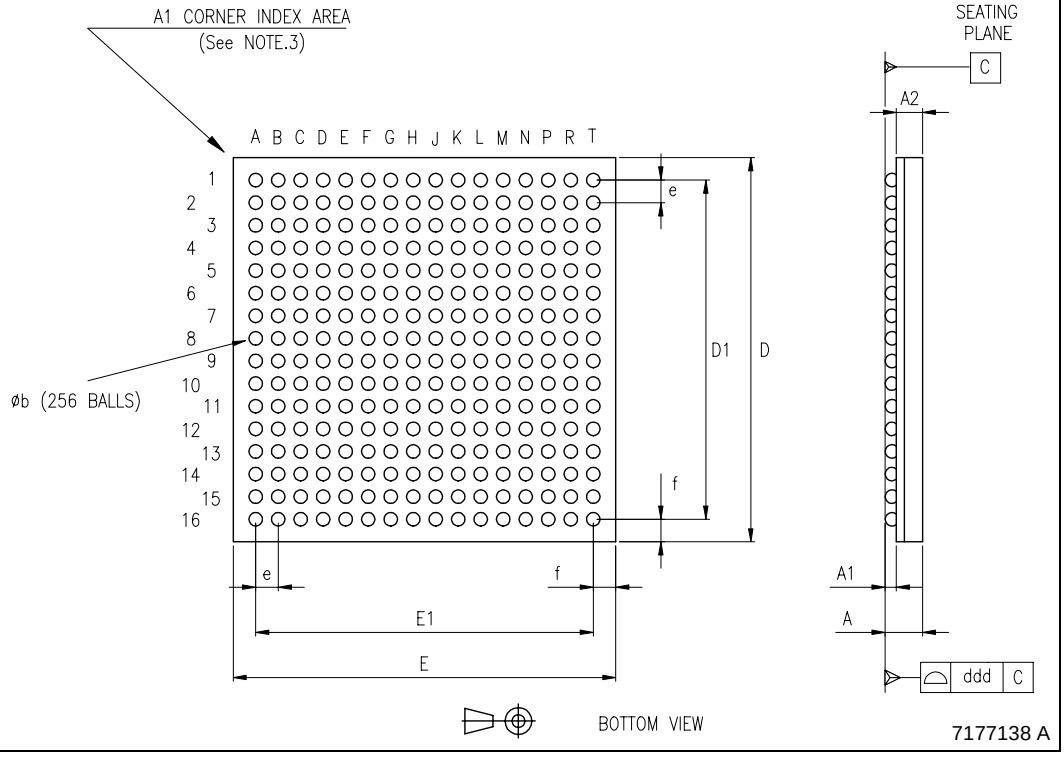


Table 2. Revision History

Date	Revision	Description of Changes
May 2004	1	First Issue