rev 1.0

LCD Panel EMI Reduction IC

Features

- FCC approved method of EMI attenuation.
- Provides up to 15 dB of EMI suppression
- Generates a low EMI spread spectrum clock of the input frequency
- 50 MHz to 170 MHz input frequency range
- Optimized for 54MHz, 65MHz, 81MHz, 140MHz, and 162MHz pixel clock frequencies
- Internal loop filter minimizes external components and board space
- 8 selectable spread ranges, up to +/- 2.2%
- SSON# control pin for spread spectrum enable and disable options
- 2 selectable modulation rates
- Low cycle-to-cycle jitter
- 3.3V operating voltage
- 16 mA output drives
- TTL or CMOS compatible outputs
- Ultra low power CMOS design
- Supports most mobile graphic accelerator and LCD timing controller specifications
- Available in 8 pin SOIC and TSSOP

Product Description

The P2040C is a selectable spread spectrum frequency modulator designed specifically for digital flat panel applications. The P2040C reduces electromagnetic interference (EMI) at the clock source which provides system wide reduction of EMI of all clock dependent signals. The P2040C allows significant system cost savings by reducing the number of circuit board layers and shielding that are traditionally required to pass EMI regulations.

The P2040C uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all-digital method.

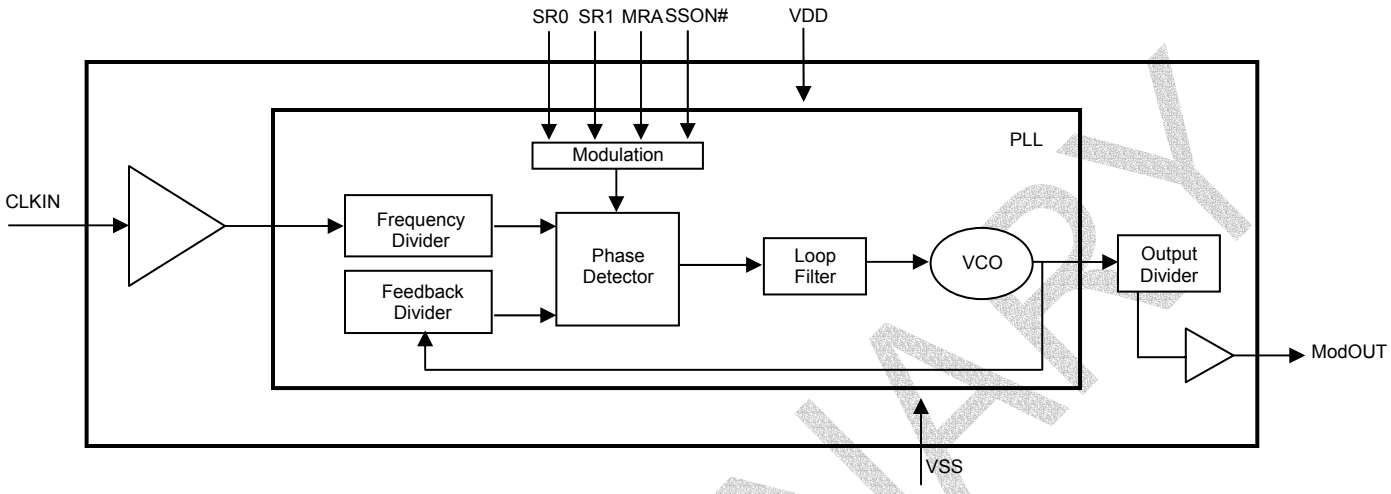
The P2040C modulates the output of a single PLL in order to “spread” the bandwidth of a synthesized clock and, more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal’s bandwidth is called “spread spectrum clock generation”.

Applications

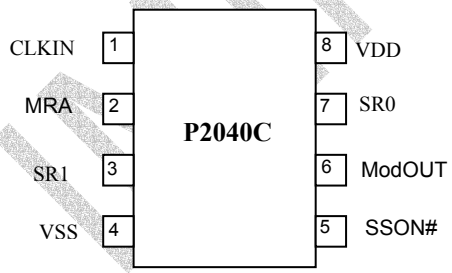
The P2040C is targeted towards digital flat panel applications for Notebook PCs, Palm-size PCs, Office Automation Equipments, and LCD Monitors.

Alliance Semiconductor
2575, Augustine Drive • Santa Clara, CA • Tel: 408.855.4900 • Fax: 408.855.4999 • www.alsc.com

Block Diagram



Pin Configuration



Pin Description

Pin#	Pin Name	Type	Description
1	CLKIN	I	External reference frequency input. Connect to externally generated reference signal.
2	MRA	I	Digital logic input used to select modulation rate. This pin has an internal pull-up resistor.
3	SR1	I	Digital logic input used to select Spreading Range. This pin has an internal pull-up resistor.
4	VSS	P	Ground to entire chip. Connect to system ground.
5	SSON#	I	Digital logic input used to enable Spread Spectrum function (Active LOW). Spread Spectrum function enabled when LOW, disabled when HIGH. This pin has an internal pull-low resistor.
6	ModOUT	O	Spread spectrum clock output.
7	SR0	I	Digital logic input used to select Spreading Range. This pin has an internal pull-up resistor.
8	VDD	P	Power supply for the entire chip (3.3V)

Modulation Selection (Commercial) – Table 1

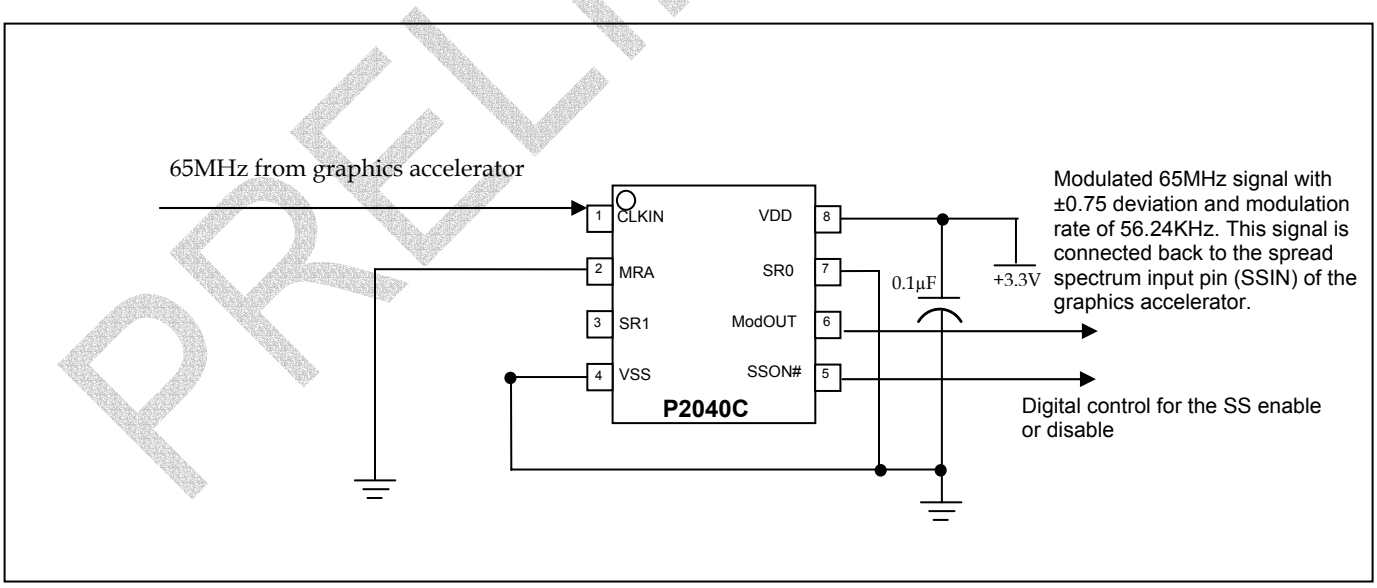
MRA	SR1	SR0	Spreading Range					Modulation Rate
			54 MHz	65 MHz	81 MHz	108 MHz	162 MHz	
0	0	0	+/-1.4%	+/-1.2%	+/-1.0%	+/-0.8%	+/-0.4%	(Fin/80) * 62.49 KHz
0	0	1	+/-2.0%	+/-1.9%	+/-1.6%	+/-1.2%	+/-0.8%	(Fin/80) * 62.49 KHz
0	1	0	+/-1.1%	+/-0.9%	+/-0.5%	+/-0.4%	+/-0.3%	(Fin/80) * 62.49 KHz
0	1	1	+/-1.8%	+/-1.5%	+/-1.0%	+/-0.6%	+/-0.4%	(Fin/80) * 62.49 KHz
1	0	0	+/-1.3%	+/-1.3%	+/-1.3%	+/-1.2%	+/-1.1%	(Fin/80) * 20.83 KHz
1	0	1	+/-2.2%	+/-2.1%	+/-2.1%	+/-1.9%	+/-1.8%	(Fin/80) * 20.83 KHz
1	1	0	+/-1.4%	+/-1.3%	+/-1.4%	+/-1.2%	+/-0.9%	(Fin/80) * 20.83 KHz
1	1	1	+/-2.1%	+/-2.1%	+/-2.1%	+/-2.0%	+/-1.4%	(Fin/80) * 20.83 KHz

Spread Spectrum Selection

Table 1 illustrates the possible spread spectrum options. The optimal setting should minimize system EMI to the fullest without affecting system performance. The spreading is described as a percentage deviation of the center frequency (Note: the center frequency is the frequency of the external reference input on CLKIN, Pin 1).

Example: P2040C is designed for high resolution flat panel applications and is able to support panel frequencies from 54MHz to 170MHz. For a 65MHz pixel clock frequency, a spreading selection of MRA=0, SR1=1 and SR0=1 provides a percentage deviation of +/-1.50% (see Table 1). This results in frequency on ModOUT being swept from 64.03MHz to 65.98MHz at a modulation rate of 50.77KHz (see Table 1). This particular example (see Figure below) given here is a common EMI reduction method for notebook LCD panel and has already been implemented by most of the leading OEM and mobile graphic accelerator manufacturers.

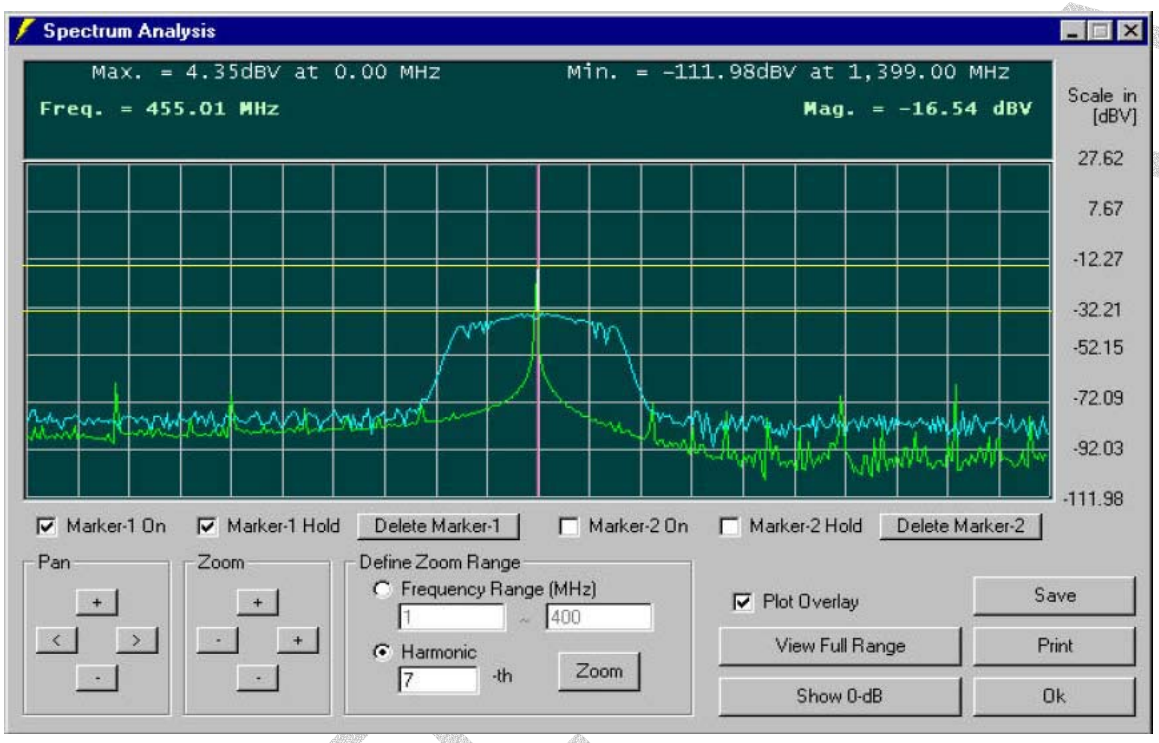
P2040C Application Schematic for Mobile LCD Graphics



rev 1.0

EMC Software Simulation

By using Alliance EMI-Lator®[1] electromagnetic interference simulation software, radiated system level EMI analysis can be made easier to allow a quantitative assessment of EMI reduction products. The simulation engine of this EMC software has already been characterized to correlate to the electrical characteristics of the Alliance EMI reduction ICs. The following illustration is an example of the simulation result. Please visit our website at www.alsc.com for information on how to obtain a free copy and a demonstration of the EMI-Lator simulation software.



Simulation results From EMI-Lator®

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	-0.5 to +7.0	V
T_{STG}	Storage Temperature	-65 to +125	ºC
T_A	Operating Temperature	0 to +70	ºC
Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.			

DC Electrical Characteristics

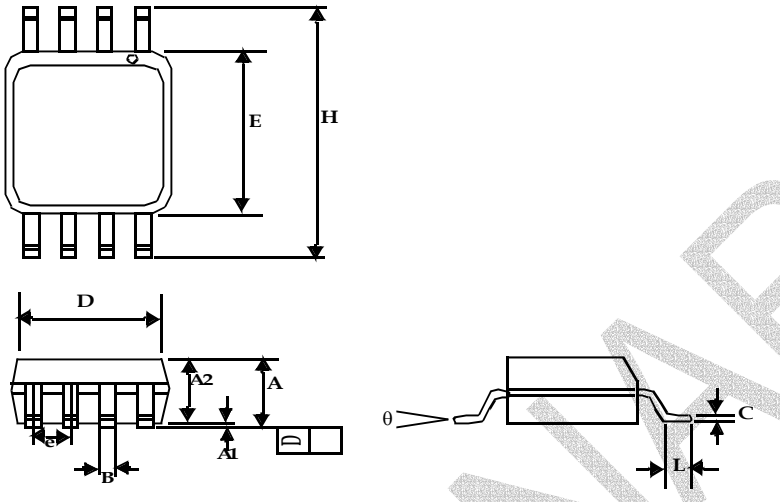
Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage	GND – 0.3	-	0.8	V
V_{IH}	Input High Voltage	2.0	-	V_{DD} + 0.3	V
I_{IL}	Input Low Current (pull-up resistor on inputs SR0, 1 and MRA)	-	-	-35	µA
I_{IH}	Input High Current (pull-down resistor on input SSON#)	-	-	35	µA
V_{OL}	Output Low Voltage (VDD=3.3V, IOL = 20 mA)	-	-	0.4	V
V_{OH}	Output High Voltage (VDD=3.3V, IOH = 20 mA)	2.5	-	-	V
I_{DD}	Static Supply Current	-	0.6	-	mA
I_{CC}	Dynamic Supply Current (3.3V and 15 pF loading)	9	16	22	mA
V_{DD}	Operating Voltage	2.7	3.3	3.7	V
t_{ON}	Power Up Time (First locked clock cycle after power up)		0.18		mS
Z_{OUT}	Clock Output Impedance		50		Ω

AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input Frequency, P2040C	50	**120**	175	MHz
t_{LH} *	Output Rise Time (0.8V to 2.0V)	0.7	0.9	1.1	ns
t_{HL} *	Output Fall Time (2.0V to 0.8V)	0.6	0.8	1.0	ns
t_{JC}	Jitter (cycle to cycle)	-	-	360	ps
t_D	Output Duty Cycle	45	50	55	%
*t_{LH} and t_{HL} are measured into a capacitive load of 15pF					

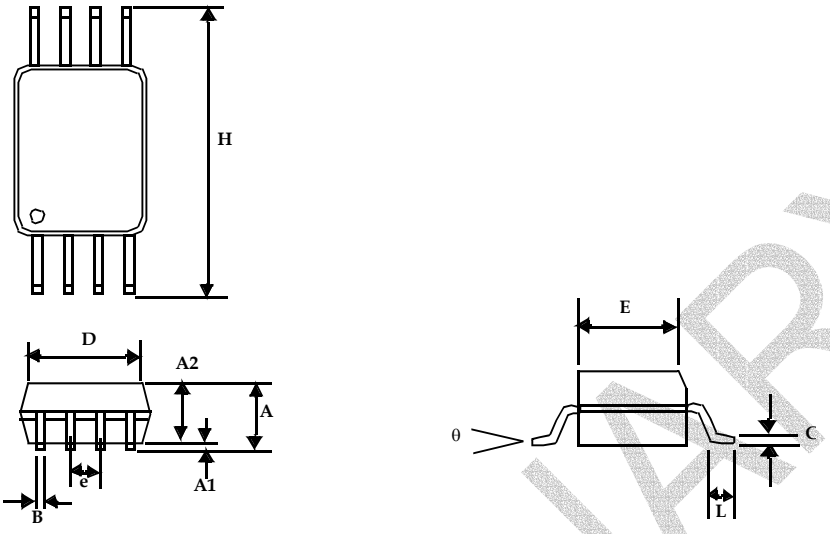
Package Information

8-Pin SOIC



Symbol	Dimensions in inches		Dimensions in millimeters	
	Min	Max	Min	Max
A	0.057	0.071	1.45	1.80
A1	0.004	0.010	0.10	0.25
A2	0.053	0.069	1.35	1.75
B	0.012	0.020	0.31	0.51
C	0.004	0.01	0.10	0.25
D	0.186	0.202	4.72	5.12
E	0.148	0.164	3.75	4.15
e	0.050 BSC		1.27 BSC	
H	0.224	0.248	5.70	6.30
L	0.012	0.028	0.30	0.70
θ	0°	8°	0°	8°

8-Pin TSSOP



	Dimensions in inches		Dimensions in millimeters	
Symbol	Min	Max	Min	Max
A	0.047			1.10
A1	0.002	0.006	0.05	0.15
A2	0.031	0.041	0.80	1.05
B	0.007	0.012	0.19	0.30
C	0.004	0.008	0.09	0.20
D	0.114	0.122	2.90	3.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.244	0.260	6.20	6.60
L	0.018	0.030	0.45	0.75
θ	0°	8°	0°	8°

rev 1.0

Ordering Information

Part Number	Marking	Package Type	Qty/reel	Temperature
A2040C-08ST	A2040C	8-Pin SOIC, TUBE		-40°C to 125°C
A2040C-08SR	A2040C	8-Pin SOIC, TAPE & REEL	2500	-40°C to 125°C
A2040C-08TT	A2040C	8-Pin TSSOP, TUBE		-40°C to 125°C
A2040C-08TR	A2040C	8-Pin TSSOP, TAPE & REEL	2500	-40°C to 125°C
I2040C-08ST	I2040C	8-Pin SOIC, TUBE		-40°C to 125°C
I2040C-08SR	I2040C	8-Pin SOIC, TAPE & REEL	2500	-40°C to 125°C
I2040C-08TT	I2040C	8-Pin TSSOP, TUBE		-40°C to 125°C
I2040C-08TR	I2040C	8-Pin TSSOP, TAPE & REEL	2500	-40°C to 125°C
P2040C-08ST	P2040C	8-Pin SOIC, TUBE		0°C to 70°C
P2040C-08SR	P2040C	8-Pin SOIC, TAPE & REEL	2500	0°C to 70°C
P2040C-08TT	P2040C	8-Pin TSSOP, TUBE		0°C to 70°C
P2040C-08TR	P2040C	8-Pin TSSOP, TAPE & REEL	2500	0°C to 70°C

Part Numbering Guide

X	2040	C	08	XX
1	2	3	4	5

1. Flow Prefix:
   a. A = Automotive temperature range (-40°C to 125°C)
   b. I = Industrial Temperature range (-40°C to 85°C)
   c. C = Commercial temperature range (0°C to 70°)
2. Device Number
3. Deviation (%) and spread option identifier
4. Device pin count
5. Package identifier
   a. ST – SOIC in TUBE
   b. SR – SOIC in TAPE & REEL
   c. TT – TSSOP in TUBE
   d. TR – TSSOP in TAPE & REEL

Alliance Semiconductor Corporation
2595, Augustine Drive,
Santa Clara, CA 95054
Tel# 408-855-4900
Fax: 408-855-4999
www.alsc.com

Preliminary Information
Part Number: P2040C
Document Version: v1.0

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to Alliance Semiconductor, dated 11-11-2003