PRELIMINARY

MX28F2100B

2M-BIT [256K x 8/128K x 16] CMOS FLASH MEMORY

FEATURES

- 262,144x8/131,072x16 switchable
- Fast access time: 70/90/120ns
- Low power consumption
  - 50mA maximum active current
  - 100uA maximum standby current
- Programming and erasing voltage 12V ± 7%
- Command register architecture
  - Byte/Word Programming (50 us typical)
  - Auto chip erase 5 sec typical (including preprogramming time)
  - Block Erase (Any one from 5 blocks:16K-Byte x1, 8K-Byte x2, 96K-Byte x1, and 128K-Byte x1)
  - Auto Erase with Erase Suspend capability
- Status Register feature for Device status detection
- Auto Erase (chip & block) and Auto Program
  - Status Registers
- 10,000 minimum erase/program cycles
- Latch-up protected to 100mA from -1 to VCC+1V
- Package type:
  - 44-pin SOP
  - 48-pin TSOP (Type 1)

GENERAL DESCRIPTION

The MX28F2100B is a 2-mega bit Flash memory organized as 256K bytes of 8 bits or 128K words of 16 bits switchable. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX28F2100B is packaged in 44-pin SOP and 48-pin TSOP(I). It is designed to be reprogrammed and erased in-system or in-standard EPROM programmers.

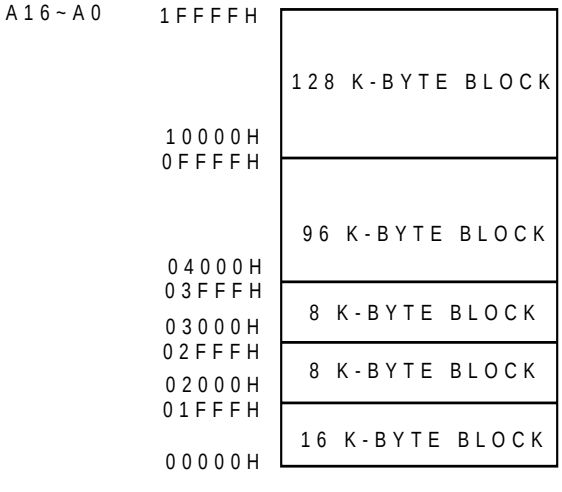
The standard MX28F2100B offers access times as fast as 70ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX28F2100B has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX28F2100B uses a command register to manage this functionality. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

MXIC Flash technology reliably stores memory contents even after 10,000 erase and program cycles. The MXIC cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The MX28F2100B uses a 12.0V ± 7% VPP supply to perform the High Reliability Erase and auto Program/Erase algorithms.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC + 1V.

BLOCK STRUCTURE

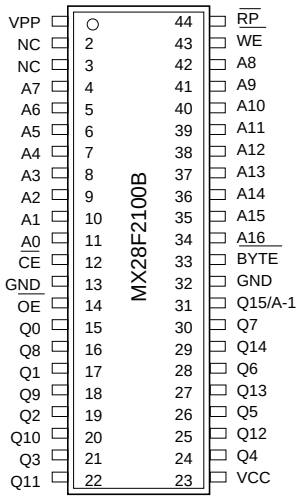


Word Mode (x16) Memory Map

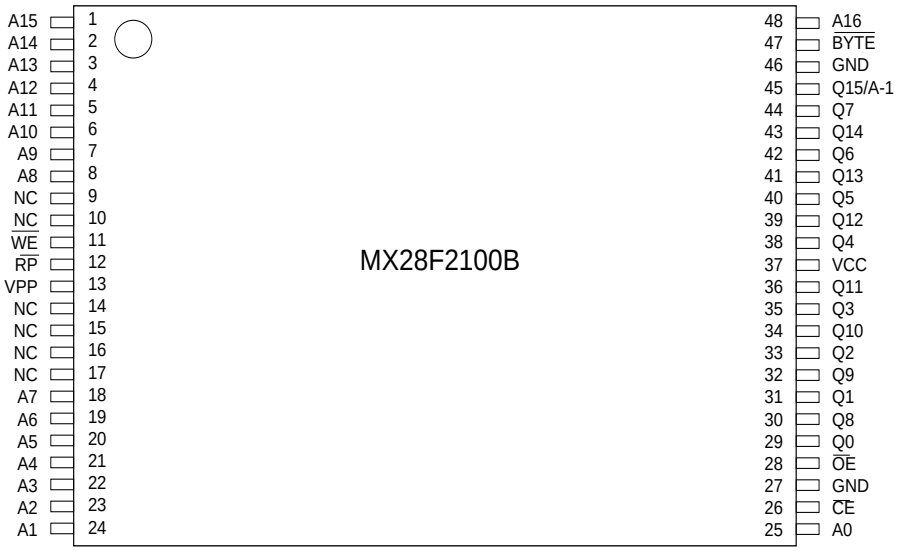
*Byte Mode operation should include A-1(LSB) for addressing

PIN CONFIGURATIONS

44 SOP(500 mil)



TSOP (TYPE 1) (12mm x 20mm)

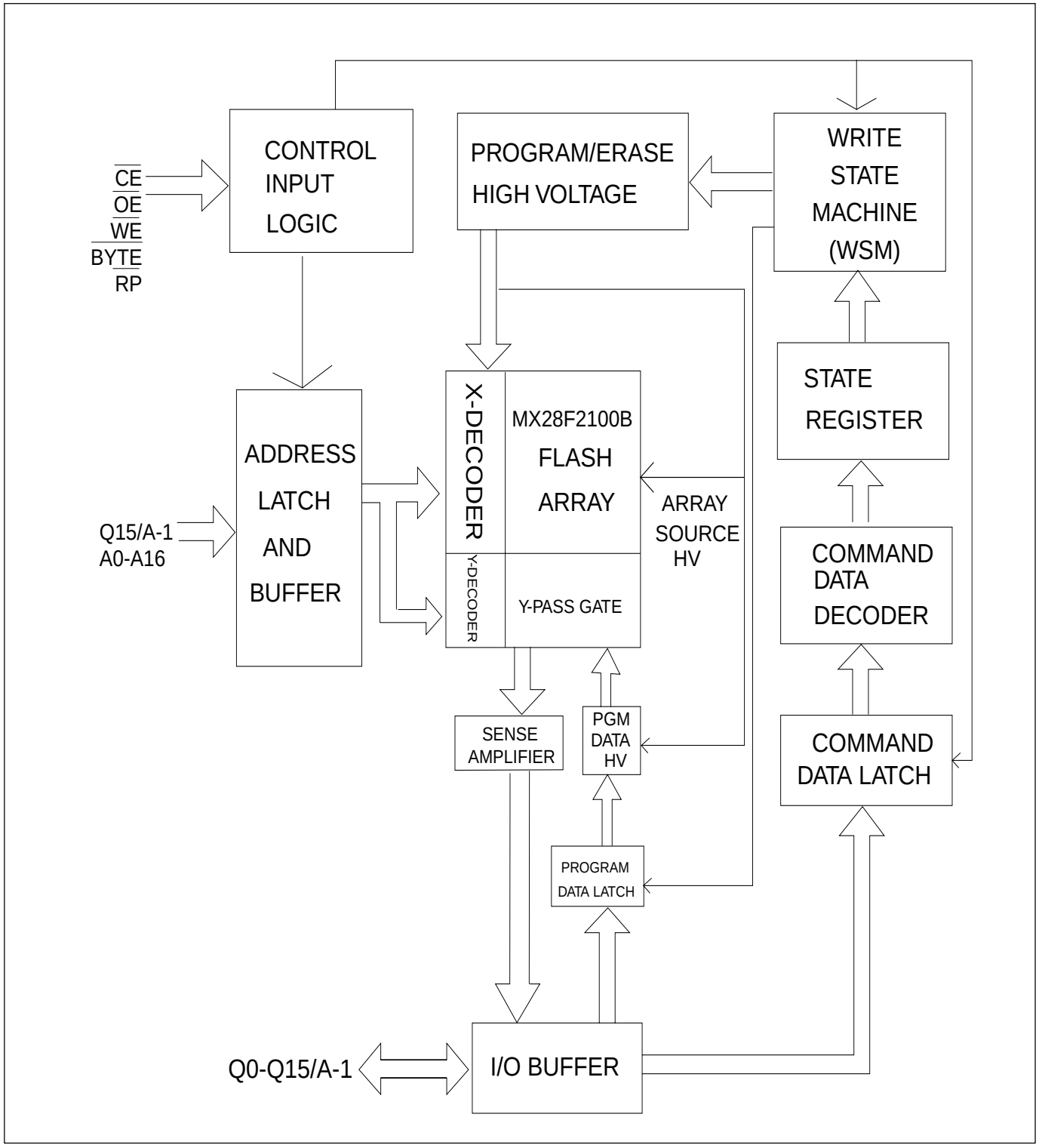


(NORMAL TYPE)

PIN DESCRIPTION:

SYMBOL	PIN NAME
A0~A16	Address Input
Q0~Q14	Data Input/Output
Q15/A-1	Q15(Word mode)/LSB addr(Byte mode)
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{BYTE}$	Word/Byte Selction input
$\overline{RP}$	Reset/Deep Power Down
$\overline{OE}$	Output Enable Input
VPP	Power supply for Program and Erase
VCC	Power Supply Pin (+5V)
GND	Ground Pin

BLOCK DIAGRAM



AUTOMATIC PROGRAMMING

The MX28F2100B is byte/word programmable using the Automatic Programming algorithm. The Automatic Programming algorithm does not require the system to time out or verify the data programmed. The typical room temperature chip programming time of the MX28F2100B is less than 5 seconds.

AUTOMATIC CHIP ERASE

The entire chip is bulk erased using 10 ms erase pulses according to MXIC's High Reliability Chip Erase algorithm. Typical erasure at room temperature is accomplished in less than five seconds. The device may also be erased using the Automatic Erase algorithm. The Automatic Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are controlled internally.

AUTOMATIC BLOCK ERASE

The MX28F2100B is block(s) erasable using MXIC's Auto Block Erase algorithm. Block erase modes allow one of 5 blocks of the array to be erased in one erase cycle. The Automatic Block Erase algorithm automatically programs the specified block(s) prior to electrical erase. The timing and verification of electrical erase are controlled internal to the device.

AUTOMATIC PROGRAMMING ALGORITHM

MXIC's Automatic Programming algorithm requires the user to only write a program set-up command and a program command (program data and address). The device automatically times the programming pulse width, provides the program verify, and counts the number of sequences. A status register scheme provides feedback to the user as to the status of the programming operation.

AUTOMATIC ERASE ALGORITHM

MXIC's Automatic Erase algorithm requires the user to only write an Erase Set-up command and an Erase command. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verify, and counts the number of sequences. A status register provides feedback to the user as to the status of the erase operation. It is noted that after an Erase Set-up command, if the next command is not an Erase command, then the state-machine will set both the program status and Erase Status bits of the Status Register to a "1", place the device into the read Status Register state, and wait for another command.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. During a system write cycle, addresses are latched on the falling edge, and data is latched on the rising edge of WE .

MXIC's Flash technology combines years of EPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MX28F2100B electrically erases all bits within a sector or chip simultaneously using Fowler-Nordheim tunneling. The array is programmed one byte/word at a time using the EPROM programming mechanism of hot electron injection.

During a program cycle, the state-machine will control the program sequences and command register will not respond to any command set. During a Sector/Chip Erase cycle, the command register will respond to Erase Suspend command. After Erase Suspend completed, the device stays at status register Read state. After the state machine has completed its task, it will allow the command register to respond to its full command set.

TABLE 1. SOFTWARE COMMAND DEFINITIONS

COMMAND	BUS CYCLE	FIRST BUS CYCLE				SECOND BUS CYCLE			
		Mode	Address	Data		Mode	Address	Data	
				X8	X16			X8	X16
Read Memory Array	1	Write	X	FFH	XXFFH	---	---	---	---
Setup Auto program/ Auto Program	2	Write	X	10H or 40H	XX10H or XX40H	Write	Program Address	Program Data	Program Data
Setup Erase/Erase(Chip)	2	Write	X	20H	XX20H	Write	X	20H	XX20H
Setup Erase/Erase(Block)	2	Write	X	60H	XX60H	Write	Block Address	60H	XX60H
Setup Auto Erase/ Auto Erase(Chip)	2	Write	X	30H	XX30H	Write	X	30H	XX30H
Setup Auto Erase/ Auto Erase(Block)	2	Write	X	20H	XX20H	Write	Block Address	D0H	XXD0H
Erase Verify	2	Write	Verify Address	A0H	XXA0H	Read	X	Verify Data	Verify Data
Read device identifier code	2	Write	X	90H	XX90H	Read	ADI	DDI	DDI
Erase Suspend	1	Write	X	B0H	XXB0H	---	---	---	---
Erase Resume	1	Write	X	D0H	XXD0H	---	---	---	---
Read Status Register	2	Write	X	70H	XX70H	Read	X	SRD	SRD
Clear Status Register	1	Write	X	50H	XX50H	---	---	---	---

Note:
1. Write and Read mode are defined in mode selection table.
2. ADI = Address of Device identifier; A0 = 0 for manufacture code, A0 = 1 for device code.
   DDI = Data of Device identifier : C2H for manufacture code, 2BH for device code(Byte = VIL) ; 00C2H for manufacture code, 002BH for device code(Byte =VIH)
   X = X can be VIL or VIH
   SRD = Status Register Data

COMMAND DEFINITIONS

Placing high voltage on the VPP pin enables read/write operations. Device operations are selected by writing specific data patterns into the command register. Table 1 defines these MX28F2100B register commands. Table 2 defines the bus operations of MX28F2100B.

TABLE 2. MX28F2100B BUS OPERATION

Mode \ Pins			A0	A9	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	VPP	Data I/O		
									D0~D7	D8~D14	D15/A-1
Byte Mode $\overline{BYTE}$ = L	Read-Only	Read	A0	A9	VIL	VIL	VIH	VPPL	Data Out	Hi-Z	A-1
		Output Disable	X	X	VIL	VIH	VIH	VPPL	Hi-Z	Hi-Z	X
		Standby	X	X	VIH	X	X	VPPL	Hi-Z	Hi-Z	X
		Read Silicon ID(Mfr)(2)	VIL	VID(3)	VIL	VIL	VIH	VPPL	Data=C2H	Hi-Z	VIL
		Read Silicon ID(Device)(2)	VIH	VID(3)	VIL	VIL	VIH	VPPL	Data=2BH	Hi-Z	VIL
	Read/Write	Read	A0	A9	VIL	VIL	VIH	VPPH	Data Out(4)	Hi-Z	A-1
		Output Disable	X	X	VIL	VIH	VIH	VPPH	Hi-Z	Hi-Z	X
		Standby(5)	X	X	VIH	X	X	VPPH	Hi-Z	Hi-Z	X
		Write	A0	A9	VIL	VIH	VIL	VPPH	Data In(6)	X	A-1
Word Mode $\overline{BYTE}$ = H	Read-Only	Read	A0	A9	VIL	VIL	VIH	VPPL	Data Out	Data Out	Data Out
		Output Disable	X	X	VIL	VIH	VIH	VPPL	Hi-Z	Hi-Z	Hi-Z
		Standby	X	X	VIH	X	X	VPPL	Hi-Z	Hi-Z	Hi-Z
		Read Silicon ID(Mfr)(2)	VIL	VID(3)	VIL	VIL	VIH	VPPL	Data=C2H	Data=00H(8)	0B
		Read Silicon ID(Device)(2)	VIH	VID(3)	VIL	VIL	VIH	VPPL	Data=2BH	Data=00H(8)	0B
	Read/Write	Read	A0	A9	VIL	VIL	VIH	VPPH	Data Out(4)	Data Out	Data Out
		Output Disable	X	X	VIL	VIH	VIH	VPPH	Hi-Z	Hi-Z	Hi-Z
		Standby(5)	X	X	VIH	X	X	VPPH	Hi-Z	Hi-Z	Hi-Z
		Write	A0	A9	VIL	VIH	VIL	VPPH	Data In(6)	Data In(6)	Data In(6)

NOTES:

1. VPPL may be grounded, a no-connect with a resistor tied to ground, or ≤ VCC + 2.0V. VPPH is the programming voltage specified for the device. When VPP = VPPL, memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 1. All other addresses are low.
3. VID is the Silicon-ID-Read high voltage, 11.5V to 13V.
4. Read operations with VPP = VPPH may access array data or Silicon ID codes.
5. With VPP at high voltage, the standby current equals ICC + IPP (standby).
6. Refer to Table 1 for valid Data-In during a write operation.
7. X can be VIL or VIH.
8. Includes D15

TABLE 3. SILICON ID CODE

Code \ Pins		A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Code(Hex)
$\overline{BYTE}$ = L	Manufacture code	VIL	VIL	---	---	---	---	---	---	---	1	1	0	0	0	0	1	0	C2H
	Device code	VIH	VIL	---	---	---	---	---	---	---	0	0	1	0	1	0	1	1	2BH
$\overline{BYTE}$ = H	Manufacture code	VIL	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	00C2H
	Device code	VIH	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	002BH

READ COMMAND

While V_{PP} is high, for erasure and programming, memory contents can also be accessed via the Read command. The read operation is initiated by writing XXFFH into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

RESET COMMAND

A Reset command is provided as a means to safely abort the erase- or program-command sequences. Following Set-up command with two consecutive writes of XXFFH for ERS (or one write of XXFFH for PGM) will safely abort the operation. Memory contents will not be altered. A valid command must then be written to place the device in the desired state.

SILICON-ID-READ COMMAND

Flash-memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer- and device-codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not a desired system-design practice.

The MX28F2100B contains a Silicon-ID-Read operation to supplement traditional PROM-programming methodology. The operation is initiated by writing XX90H into the command register. Following the command write, a read cycle with A0=VIL retrieves the manufacturer code of C2H(BYTE=VIL, 00C2H(BYTE=VIH). A read cycle with A0=VIH returns the device code of 2BH(BYTE = VIL), 002BH(BYTE = VIH).

ERASE-VERIFY COMMAND

After each erase operation, all bytes must be verified. The Erase Verify operation is initiated by writing XXA0H into the command register. The address for the byte to be verified must be supplied as it is latched on the falling edge of the WE pulse.

The MX28F2100B applies an internally generated margin voltage to the addressed byte. Reading FFFFH from the addressed byte indicates that all bits in the byte are erased.

The Erase-Verify command must be written to the command register prior to each byte verification to latch its address. The process continues for each byte in the array until a byte does not return FFFFH data, or the last address is accessed.

In the case where the data read is not FFFFH, another erase operation needs to be performed. (Refer to Set-up Erase/Erase). Verification then resumes from the address of the last-verified byte. Once all bytes in the array have been verified, the erase step is complete. The device can be programmed. At this point, the verify operation is terminated by writing a valid command (e.g. Program Set-up) to the command register. The High Reliability Erase algorithm illustrates how commands and bus operations are combined to perform electrical erasure of the MX28F2100B.

SET-UP AUTOMATIC CHIP ERASE/ERASE COMMANDS

The Automatic Chip Erase does not require the device to be entirely pre-programmed prior to excuting the Automatic Set-up Erase command and Automatic Chip Erase command. Upon executing the Automatic Chip Erase command, the device automatically will program and verify the entire memory for an all-zero data pattern. When the device is automatically verified to contain an all-zero pattern, a self-timed chip erase and verify begin. The erase and verify operations are completed by the feed back of the status register. The system is not required to provide any control or timing during these operations.

When using the Automatic Chip Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array(no erase verify command is required). The margin voltages are internally generated in the same manner as when the standard Erase Verify command is used.

If the Erase operation was unsuccessful, bit 5 of the Status Register will be set to a "1", indicating an Erase Failure. If Vpp was not within acceptable limits after the Erase command is issued, the state machine will not execute an erase sequence; in stead, bit 5 of the Status Register is set to a "1" to indicate an Erase Failure, and bit 3 is set to a "1" to indentify that Vpp supply voltage was not within acceptable limits.

The Automatic Set-up Erase command is a command only operation that stages the device for automatic electrical erasure of all bytes in the array. Automatic set-up erase is performed by writing XX30H to the command register.

To commence Automatic Chip Erase, the command XX30H must be written again to the command register.

SET-UP AUTOMATIC BLOCK ERASE/ERASE COMMANDS

The Automatic Block Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Set-up Block Erase command and Automatic Block Erase command. Upon executing the Automatic Block Erase command, the device automatically will program and verify the block(s) memory for an all-zero data pattern. The system is not required to provide any controls or timing during these operations.

When the block(s) is automatically verified to contain an all-zero pattern, a self-timed block erase and verify begin. The system is not required to provide any control or timing during these operations.

When using the Automatic Block Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verify command is required). The margin voltages are internally generated in the same manner as when the standard Erase Verify command is used. The Automatic Set-up Block Erase command is a command only operation that stages the device for automatic electrical erasure of selected blocks in the array. Automatic Set-up Block Erase is performed by writing XX20H to the command register. To enter Automatic Block Erase, the user must write the command D0H to the command register. Block addresses selected are loaded into internal register on the second falling edge of $\overline{WE}$. Each successive block load cycle started by the falling edge of $\overline{WE}$ must begin within 30us from the rising edge of the preceding $\overline{WE}$. Otherwise, the loading period ends and internal auto block erase cycle starts.

ERASE SUSPEND

This command only has meaning while the state machine is executing Automatic Chip/Block Erase operation, and therefore will only be responded to during Automatic Chip/Block Erase operation. It is noted that Erase Suspend is meaningful for block erase only after block addresses load are finished (100 us after the last address is loaded). After this command has been executed, the command register will initiate erase suspend mode. The state machine will set DQ7, DQ6 as 1, 1, after suspend is ready. At this time, state machine only allows the command register to respond to the Read Memory Array, Erase Resume and Read Status Register.

ERASE RESUME

This command will cause the command register to clear the suspend state and set DQ6, DQ7, back to 0, 0, but only if an Erase Suspend command was previously issued. Erase Resume will not have any effect in all other conditions.

SET-UP AUTOMATIC PROGRAM/PROGRAM COMMANDS

The Automatic Set-up Program is a command only operation that stages the device for automatic programming. Automatic Set-up Program is performed by writing XX10H/XX40H to the command register. Program command is the command for byte-program or word-program.

Once the Automatic Set-up Program operation is performed, the next $\overline{WE}$ pulse causes a transition to an active programming operation. Addresses are latched on the falling edge, and data are internally latched on the rising edge of the $\overline{WE}$ pulse. The rising edge of $\overline{WE}$ also begins the programming operation. The system is not required to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin.

If the program opetation was unsuccessful, bit 4 of the Status Register will be set to a "1", indicating a program failure. If Vpp was not within acceptable limits after the program command is issued, the state machine will not execute a program sequence; in stead, bit 4 of the Status Register is set to a "1" to indicate a Program Failure, and bit 3 is set to a "1" to identify that Vpp supply voltage was not within acceptable limits.

STATUS REGISTER

The device contains a Status Register which may be read to determine when a Program or Erase operation is complete, and whether that operation completed successfully. The Status Register may be read at any time by writing the Read Status command to the command interface. After writing this command, all subsequent Read operations output data from the Status Register until another command is written to the command interface. A Read Array command must be written to the command interface to return to the read array mode.

The Status Register bits are output on DQ[0:7], whether the device is in the byte-wide (x8) or word-wide (x16) mode. In the word-wide mode the upper byte, DQ[8:15], is set to 00H during a Read Status command. In the byte-wide mode, DQ[8:14] are tri-stated and DQ15/A-1 retains the low order address function.

The contents of the Status Register are latched on the falling edge of $\overline{OE}$ or $\overline{CE}$, whichever occurs last in the read cycle. This prevents possible bus errors which might occur if the contents of the Status Register change while reading the Status Register. $\overline{CE}$ or $\overline{OE}$ must be toggled with each subsequent status read, or the completion of a Program or Erase operation will not be evident from the Status Register.

When the state machine is active, this register will indicate the status of the state machine, and will also hold the bits indicating whether or not the state machine was successful in performing the desired operation.

CLEARING THE STATUS REGISTER

The state machine sets status bits "3" through "7" to "1", and clears bits "6" and "7" to "0", but cannot clear status bits "3" through "5" to "0". Bits 3 through 5 can only be cleared by the controlling CPU through the use of the Clear Status Register command. These bits can indicate various error conditions. By allowing the system software to control the resetting of these bits, several operations may be performed (such as cumulatively programming several bytes or erasing multiple blocks in sequence). The Status Register may then be read to determine if an error occurred during that programming or erasure series. This adds flexibility to the way the device may be programmed or erased. Once an error occured, the command Interface Only responds to clear Status Register, Read Status Register and Read Array. To clear the Status Register, the Clear Status Register command is written to the command interface. Then, any other command may be issued to the command interface. Note, again, that before read cycle can be initiated, a Read Array command must be written to the command interface to specify whether the read data is to come from the Memory Array, Status Register, or Sili-con -ID.

Status Register Bit Definition

WSMS	ESS	ES	PS	VPPS
7	6	5	4	3

SR.7 = WRITE STATE MACHINE STATUS(WSMS)
1 = Ready
0 = Busy

SR.6 = ERASE-SUSPEND STATUS (ESS)
1 = Erase Suspended
0 = Erase in Progress/Completed

SR.5 = ERASE STATUS
1 = Error in Erase
0 = Successful Erasure

SR.4 = PROGRAM STATUS
1 = Error in Byte/Word Program
0 = Successful Byte/Word Program

SR.3 = Vpp STATUS
1 = Vpp Low Detect, Operation Abort
0 = Vpp OK

NOTE :
State machine bit must first be checked to determine Byte/Word program or Block Erase completion, before the Program or Erase Status bits are checked for success. When Erase Suspend is issued, state machine halts execution and sets both WSMS and ESS bits to "1," ESS bit remains set to "1" until an Erase Resume command is issued.

When this bit set to "1," state machine has applied the maximum number of erase pulses to the device and is still unable to successfully verify erasure.

When this bit is set to "1," state machine has attempted but failed to program a byte or word.

The Vpp status bit, unlike an A/D converter, does not provide continuous indication of Vpp level. The state machine interrogates Vpp level only after the Byte Write or Erase command sequences have been entered, and informs the system if Vpp has not been switched on.

DATA PROTECTION

The MX28F2100B is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

LOW VPP WRITE INHIBIT

To avoid initiation of a write cycle during V_{PP} power-up and power-down a write cycle is locked out for V_{PP} less than V_{PPLK}(typically 9V). If $V_{PP} < V_{PPLK}$, the command register is disabled and all internal program/erase circuits are disabled. Subsequent writes will be ignored until the V_{PP} level is greater than V_{PPLK}. It is the user's responsibility to ensure that the control pins are logically correct to prevent unintentional write when V_{PP} is above V_{PPLK}.

WRITE PULSE "GLITCH" PROTECTION

Noise pulses of less than 5ns(typical) on $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

LOGICAL INHIBIT

Writing is inhibited by holding any one of $\overline{OE}$ = VIL, $\overline{CE}$ = VIH or WE = VIH. To initiate a write cycle CE and WE must be a logical zero while OE is a logical one.

POWER SUPPLY DECOUPLING

In order to reduced power switching effect, each device should have a 0.1uF ceramic capacitor connected between its VCC and GND, and between its VPP and GND.

VPP TRACE ON PRINTED CIRCUIT BOARD

Programming flash memories, while they reside in the target system, requires that the printed circuit board designer pay attention to the Vpp power supply trace. The Vpp pin supplies the memory cell current for programming. Use similar trace widths and layout considerations given to the Vcc power bus. Adequate Vpp supply traces and decoupling will decrease Vpp voltage spikes and overshoots.

DEEP POWER DOWN MODE

This mode is enabled by $\overline{RP}$ pin. During Read modes, $\overline{RP}$ going low deselects the memory and place the output drivers in a high-Z state.

In erase or program modes, $\overline{RP}$ low will abort erase or program operations, but the memory contents are no longer valid as the data has been corrupted by $\overline{RP}$ function. $\overline{RP}$ transition to VIL, or turning power off to the device will clear up Status Register and automatically defaults to the read array mode.

POWER-UP SEQUENCE

The MX28F2100B powers up in the Read only mode. In addition, the memory contents may only be altered after successful completion of a two-step command sequence. Vpp and Vcc power up sequence is not required.

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to 7.0V
VCC to Ground Potential	-0.5V to 7.0V
A9 & VPP & $\overline{RP}$	-0.5V to 13.5V

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

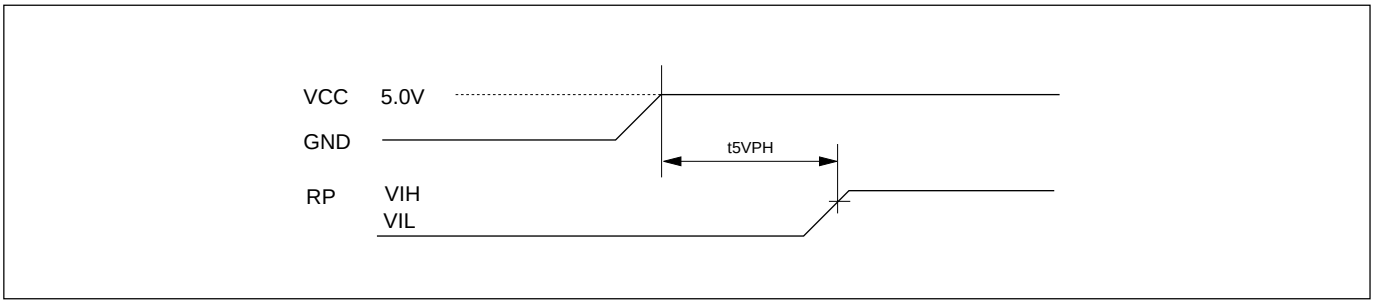
SWITCHING VCC VOLTAGES

VCC SUPPLY SWITCHING TIMING

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T5VPH	VCC at 4.5V (minimum) to $\overline{RP}$ High	3		ms

NOTICE:
The T5VPH time must be strictly followed to guarantee all other read and write specifications.

VCC SUPPLY SWITCHING WAVEFORM



CAPACITANCE TA = 25°C, f = 1.0 MHz

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance			8	pF	VIN = 0V
COUT	Output Capacitance			12	pF	VOUT = 0V

READ OPERATION

DC CHARACTERISTICS TA = 0°C TO 70°C, VCC = 5V ± 10%, VPP = GND to VCC

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
ILI	Input Leakage Current			1	uA	VIN = GND to VCC
ILO	Output Leakage Current			10	uA	VOUT = GND to VCC
IPP1	VPP Current		1	100	uA	VPP = 5.5V
ISB1	Standby VCC current			1	mA	$\overline{CE}$ = VIH
ISB2			1	100	uA	$\overline{CE}$ = VCC + 0.3V
ICC1	Operating VCC current			50	mA	IOUT = 0mA, f=1MHz
ICC2				70	mA	IOUT = 0mA, f=10MHz
VIL	Input Low Voltage	-0.3(NOTE 1)		0.8	V	
VIH	Input High Voltage	2.0		VCC + 0.3	V	
VOL	Output Low Voltage			0.45	V	IOL = 2.1mA
VOH	Output High Voltage	2.4			V	IOH = -400uA

NOTES:

1. VIL min. = -1.0V for pulse width ≤ 50 ns.
   VIL min. = -2.0V for pulse width ≤ 20 ns.
2. VIH max. = VCC + 1.5V for pulse width ≤ 20 ns
   If VIH is over the specified maximum value, read operation cannot be guaranteed.

AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%, VPP = GND to VCC

		28F2100B-70		28F2100B-90		28F2100B-12			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tACC	Address to Output Delay		70		90		120	ns	$\overline{CE}$=$\overline{OE}$=VIL
tCE	$\overline{CE}$ to Output Delay		70		90		120	ns	$\overline{OE}$=VIL
tOE	$\overline{OE}$ to Output Delay		30		40		50	ns	$\overline{CE}$=VIL
tDF	$\overline{OE}$ High to Output Float (Note1)	0	20	0	30	0	30	ns	$\overline{CE}$=VIL
tOH	Address to Output hold	0		0		0		ns	$\overline{CE}$=$\overline{OE}$=VIL

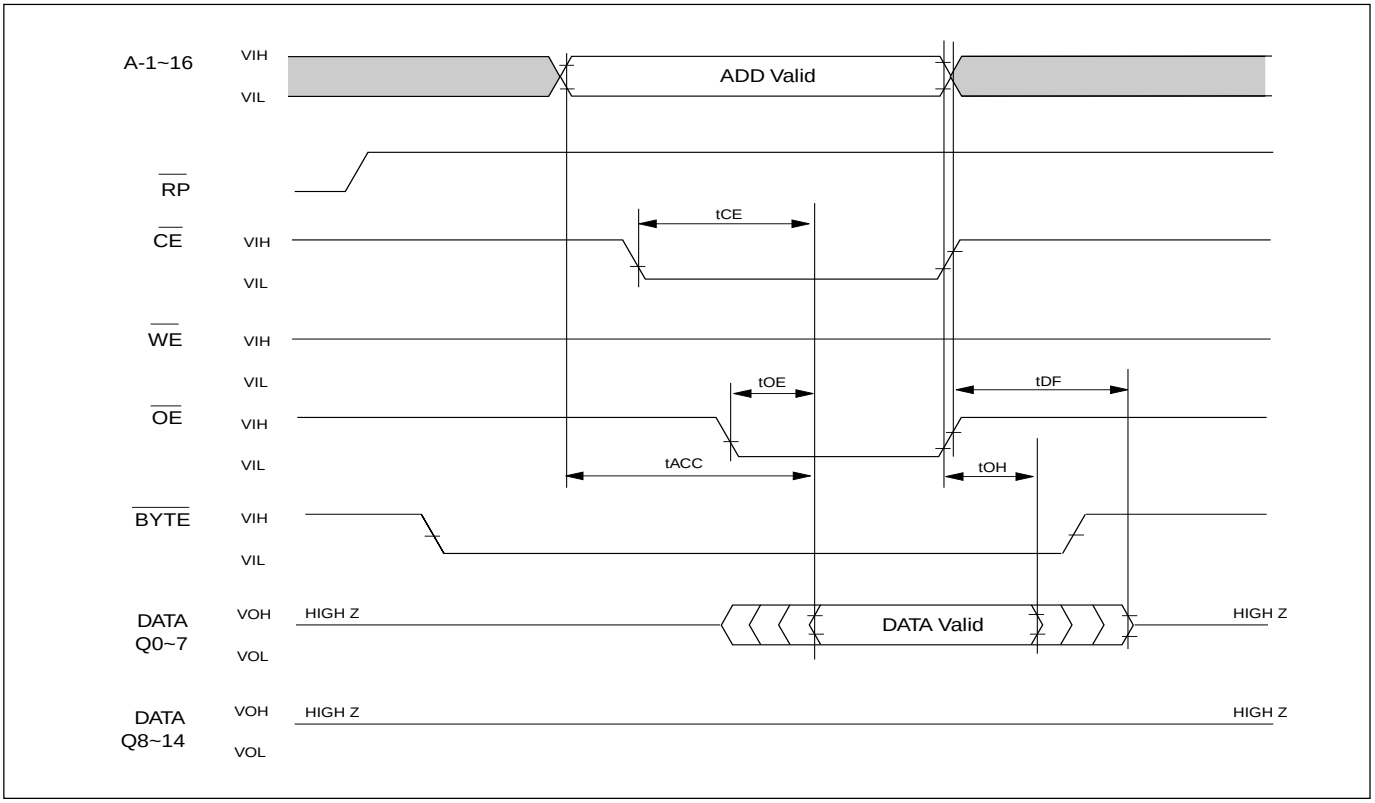
TEST CONDITIONS:

- Input pulse levels: 0.45V/2.4V
- Input rise and fall times: ≤ 10ns
- Output load: 1 TTL gate + 35pF (Including scope and jig)
- Reference levels for measuring timing: 0.8V, 2.0V

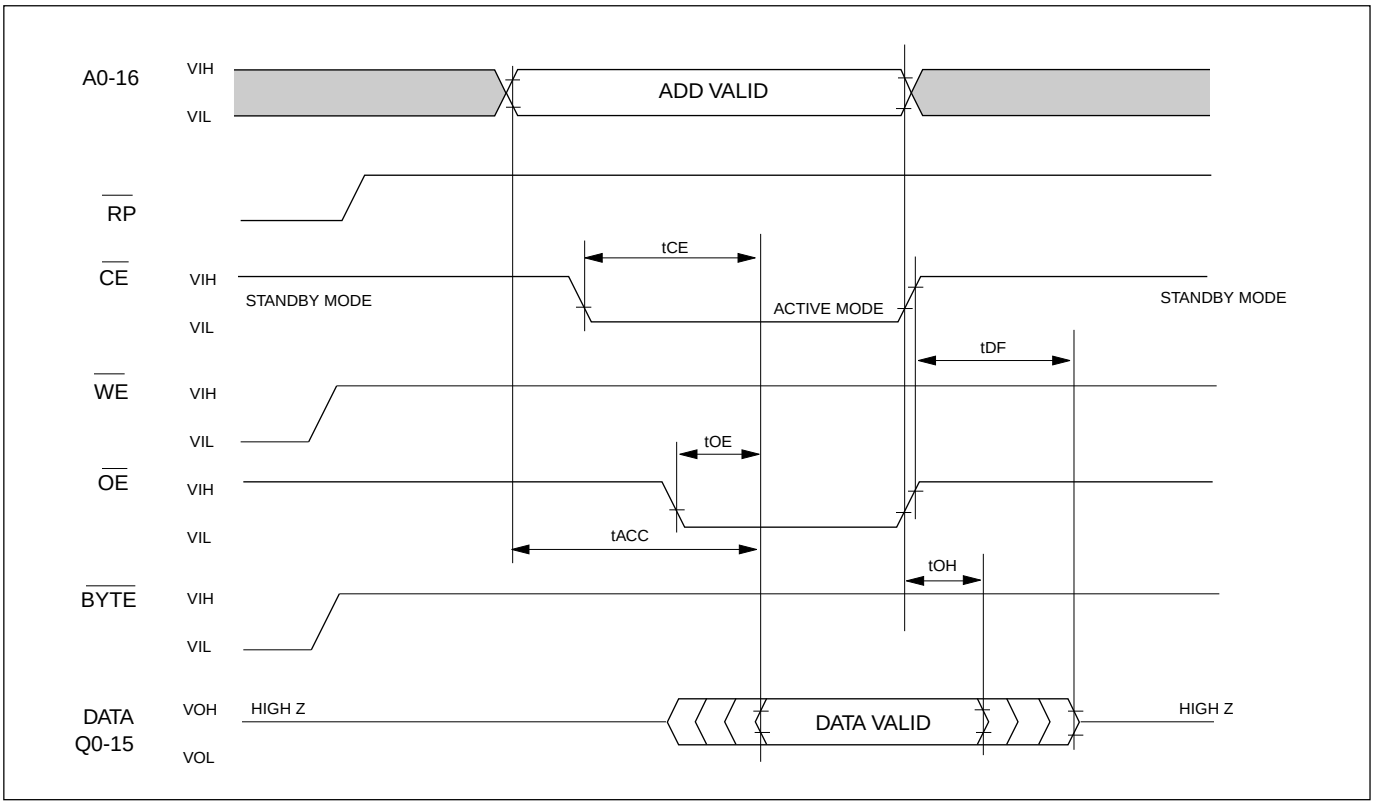
NOTE:

1. tDF is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

BYTE READ TIMING WAVEFORMS



WORD READ TIMING WAVEFORMS



COMMAND PROGRAMMING/DATA PROGRAMMING/ERASE OPERATION

DC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%, VPP = 12V ± 7%

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
ILI	Input Leakage Current			1	uA	VIN=GND to VCC
ILO	Output Leakage Current			10	uA	VOUT=GND to VCC
ISB1	Standby VCC current			1	mA	$\overline{CE}$=VIH
ISB2			1	100	uA	$\overline{CE}$=VCC ± 0.3V
ICC1 (Read)	Operating VCC Current			50	mA	IOUT=0mA, f=1MHz
ICC2				70	mA	IOUT=0mA, F=10MHz
ICC3 (Program)				50	mA	In Programming
ICC4 (Erase)				50	mA	In Erase
ICCES	VCC Erase Suspend Current		10		mA	$\overline{CE}$=VIH, Erase Suspended
IPP1 (Read)	VPP Current			200	uA	VPP=12.8V
IPP2 (Program)				50	mA	In Programming
IPP3 (Erase)				50	mA	In Erase
VIL	Input Voltage	-0.3 (Note 5)		0.8	V	
VIH		2.0		VCC+0.3V (Note 6)	V	
VOL	Output Voltage			0.45	V	IOL=2.1mA
VOH		2.4			V	IOH=-400uA
VPPLK	VPP Lockout Voltage	0.0		6	V	
VPPH	VPP for Program/Erase Operation	11.16		12.84	V	12V ± 7%

NOTES:

1. VCC must be applied before VPP and remove after VPP.
2. VPP must not exceed 14V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while VPP=12V.
4. Do not alter VPP either VIL to 12V or 12V to VIL when $\overline{CE}$=VIL.
5. VIL min. = -0.6V for pulse width ≤ 20ns.
6. If VIH is over the specified maximum value, programming operation cannot be guranteed.
7. ICCES is specified with the device de-selected. If the device is read during erase suspend mode, current draw is the sum of ICCES and ICC1 or ICC2.
8. All current are in RMS unless otherwisw noted.

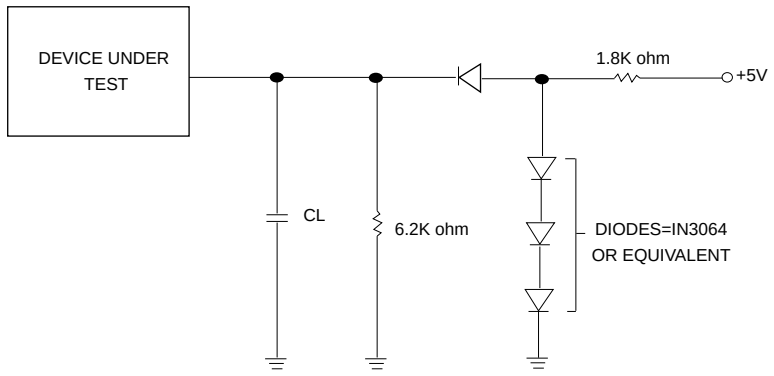
AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%, VPP =12V ± 7%

		28F2100B-70		28F2100B-90		28F2100B-12			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tVPS	VPP setup time	100		100		100		ns	
tPHEL			1000		1000		1000	ns	
tOES	$\overline{OE}$ setup time	100		100		100		ns	
tCWC	Command programming cycle	70		90		120		ns	
tCEP	$\overline{WE}$ programming pulse width	50		50		50		ns	
tCEPH1	$\overline{WE}$ programming pluse width High	20		20		20		ns	
tCEPH2	$\overline{WE}$ programming pluse width High	100		100		100		ns	
tAS	Address setup time	0		0		0		ns	
tAH	Address hold time	45		50		50		ns	
tDS	Data setup time	45		50		50		ns	
tDH	Data hold time	10		10		10		ns	
tCES	$\overline{CE}$ setup time	0		0		0		ns	
tCESC	$\overline{CE}$ setup time before command write	100		100		100		ns	
tCESV	$\overline{CE}$ setup time before verify	6		6		6		us	
tVPH	VPP hold time	100		100		100		ns	
tDF	Output disable time (Note 2)		20		30		30	ns	
tVA	Verify access time		70		90		120	ns	
tAETC	Total erase time in auto chip erase	5(TYP.)		5(TYP.)		5(TYP.)		s	
tAETB	Total erase time in auto block erase	1(TYP.)		1(TYP.)		1(TYP.)		s	
tAVT	Total programming time in auto verify	50	1600	50	1600	50	1600	us	
tET	Standby time in erase	10		10		10		ms	
tBALC	Block address load cycle	0.3	30	0.3	30	0.3	30	us	
tBAL	Block address load time	100		100		100		us	
tCH	$\overline{CE}$ Hold Time	0		0		0		ns	
tCS	$\overline{CE}$ setup to $\overline{WE}$ going low	0		0		0		ns	

NOTES:

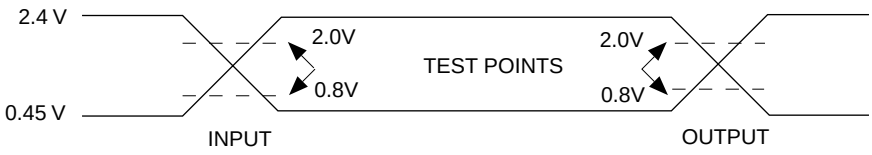
1. $\overline{CE}$ and $\overline{OE}$ must be fixed high during VPP transition from 5V to 12V or from 12V to 5V.
2. tDF defined as the time at which the output achieves the open circuit condition and data is no longer driven.
3. tPHEL: $\overline{RP}$ high recovery to $\overline{CE}$ going low: 500ns, Max 1000ns.

SWITCHING TEST CIRCUITS



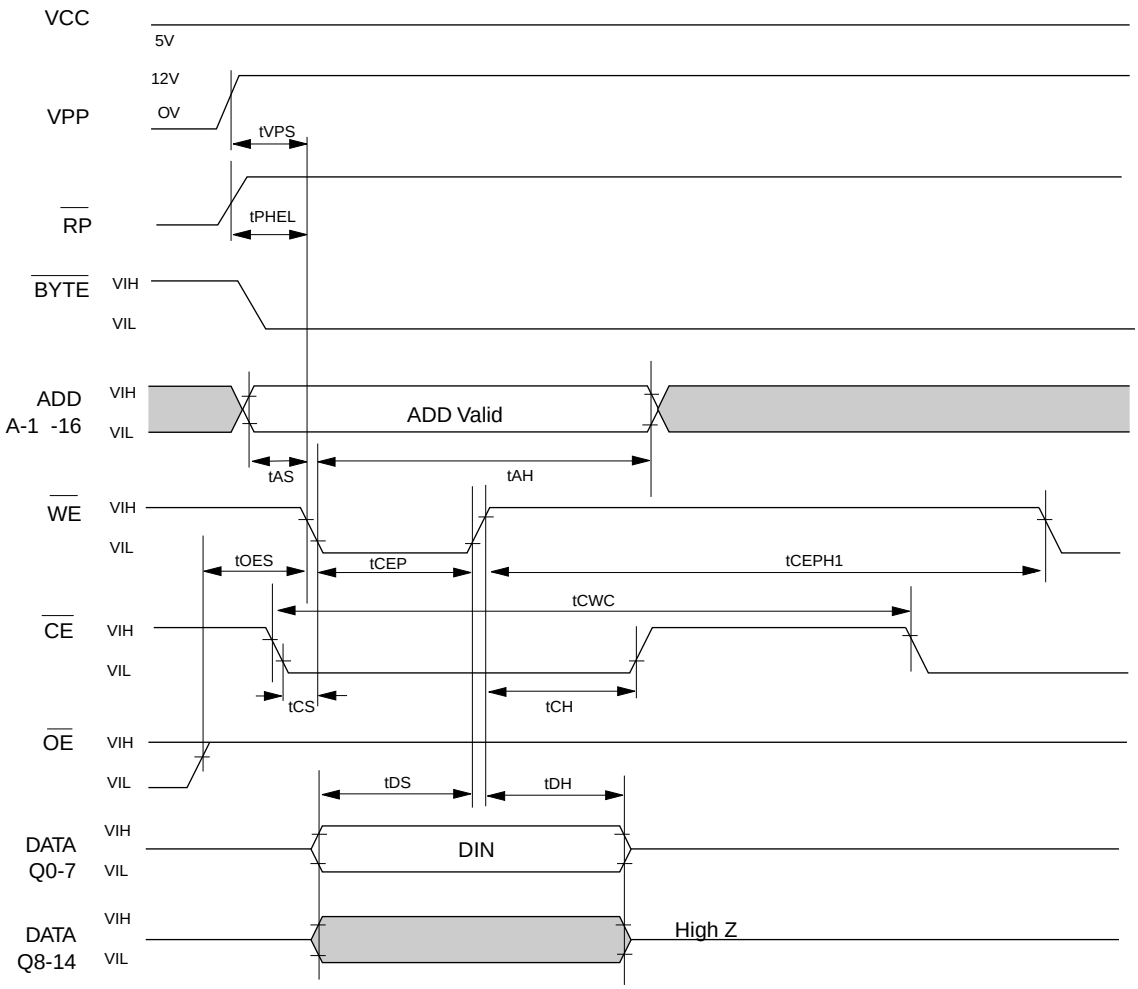
CL=35pF Including jig capacitance

SWITCHING TEST WAVEFORMS



AC TESTING: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
Input pulse rise and fall times are <20ns.

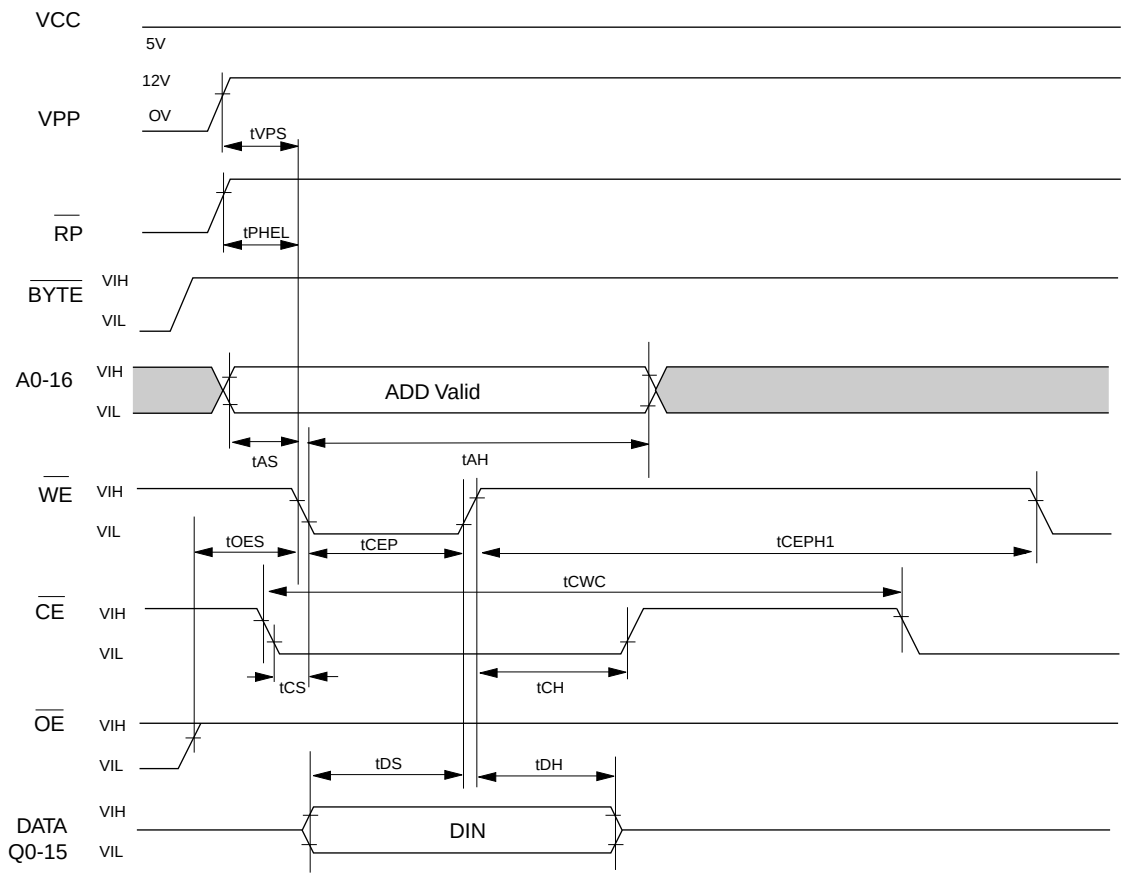
COMMAND WRITE TIMING WAVEFORM-BYTE MODE



NOTE:

$\overline{\text{BYTE}}$ pin is treated as Address pin. All timing specifications for $\overline{\text{BYTE}}$ pin are the same as those for address pin.

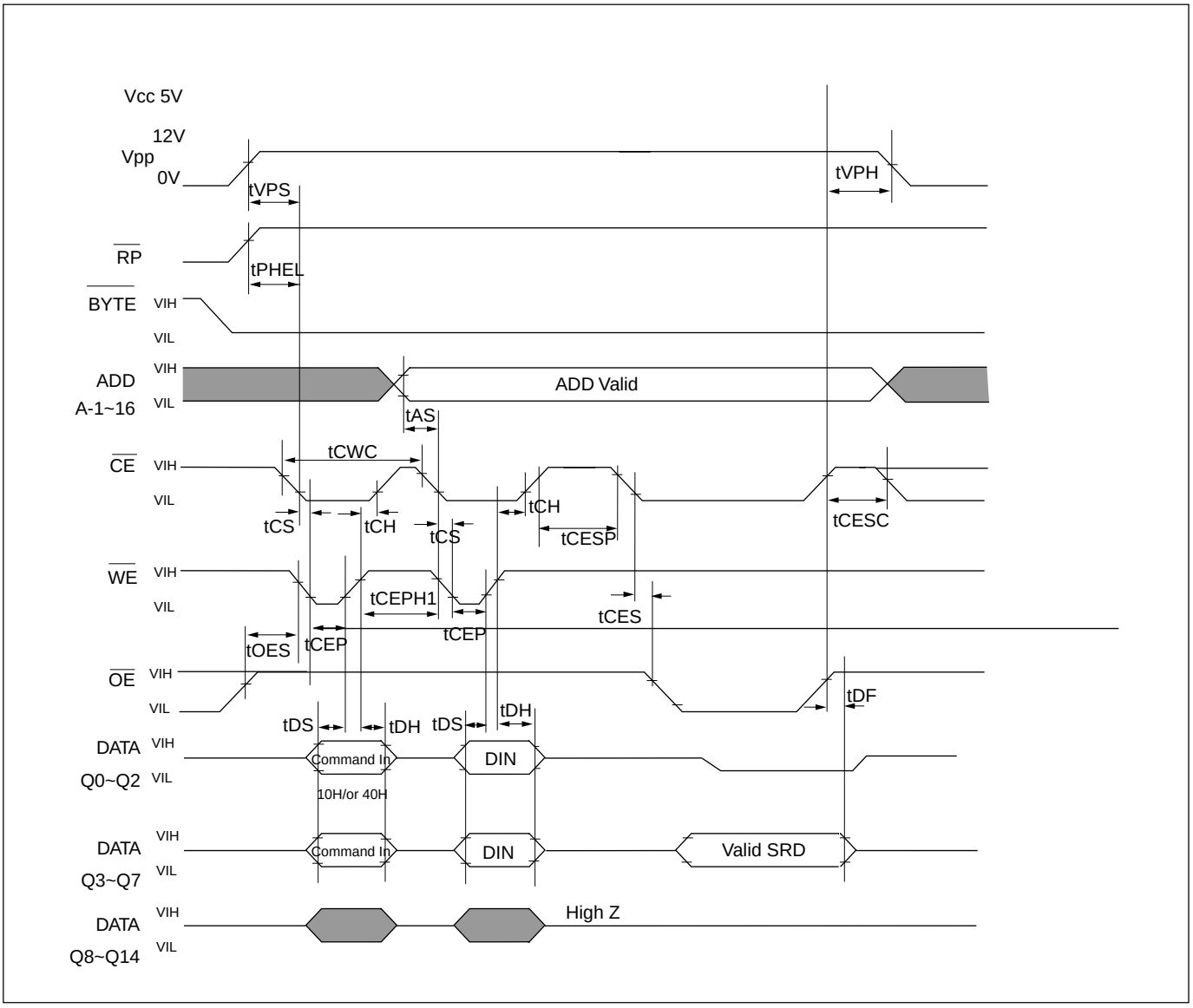
COMMAND WRITE TIMING WAVEFORM-WORD MODE



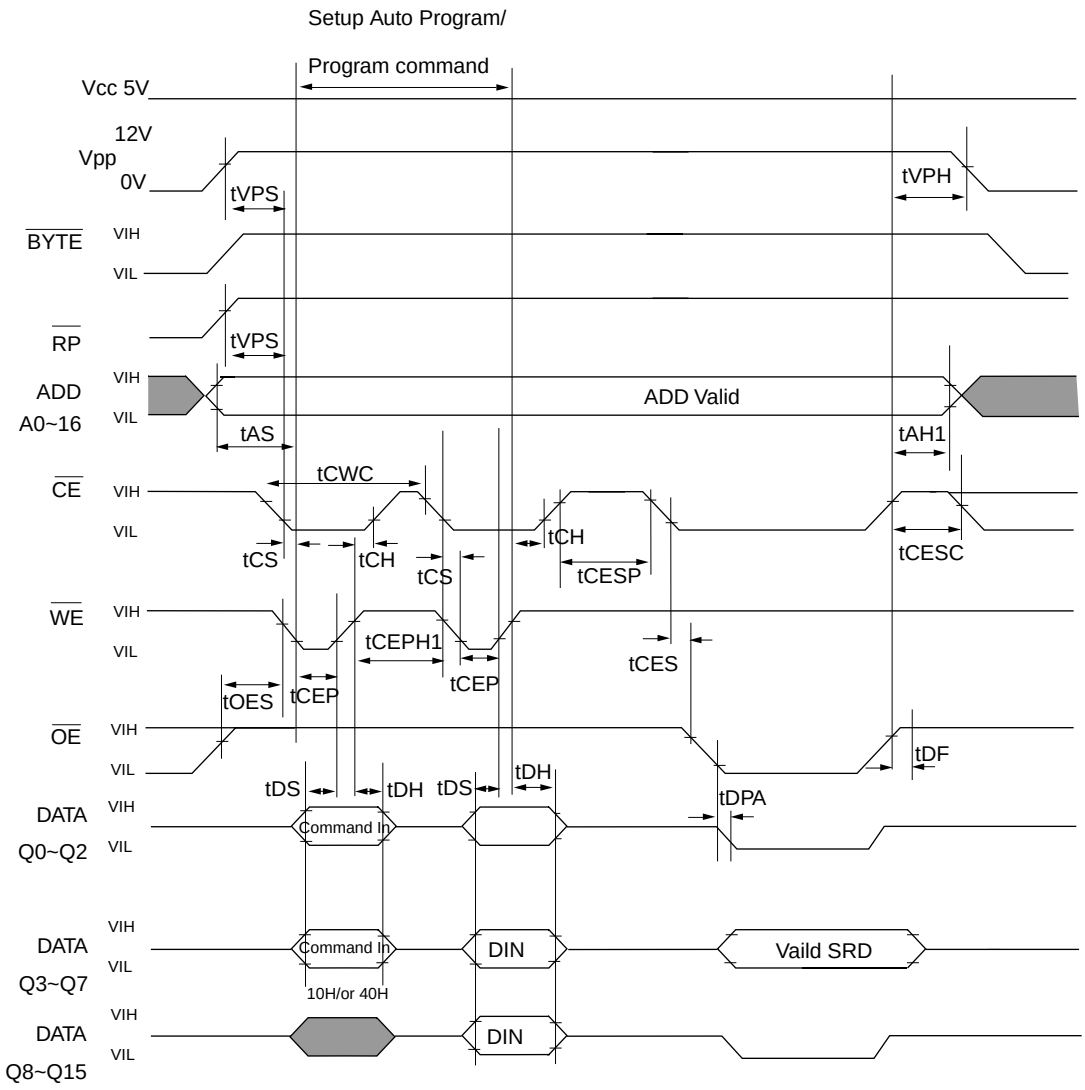
AUTOMATIC PROGRAMMING TIMING WAVEFORM

One byte data is programmed. Verify in fast algorithm and additional programming by external control are not required because these operations are excuted automatically by internal control circuit. Programming completion can be verified by status register after automatic Program starts.

AUTOMATIC PROGRAMMING TIMING WAVEFORM-BYTE MODE

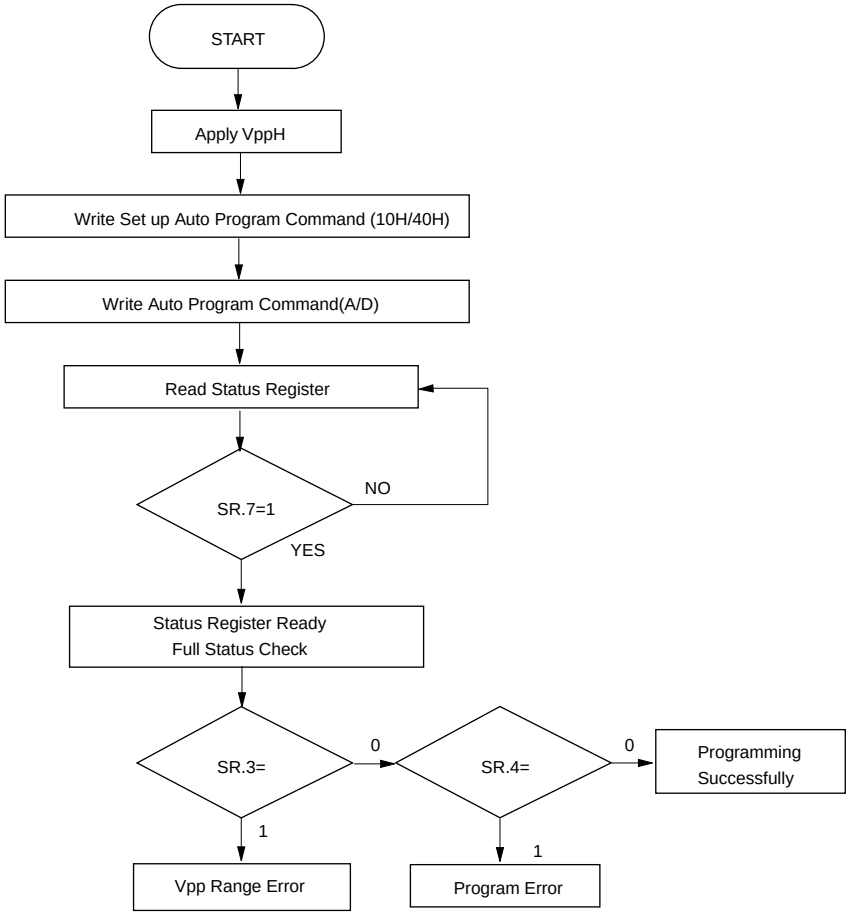


AUTOMATIC PROGRAMMING TIMING WAVEFORM-WORD MODE



AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART

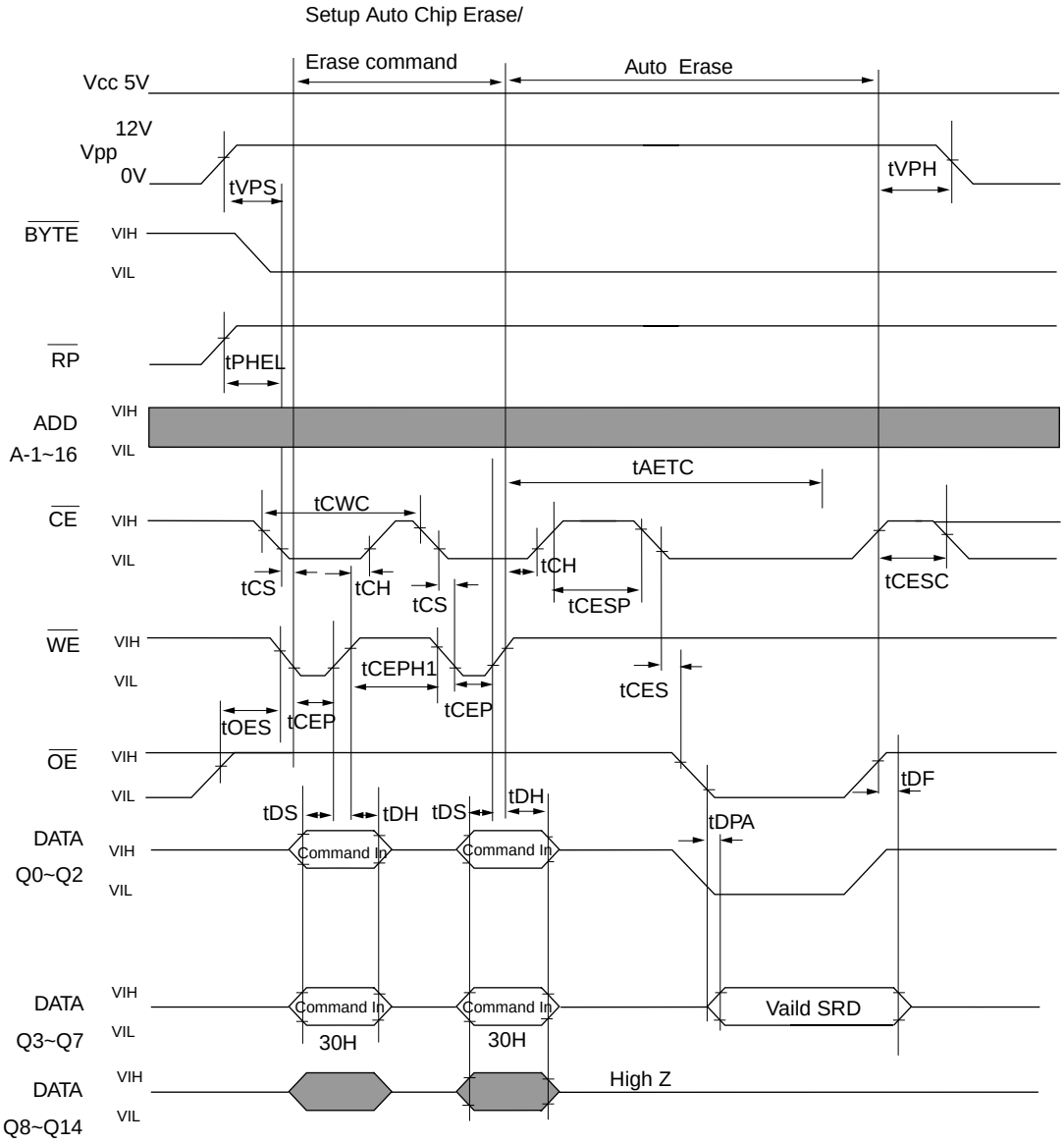
Program Command Sequence (Address/Command)



AUTOMATIC CHIP ERASE TIMING WAVEFORM

All data in chip are erased. External erase verify is not required because data is erased automatically by internal control circuit. Erasure completion can be verified by Status register contents after automatic erase starts.

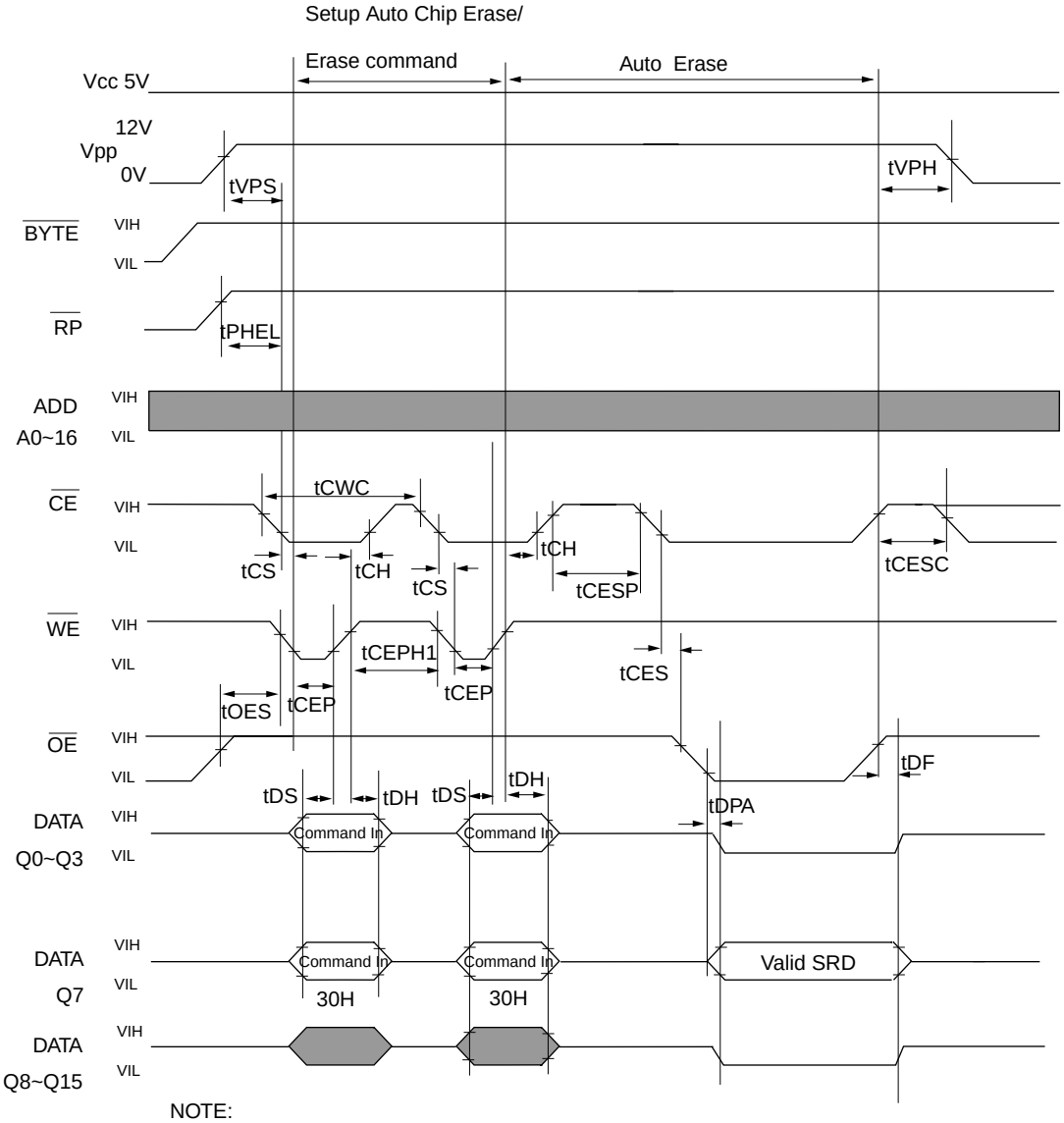
AUTOMATIC CHIP ERASE TIMING WAVEFORM-BYTE MODE



NOTE:

Erase Suspend and Read Array modes are not included in this waveform.

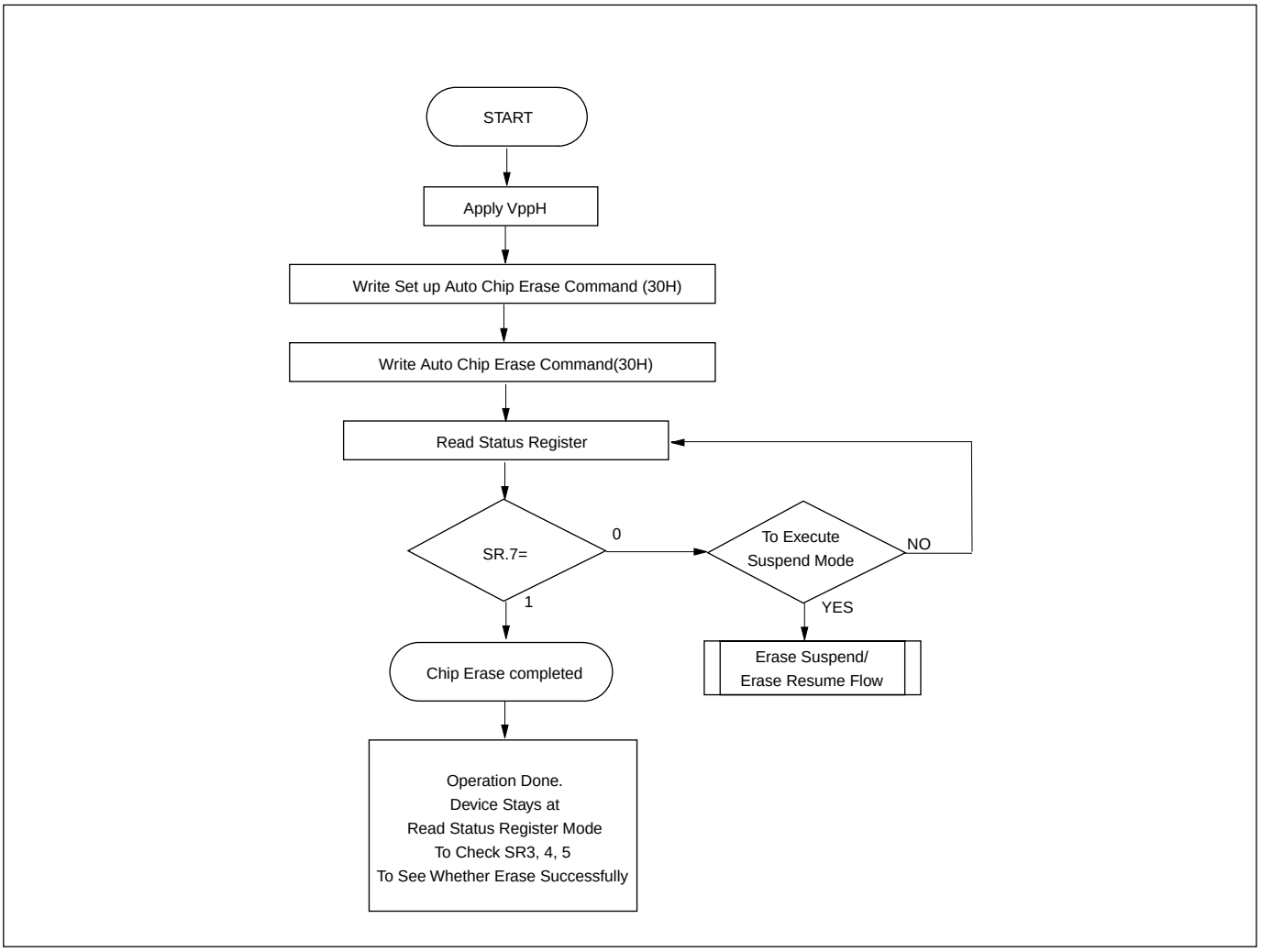
AUTOMATIC CHIP ERASE TIMING WAVEFORM-WORD MODE



NOTE:

Erase Suspend and Read Array modes are not included in this waveform.

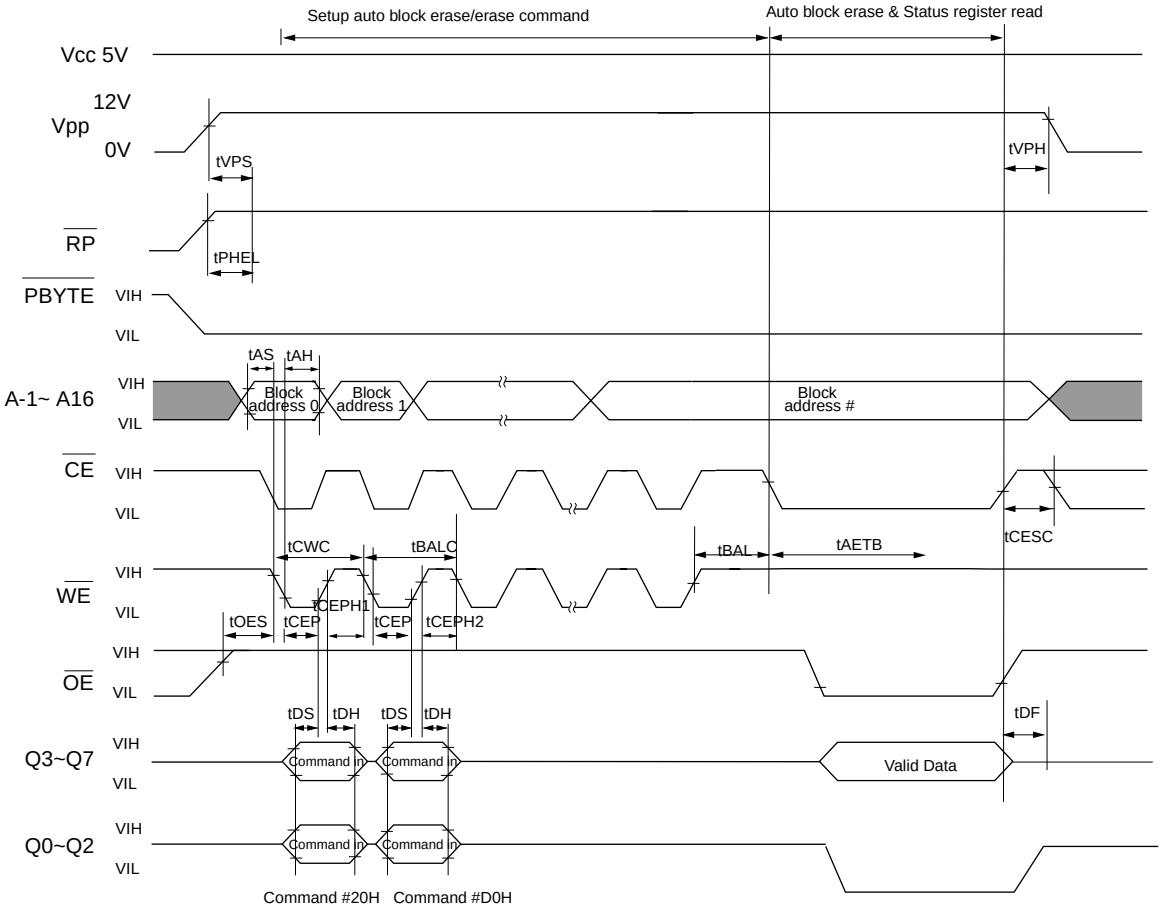
AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART



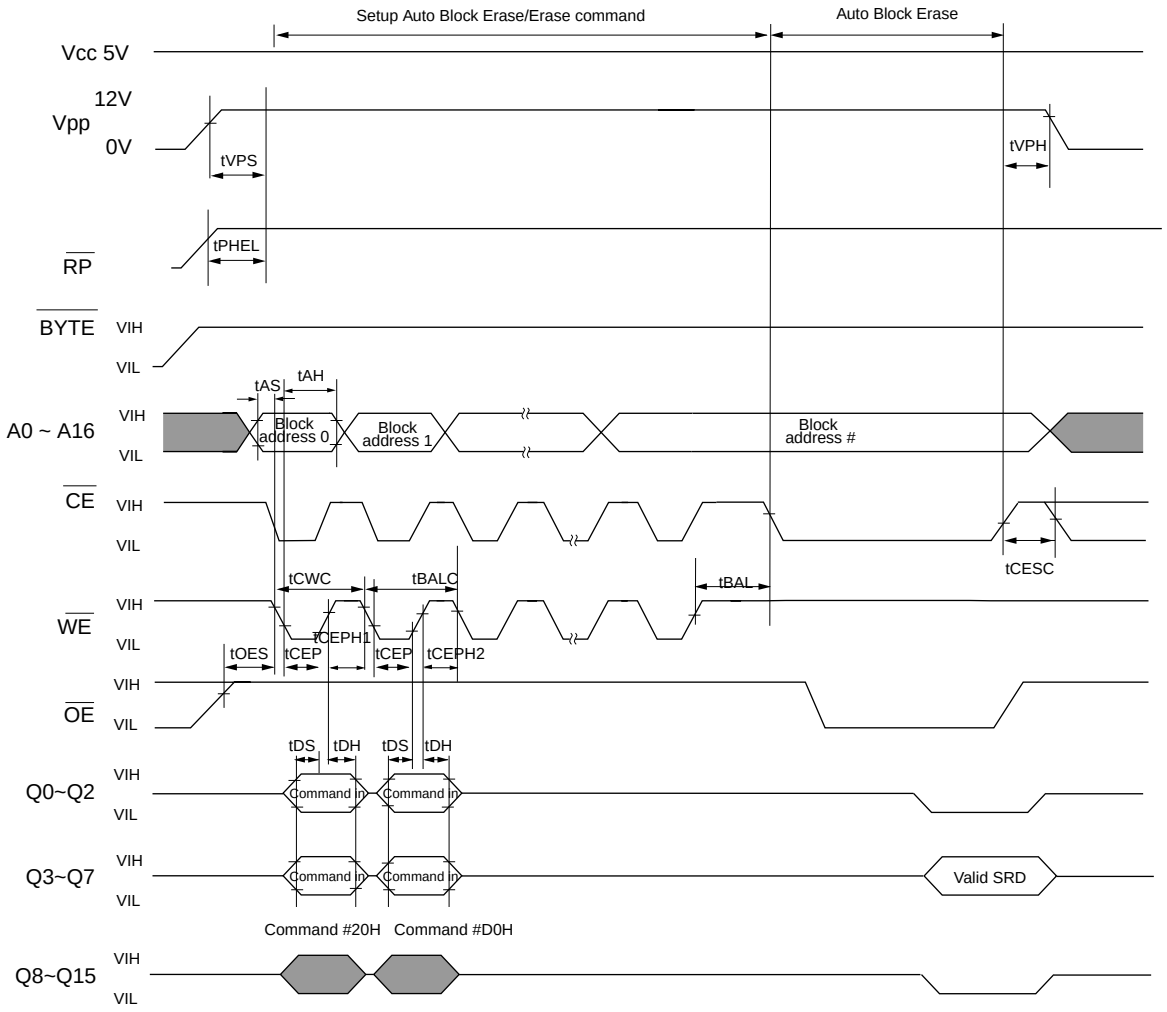
AUTOMATIC BLOCK ERASE TIMING WAVEFORM

Block data (refer to page 1 for block structure) are erased. External erase verify is not required because data are erased automatically by internal control circuit. Erasure completion can be verified by status register contents after automatic erase starts.

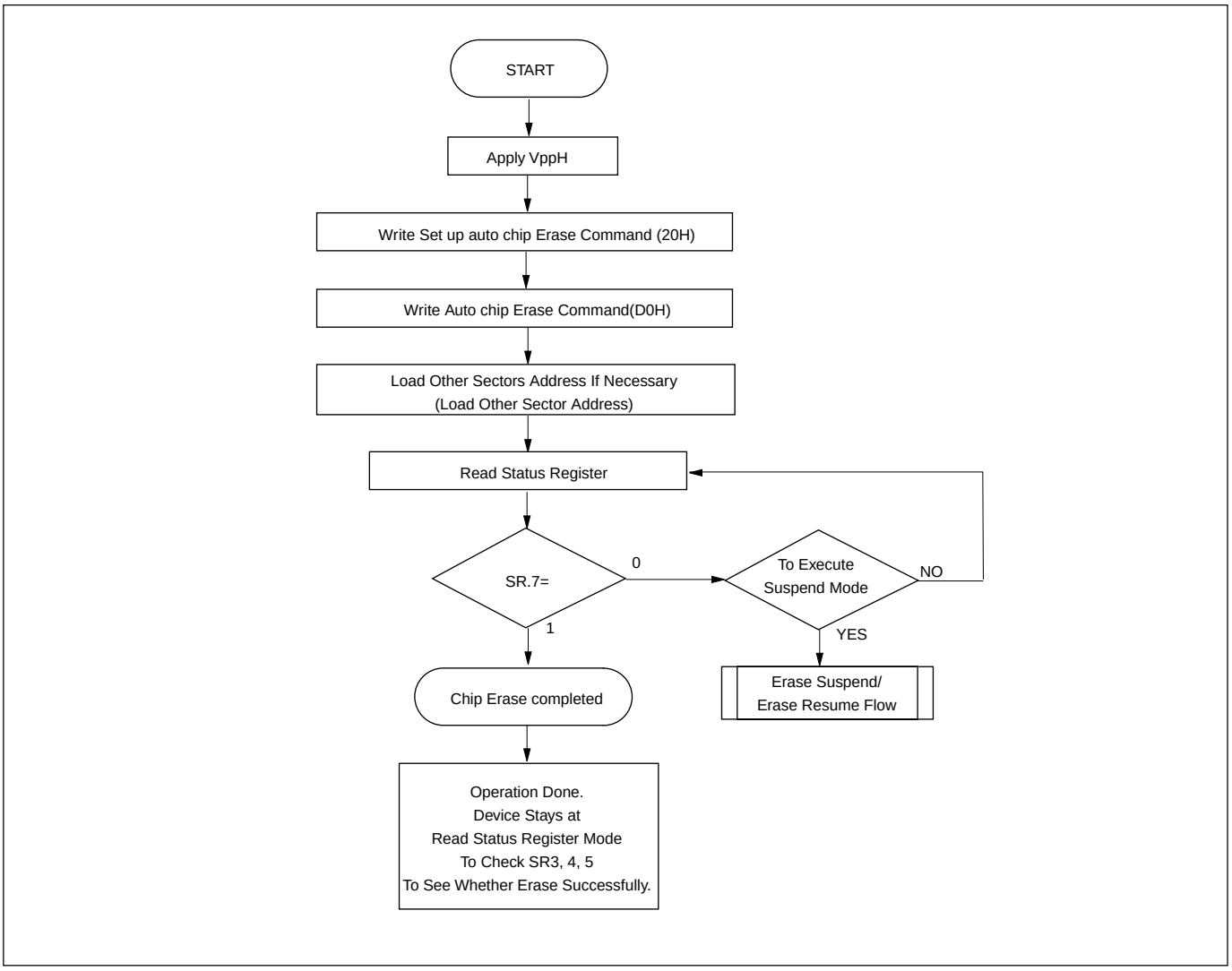
AUTOMATIC BLOCK ERASE TIMING WAVEFORM-BYTE MODE



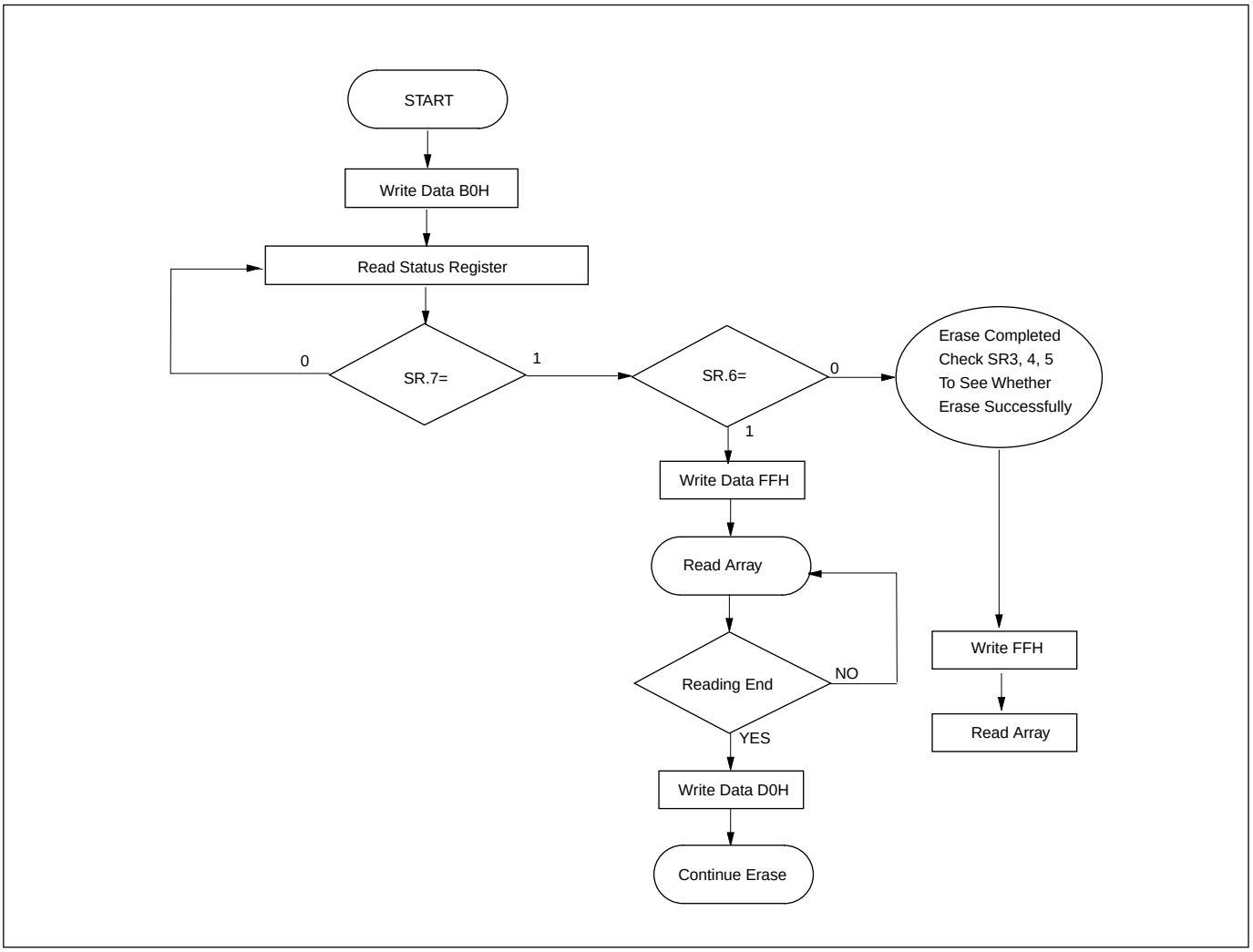
AUTOMATIC BLOCK ERASE TIMING WAVEFORM-WORD MODE



AUTOMATIC BLOCK ERASE ALGORITHM FLOWCHART



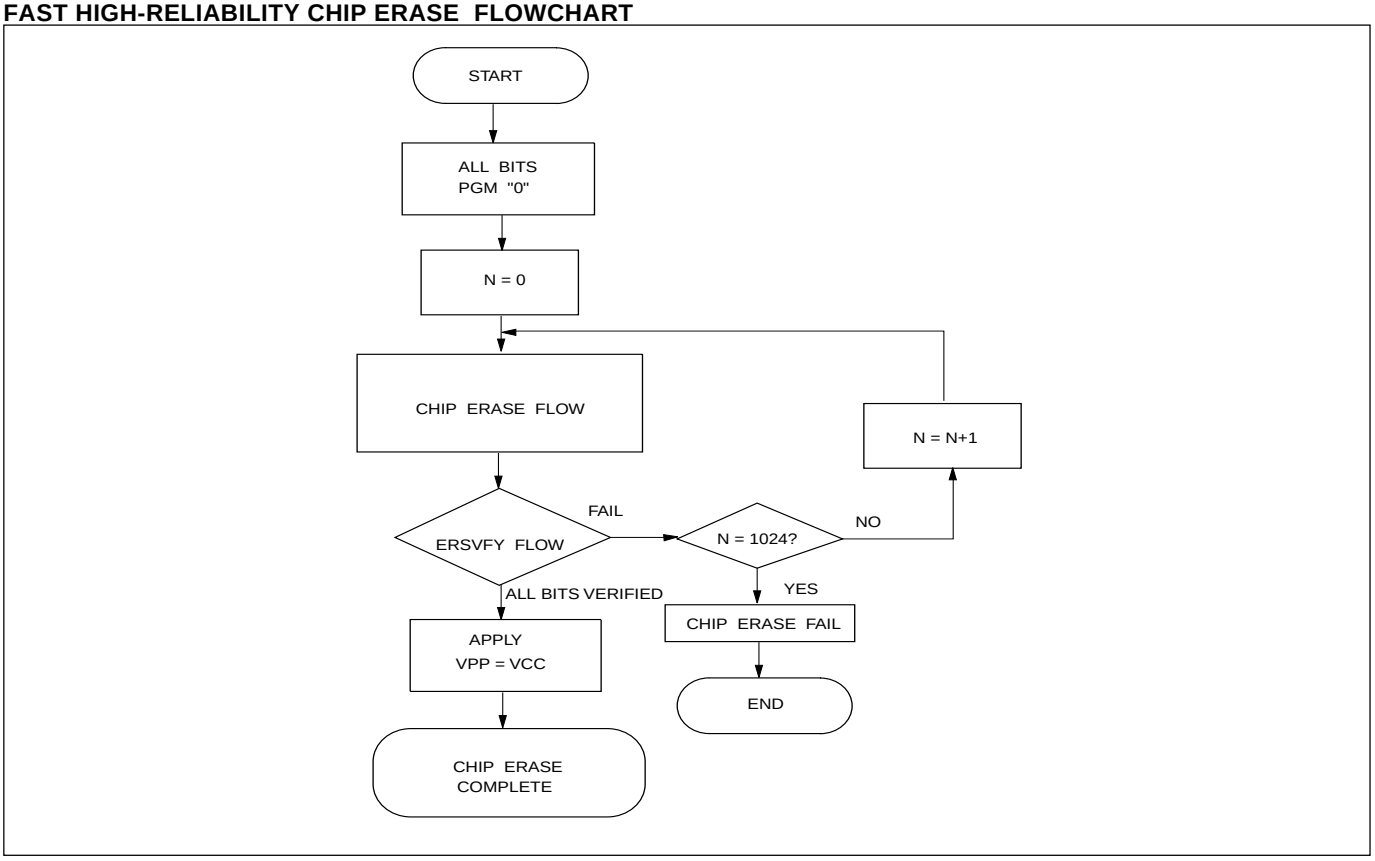
ERASE SUSPEND/ERASE RESUME FLOWCHART



FAST HIGH-RELIABILITY CHIP ERASE

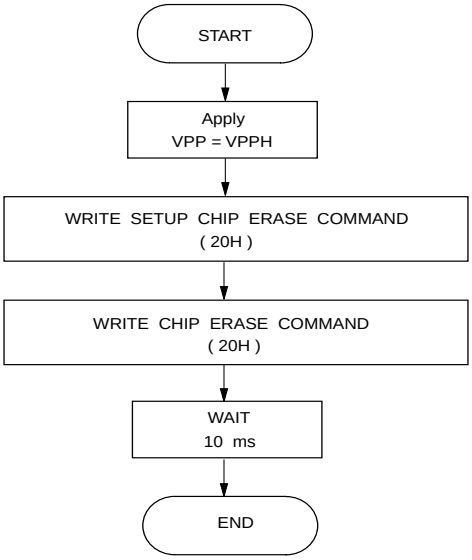
This device can be applied the Fast High-Reliability Chip erase algorithm shown in the following flowchart.

FAST HIGH-RELIABILITY CHIP ERASE FLOWCHART

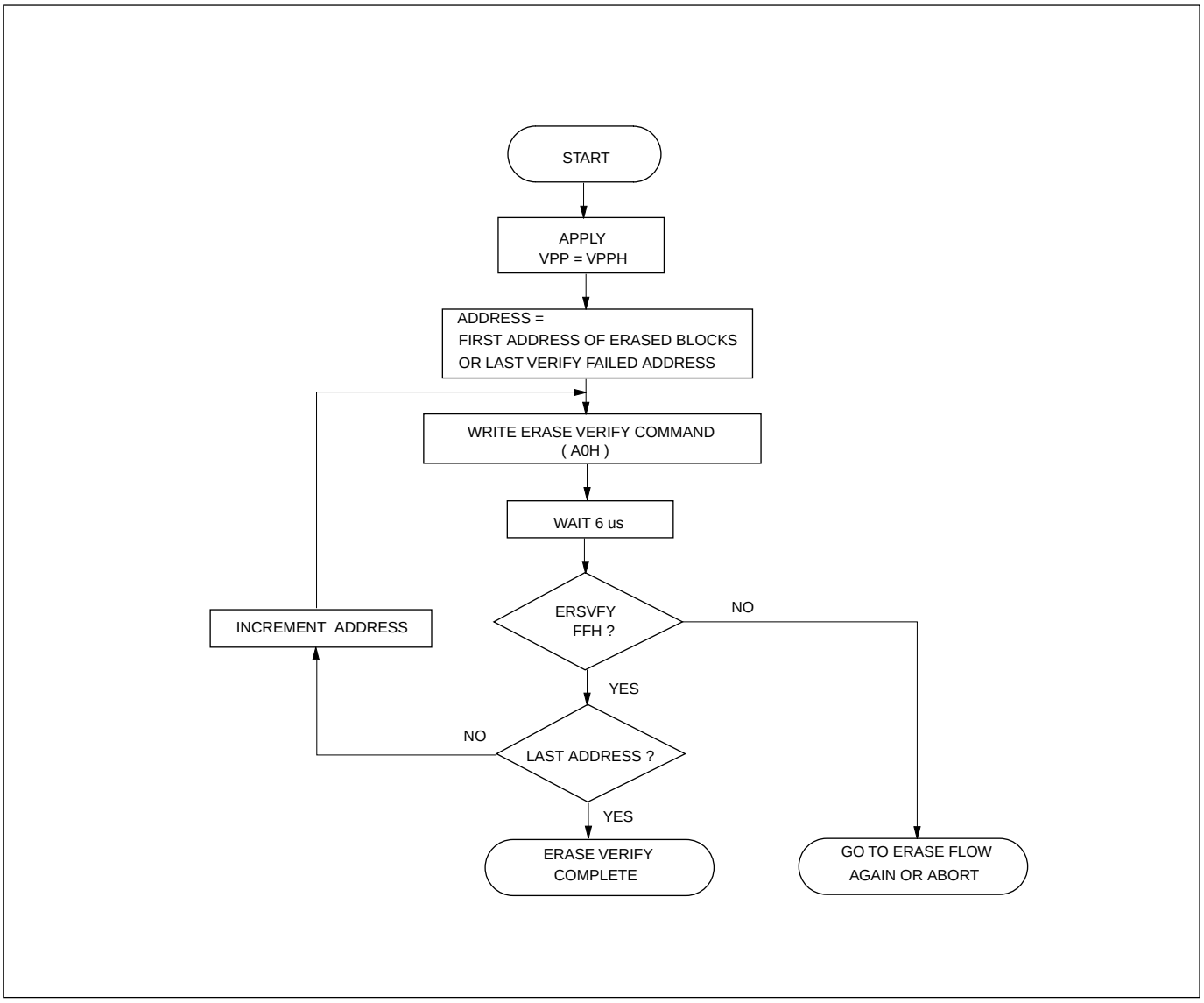


CHIP ERASE FLOW

Command Sequence



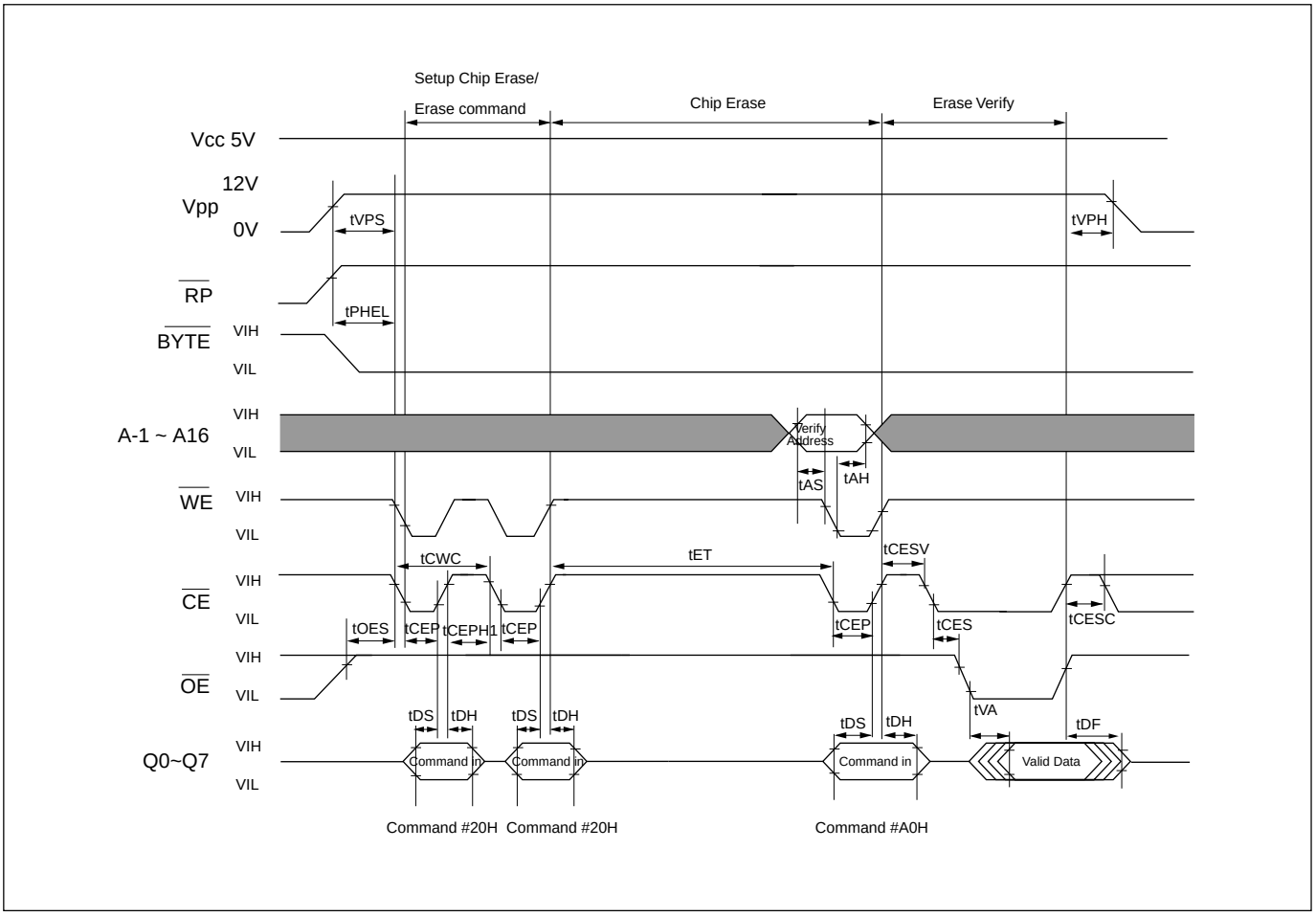
ERASE VERIFY FLOW



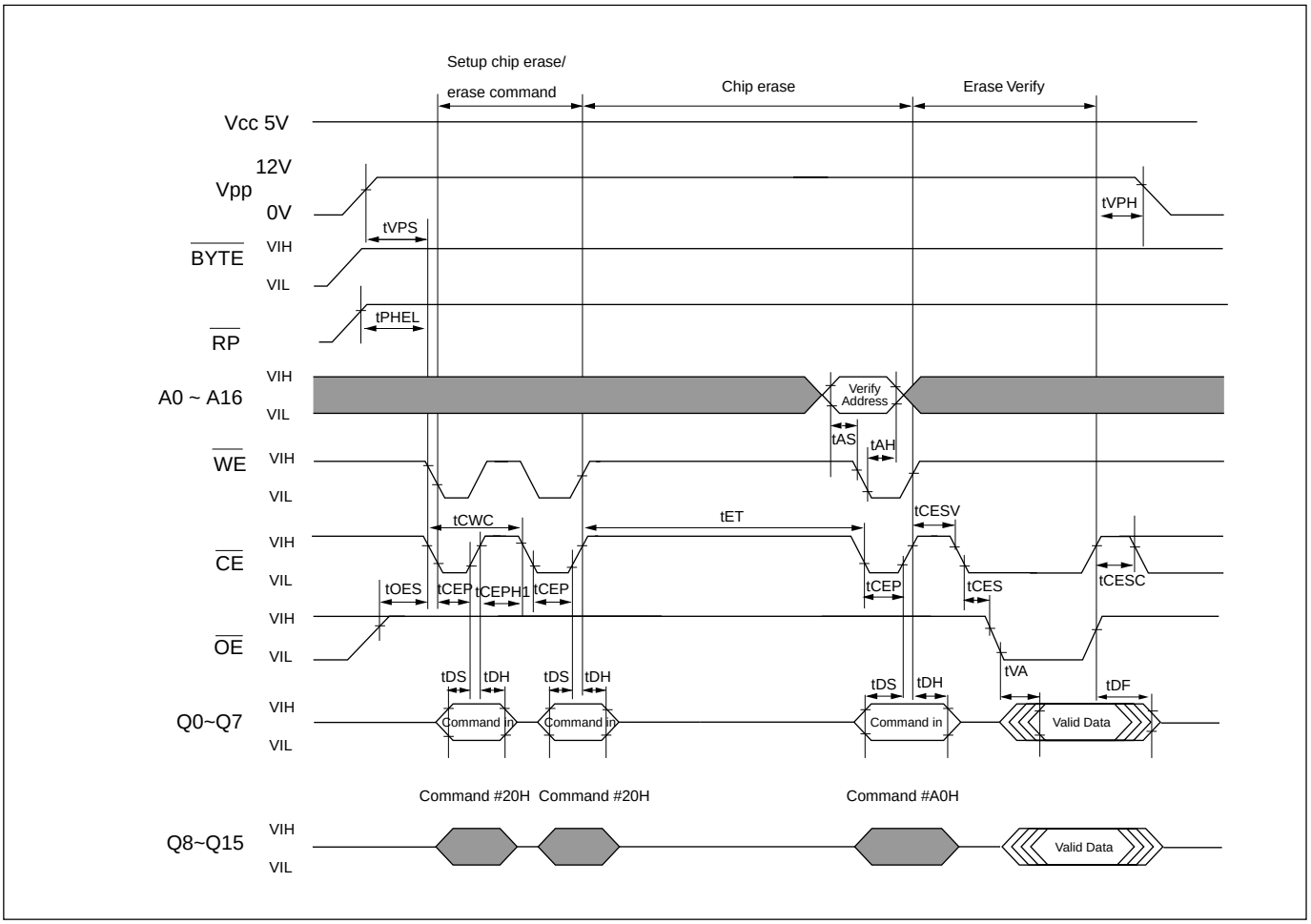
FAST HIGH-RELIABILITY CHIP ERASE TIMING WAVEFORM

All data in chip are erased. Control verification and additional erasure externally according to fast high-reliability chip erase flowchart. Successful erasure completion can be verified by status registers.

FAST HIGH-RELIABILITY CHIP ERASE TIMING WAVEFORM-BYTE MODE



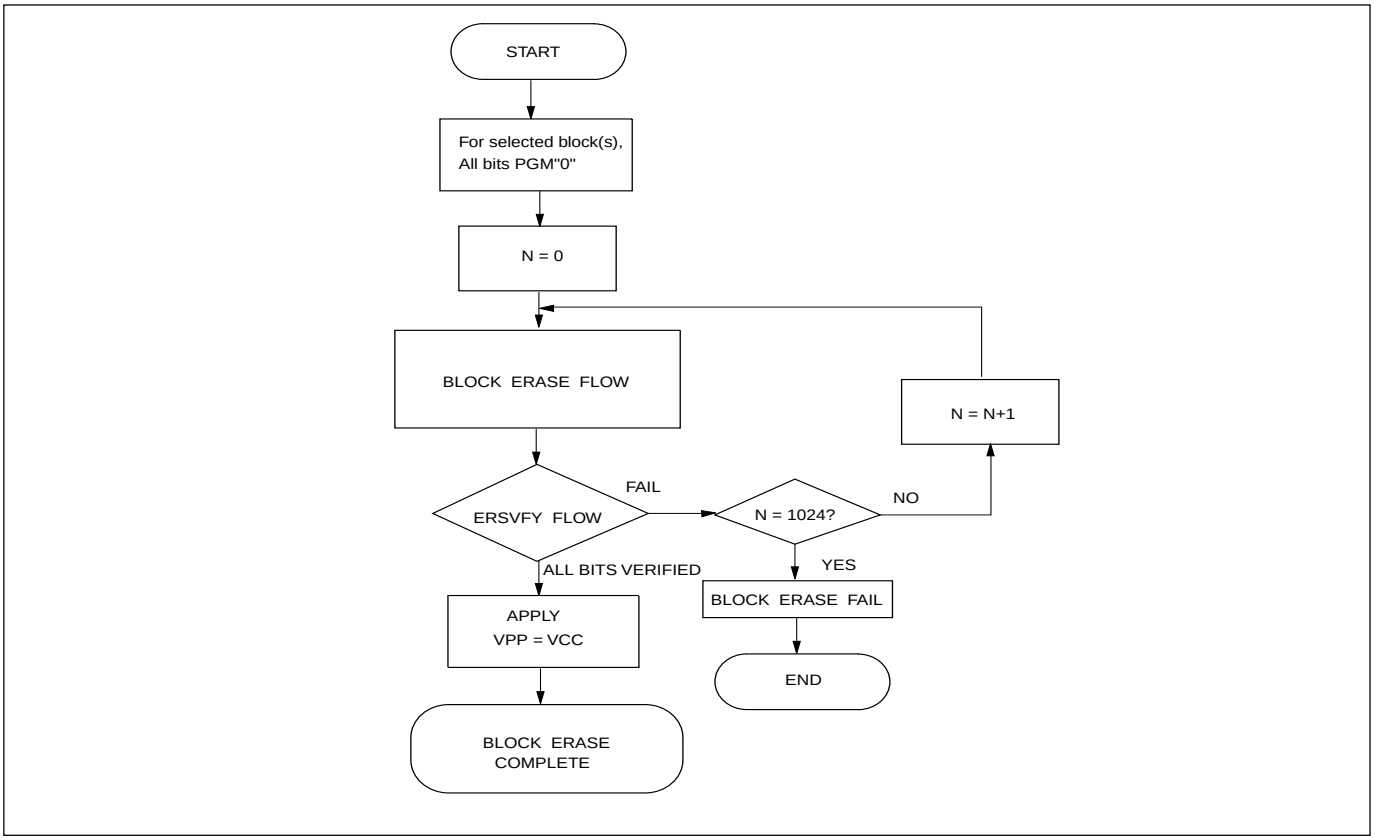
FAST HIGH-RELIABILITY CHIP ERASE TIMING WAVEFORM-WORD MODE



FAST HIGH-RELIABILITY BLOCK ERASE

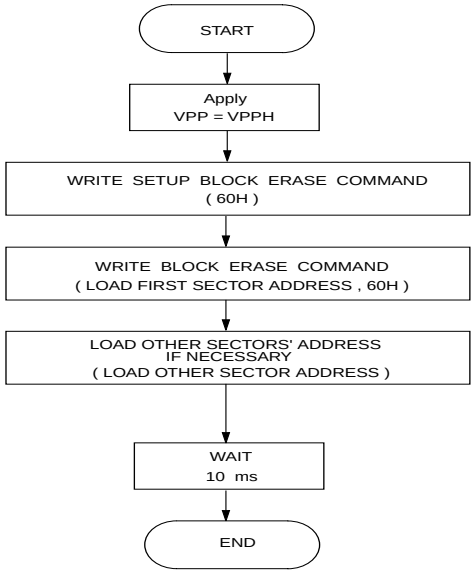
This device can be applied to the fast high-reliability block erase algorithm shown in the following flowchart.

FAST HIGH-RELIABILITY BLOCK ERASE FLOWCHART

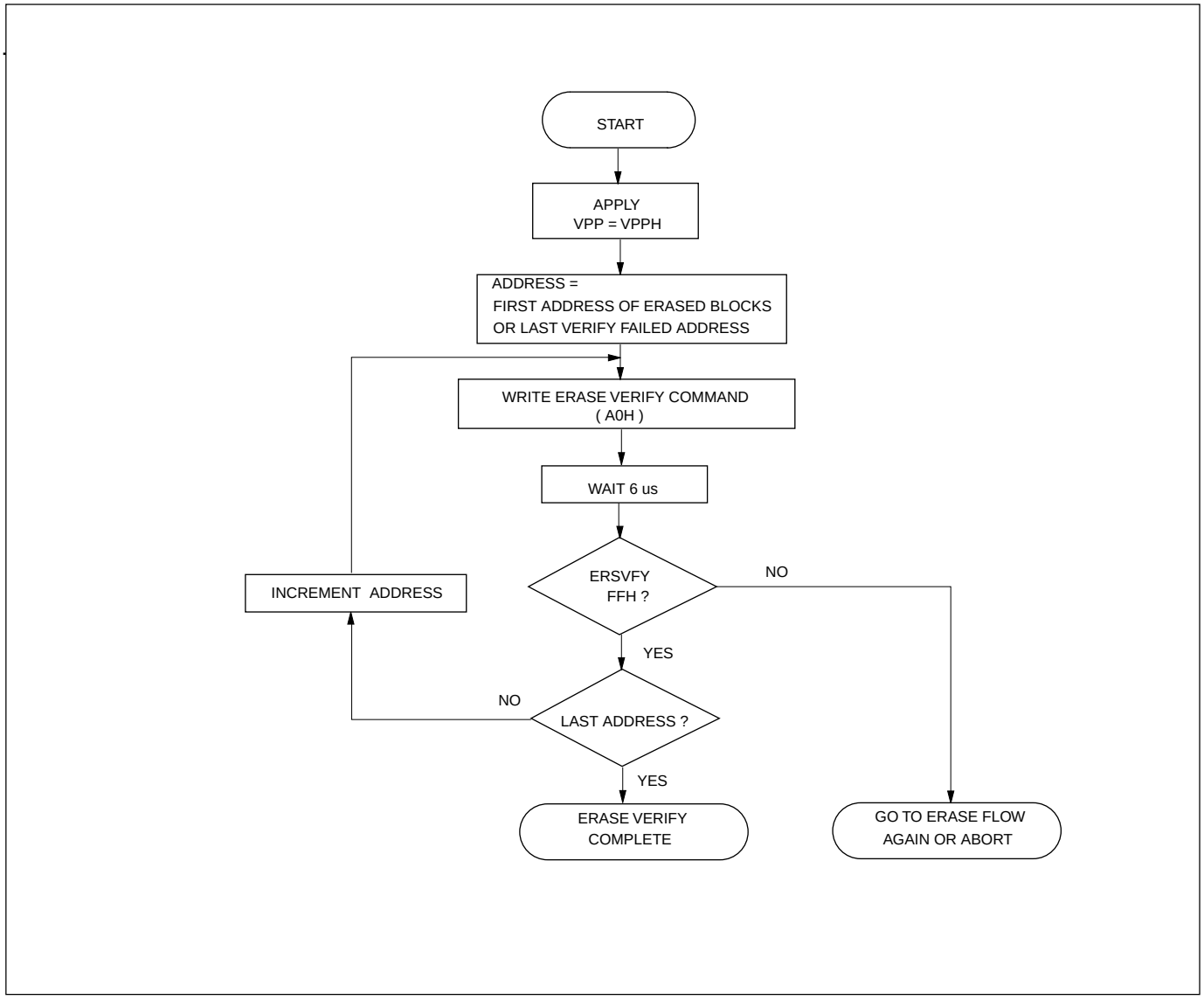


BLOCK ERASE FLOW

Command Sequence



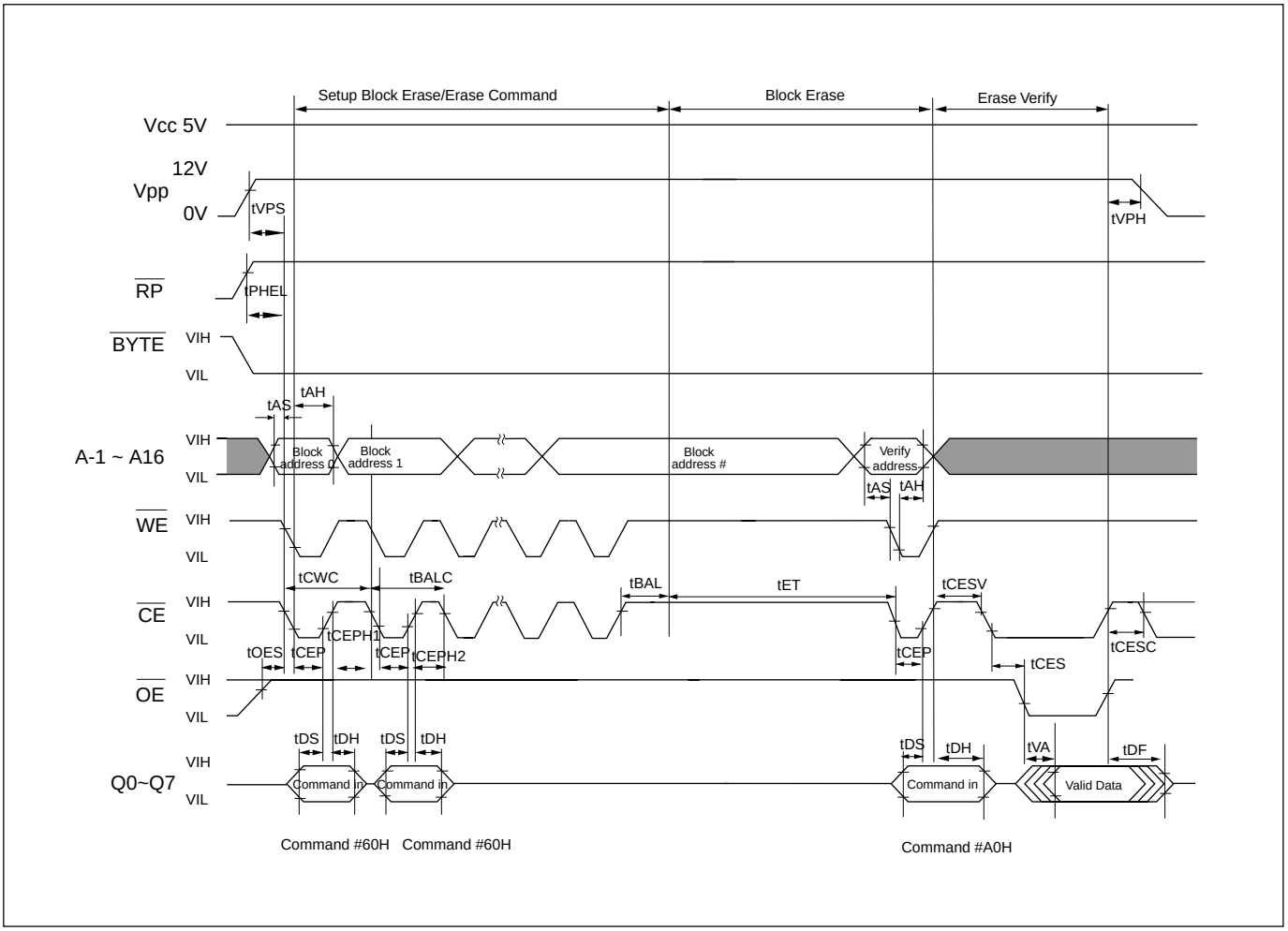
ERASE VERIFY FLOW



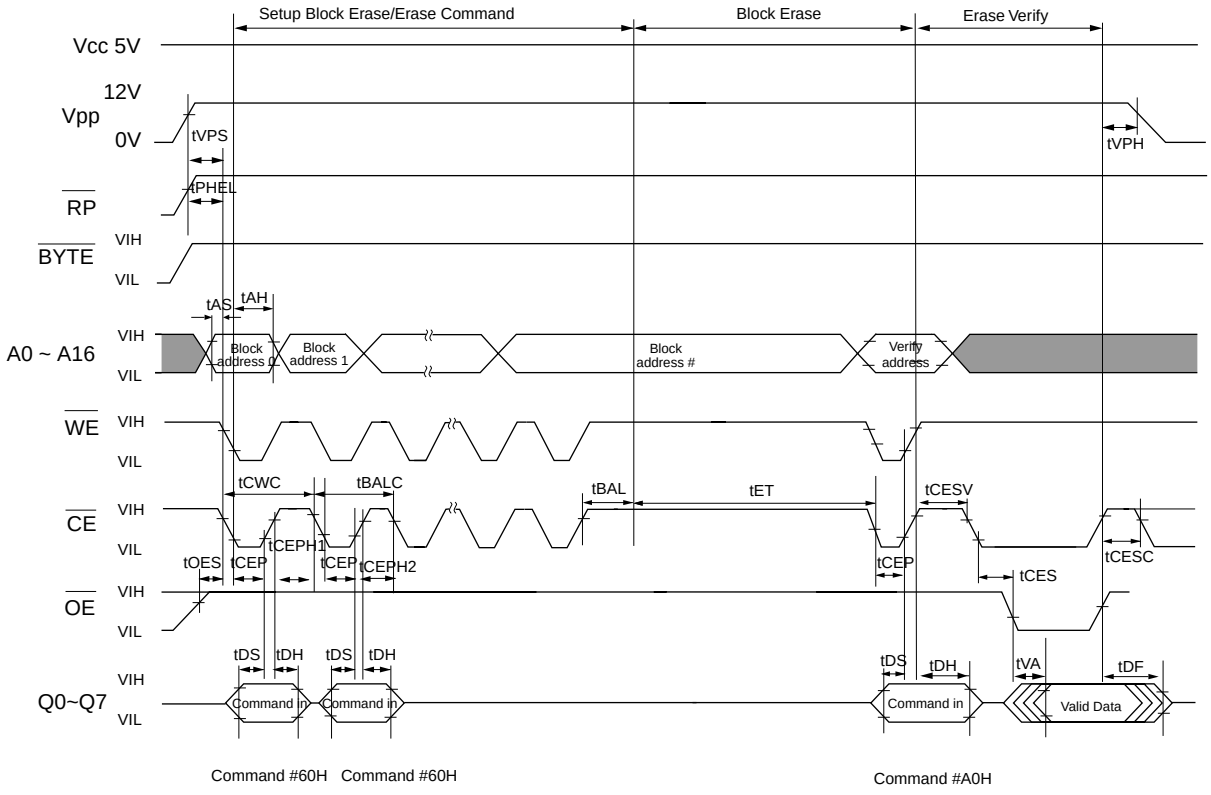
FAST HIGH-RELIABILITY BLOCK ERASE TIMING WAVEFORM

Indicated block data are erased. Control verification and additional erasure externally according to fast high-reliability block erase flowchart.

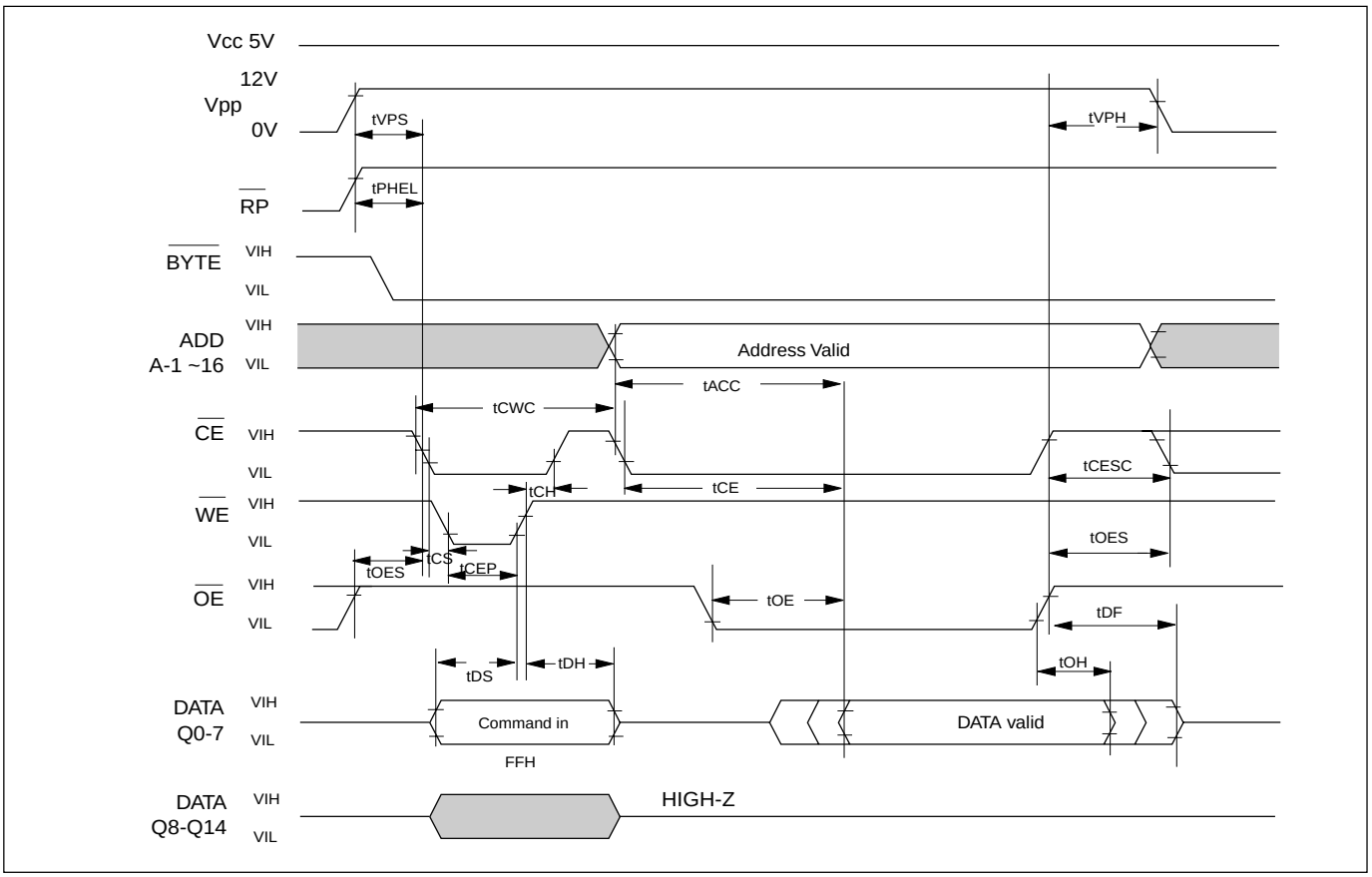
FAST HIGH-RELIABILITY BLOCK ERASE TIMING WAVEFORM-BYTE MODE



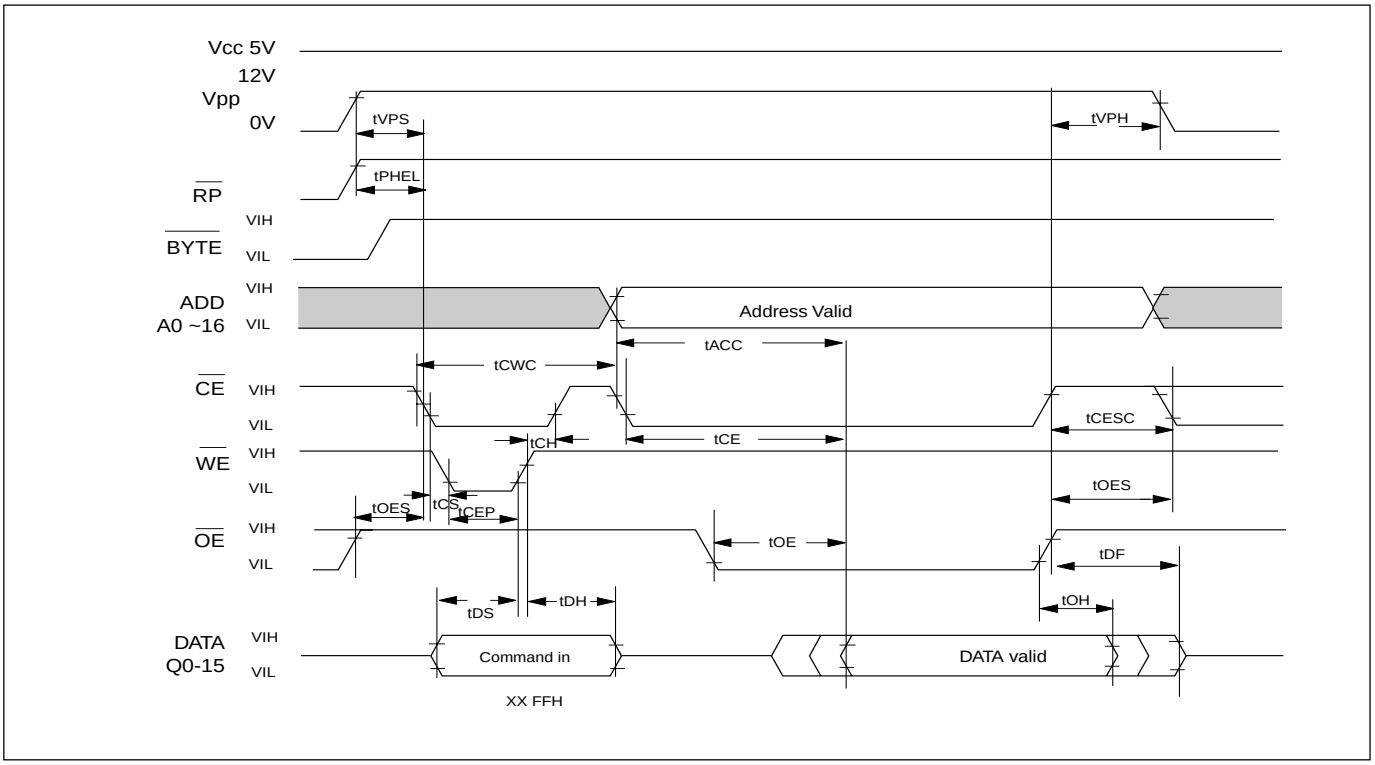
FAST HIGH-RELIABILITY BLOCK ERASE TIMING WAVEFORM-WORD MODE



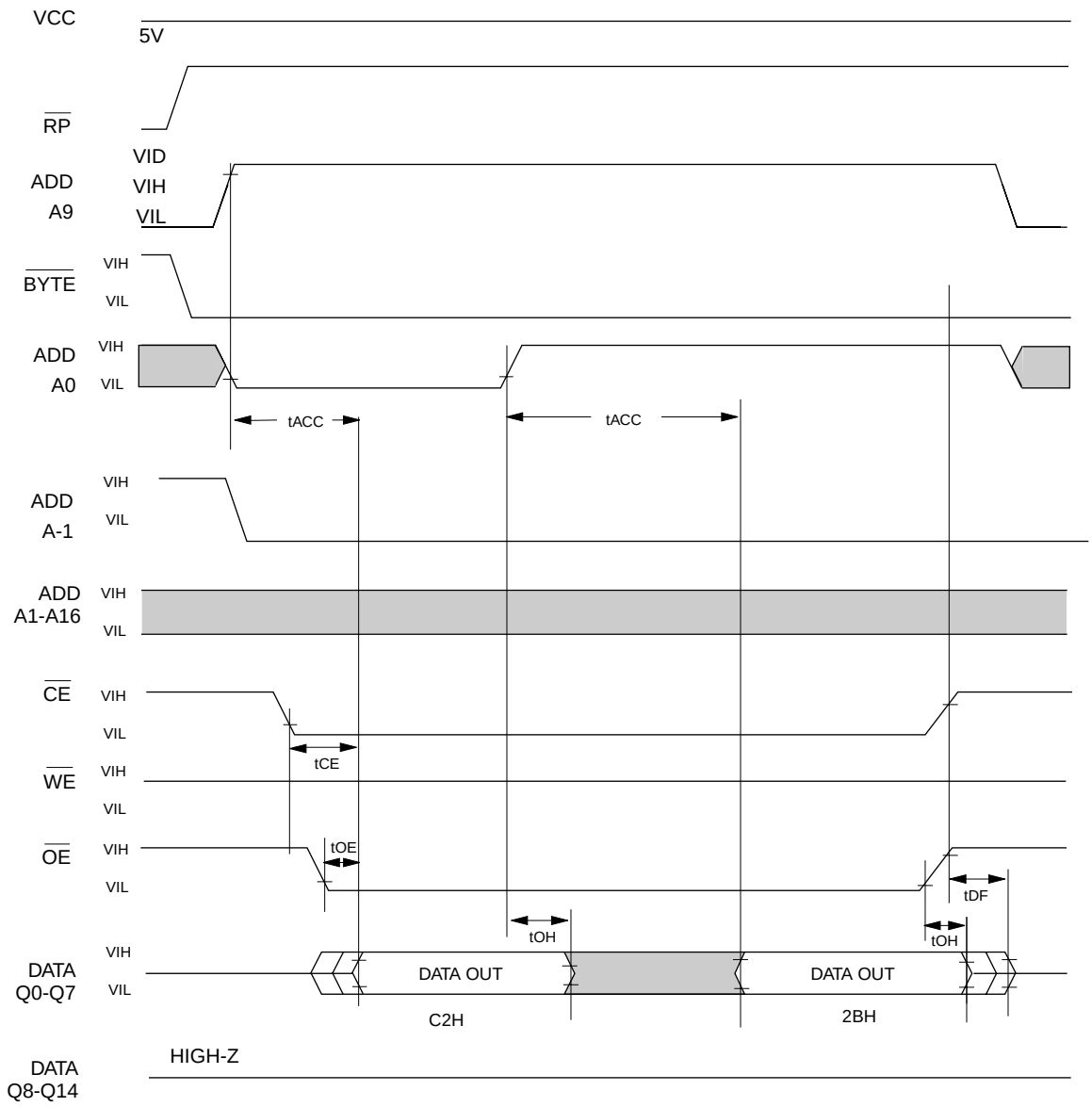
VPP HIGH READ TIMING WAVEFORM-BYTE MODE



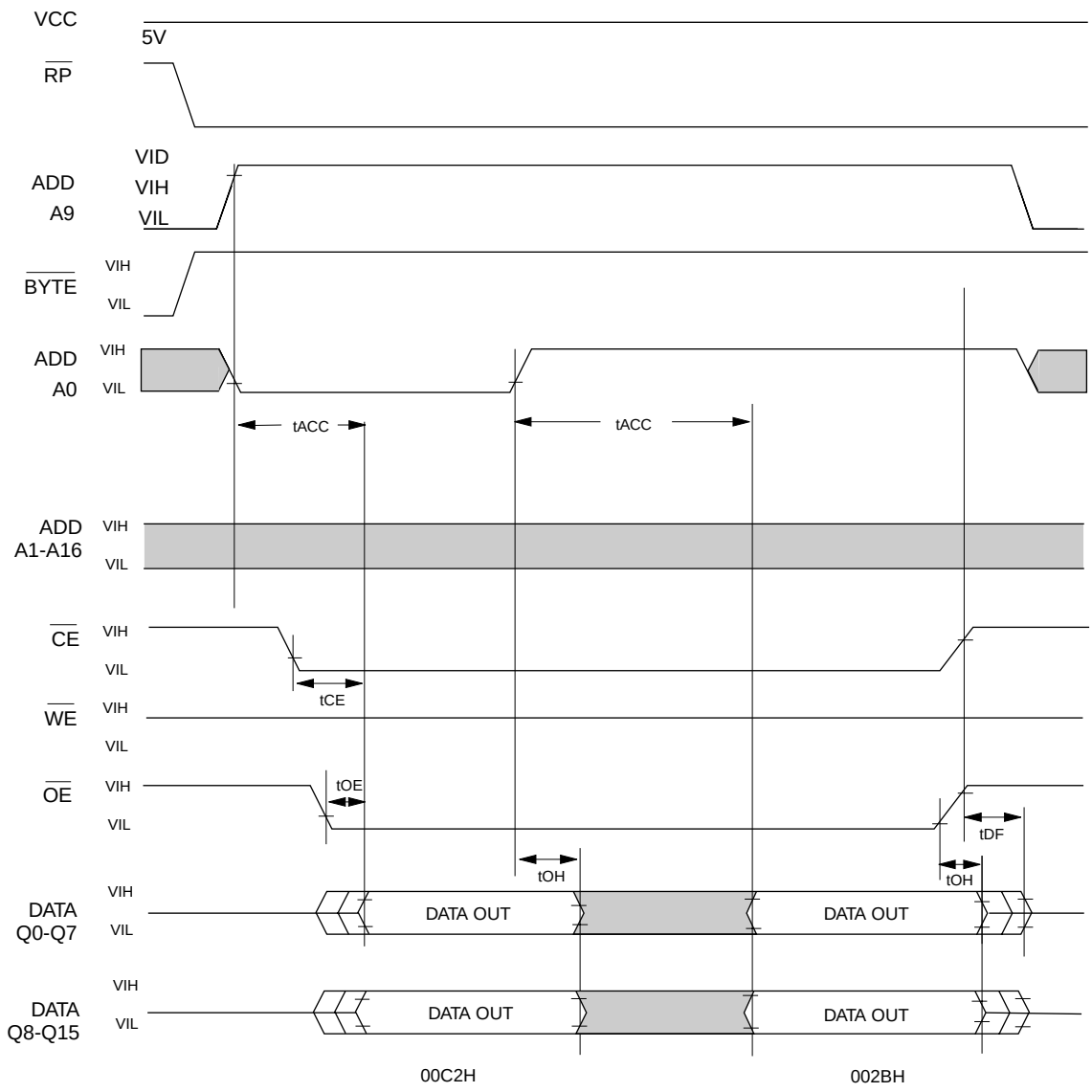
VPP HIGH READ TIMING WAVEFORM-WORD MODE



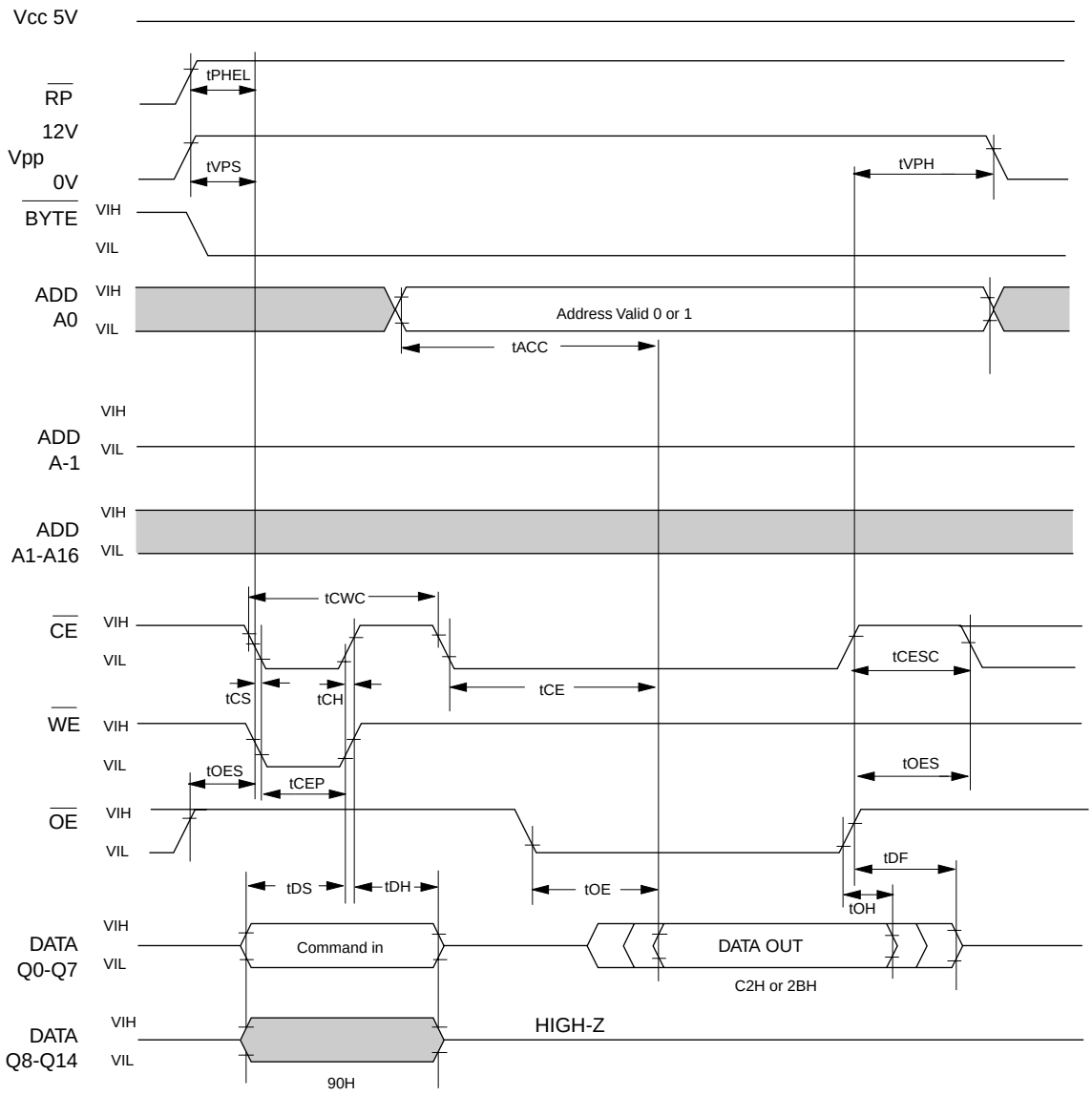
VPP LOW ID CODE READ TIMING WAVEFORM-BYTE MODE



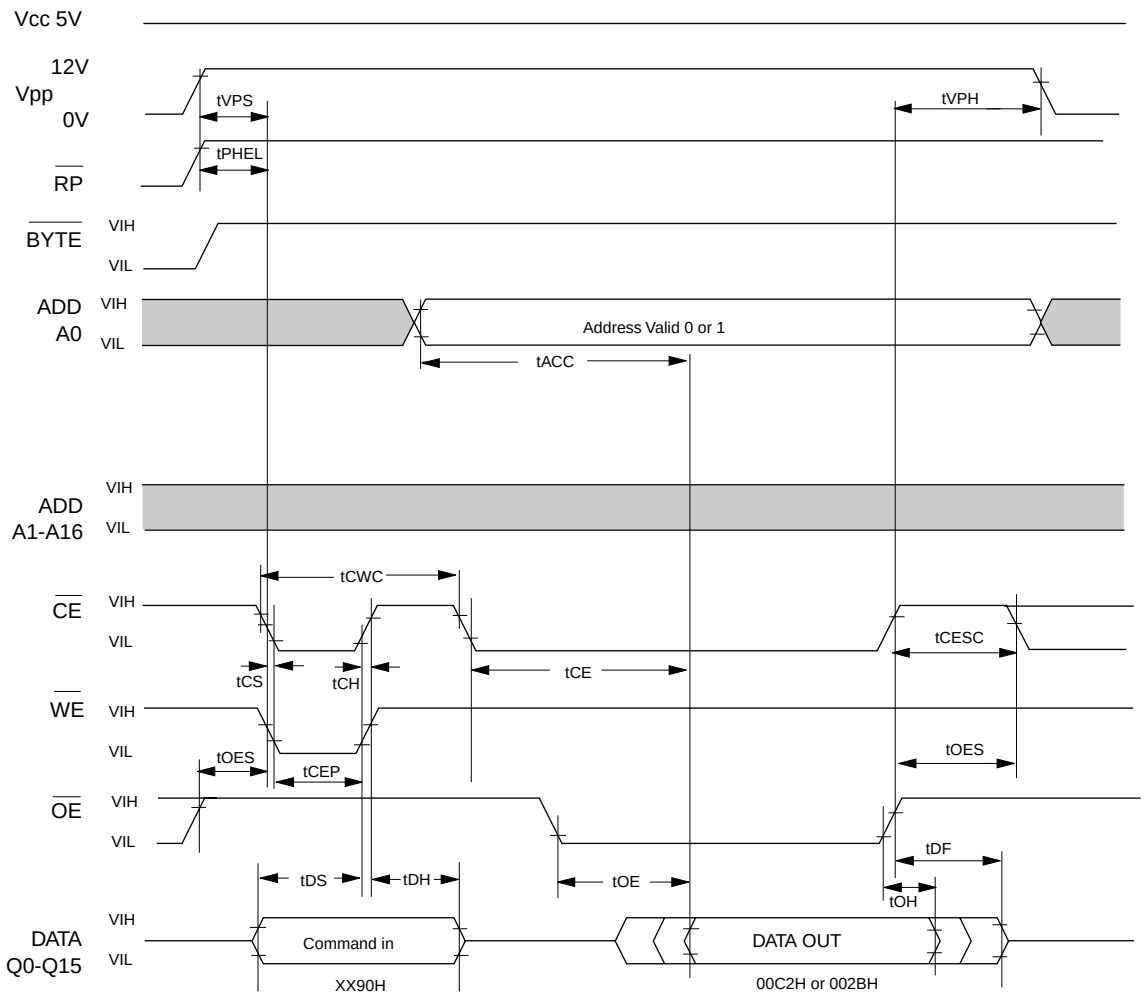
VPP LOW ID CODE READ TIMING WAVEFORM-WORD MODE



VPP HIGH ID CODE READ TIMING WAVEFORM-BYTE MODE



VPP HIGH ID CODE READ TIMING WAVEFORM-WORD MODE



NOTE:
BYTE pin is treated as Address pin All timing specifications for BYTE pin are the same as those for address pin.

ORDERING INFORMATION

PLASTIC PACKAGE

PART NO.	ACCESS TIME (ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(uA)	PACKAGE
MX28F2100BMC-70	70	50	100	44 Pin SOP
MX28F2100BMC-90	90	50	100	44 Pin SOP
MX28F2100BMC-12	120	50	100	44 Pin SOP
MX28F2100BTC-70	70	50	100	48 Pin TSOP (Normal Type)
MX28F2100BTC-90	90	50	100	48 Pin TSOP (Normal Type)
MX28F2100BTC-12	120	50	100	48 Pin TSOP (Normal Type)

Revision History

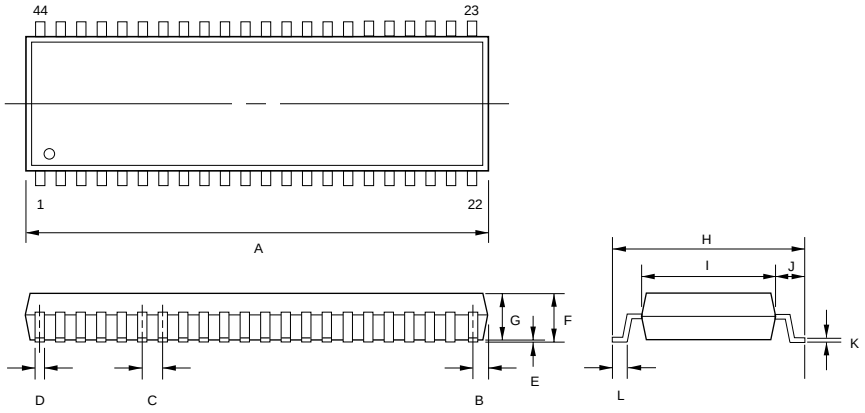
Rev. #	Description	Date
1.4	Statement cleared for customer's better understanding	10/22/1997

PACKAGE INFORMATION

44-PIN PLASTIC SOP(500 mil)

ITEM	MILLIMETERS	INCHES
A	28.70 max.	1.130max.
B	1.10 [REF]	.043 [REF]
C	1.27 [TP]	.050 [TP]
D	.40 ± .10[Typ.]	.016 ±.004[Typ.]
E	.010 min.	.004 min.
F	3.00 max.	.118 max.
G	2.80 ± .13	.110 ± .005
H	16.04 ± .30	.631 ± .012
I	12.60	.496
J	1.72	.068
K	.15 ± .10 [Typ.]	.006 ±.004[Typ.]
L	.80 ± .20	.031± .008

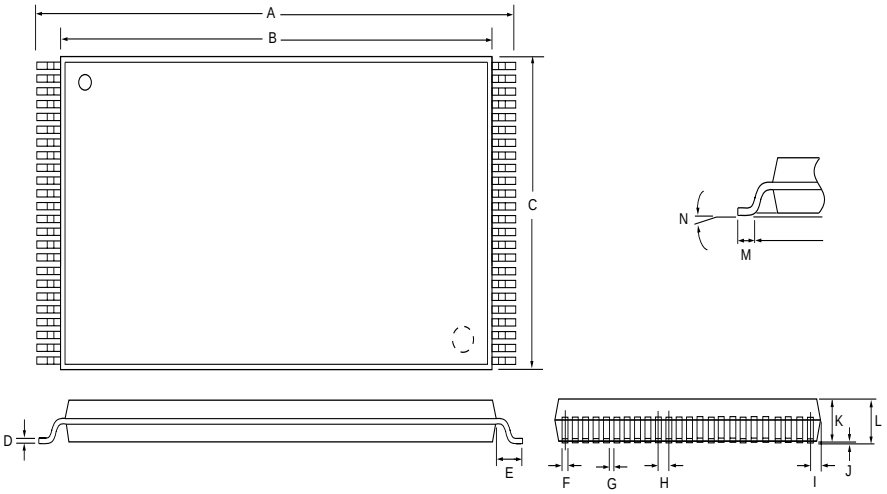
NOTE: Each lead certerline is located within .25mm[.01 inch] of its true position [TP] at a maximum at maximum material condition.



48-PIN PLASTIC TSOP

ITEM	MILLIMETERS	INCHES
A	20.0 ± .20	.787 ± .008
B	18.40 ± .10	.724 ± .004
C	12.20 max.	.480 max.
D	0.15 [Typ.]	.006 [Typ.]
E	.80 [Typ.]	.031 [Typ.]
F	.20 ± .10	.008 ± .004
G	.30 ± .10	.012 ± .004
H	.50 [Typ.]	.020 [Typ.]
I	.45 max.	.018 max.
J	0 ~ .20	0 ~ .008
K	1.00 ± .10	.039 ± .004
L	1.27 max.	.050 max.
M	.50	.020
N	0 ~5°	.500

NOTE: Each lead certerline is located within .25mm[.01 inch] of its true position [TP] at a maximum at maximum material condition.



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