



3.3V CMOS 20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O AND BUS-HOLD

IDT74LVCH162721A

FEATURES:

- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{cc} = 3.3V \pm 0.3V$, Normal Range
- $V_{cc} = 2.7V$ to $3.6V$, Extended Range
- CMOS power levels (0.4 μ W typ. static)
- All inputs, outputs, and I/O are 5V tolerant
- Supports hot insertion
- Available in SSOP, TSSOP, and TVSOP packages

DRIVE FEATURES:

- Balanced Output Drivers: $\pm 12mA$
- Low switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

DESCRIPTION:

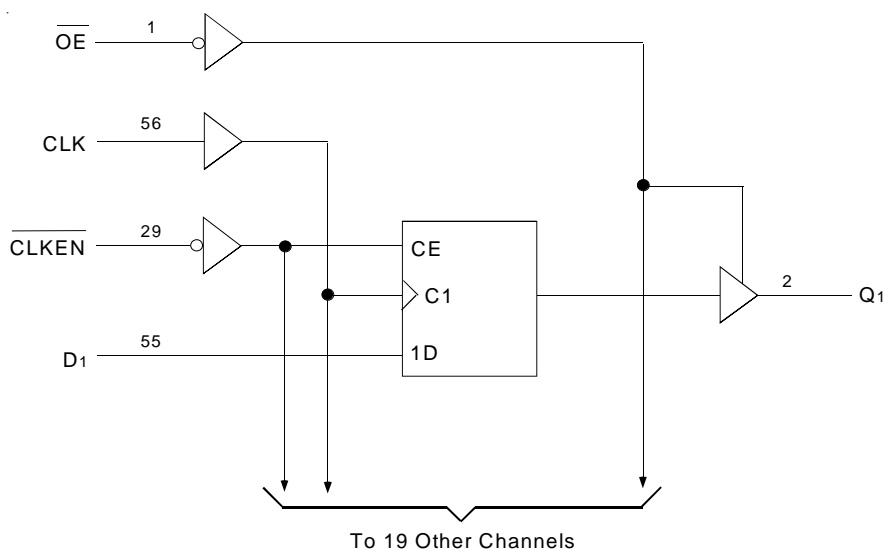
This 20-bit flip-flop is built using advanced dual metal CMOS technology. The 20 flip-flops of the LVCH162721A are edge-triggered D-type flip-flops with qualified clock storage. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs if the clock-enable (\overline{CLKEN}) input is low. If \overline{CLKEN} is high, no data is stored.

A buffered output-enable (\overline{OE}) input places the 20 outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without the need for interface or pullup components. \overline{OE} does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

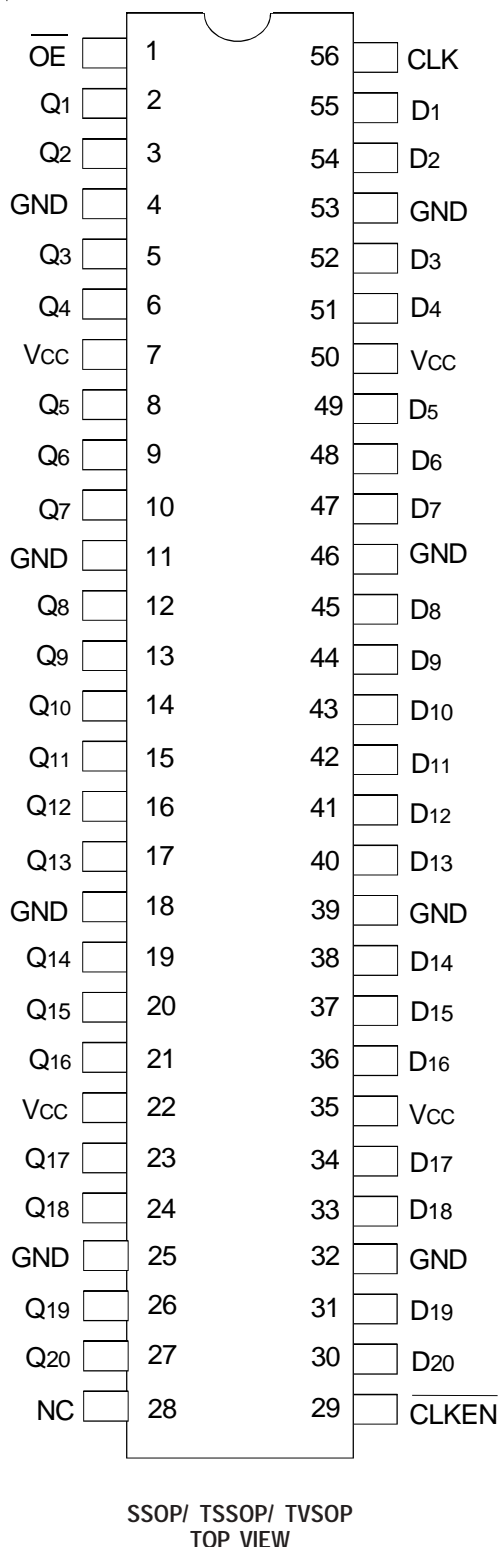
The LVCH162721A has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been designed to drive $\pm 12mA$ at the designated threshold levels.

The LVCH162721A has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +6.5	V
TSTG	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-50 to +50	mA
I _{IK} I _{OK}	Continuous Clamp Current, V _I < 0 or V _O < 0	-50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	6.5	8	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	6.5	8	pF

NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
\overline{OE}	3-State Output Enable Input (Active LOW)
D _x	Data Inputs ⁽¹⁾
Q _x	3-State Outputs
CLK	Clock Input
\overline{CLKEN}	Clock Enable Input (Active LOW)
NC	No Internal Connection

NOTE:

- These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE (EACH FLIP-FLOP)⁽¹⁾

Inputs				Outputs
\overline{OE}	\overline{CLKEN}	CLK	D _x	Q _x
L	H	X	X	Q ⁽²⁾
L	L	↑	H	H
L	L	↑	L	L
L	L	L or H	X	Q ⁽²⁾
H	X	X	X	Z

NOTES:

- H = HIGH Voltage Level
X = Don't Care
L = LOW Voltage Level
Z = High-Impedance
↑ = LOW-to-HIGH transition
- Output level before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	
V _{IL}	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH} I _{IL}	Input Leakage Current	V _{CC} = 3.6V	V _I = 0 to 5.5V	—	—	±5	μA
I _{OZH} I _{OZL}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = 0 to 5.5V	—	—	±10	μA
I _{OFF}	Input/Output Power Off Leakage	V _{CC} = 0V, V _{IN} or V _O ≤ 5.5V		—	—	±50	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = -18mA		—	-0.7	-1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CC1} I _{CC2} I _{CC3}	Quiescent Power Supply Current	V _{CC} = 3.6V	V _{IN} = GND or V _{CC}	—	—	10	μA
			3.6 ≤ V _{IN} ≤ 5.5V ⁽²⁾	—	—	10	
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND		—	—	500	μA

NOTES:

- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- This applies in the disabled state only.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
I _{BH1} I _{BH2}	Bus-Hold Input Sustain Current	V _{CC} = 3V	V _I = 2V	-75	—	—	μA
			V _I = 0.8V	75	—	—	
I _{BH3} I _{BH4}	Bus-Hold Input Sustain Current	V _{CC} = 2.3V	V _I = 1.7V	—	—	—	μA
			V _I = 0.7V	—	—	—	
I _{BHO1} I _{BHO2}	Bus-Hold Input Overdrive Current	V _{CC} = 3.6V	V _I = 0 to 3.6V	—	—	±500	μA

NOTES:

- Pins with Bus-Hold are identified in the pin description.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = - 0.1mA	V _{CC} - 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = - 4mA	1.9	—	
			I _{OH} = - 6mA	1.7	—	
		V _{CC} = 2.7V	I _{OH} = - 4mA	2.2	—	
			I _{OH} = - 8mA	2	—	
		V _{CC} = 3V	I _{OH} = - 6mA	2.4	—	
I _{OH} = - 12mA	2		—			
V _{OL}	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 4mA	—	0.4	
			I _{OL} = 6mA	—	0.55	
		V _{CC} = 2.7V	I _{OL} = 4mA	—	0.4	
			I _{OL} = 8mA	—	0.6	
		V _{CC} = 3V	I _{OL} = 6mA	—	0.55	
I _{OL} = 12mA	—		0.8			

NOTE:
1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range.
T_A = - 40°C to + 85°C.

OPERATING CHARACTERISTICS, V_{CC} = 3.3V ± 0.3V, T_A = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance Outputs enabled	C _L = 0pF, f = 10Mhz		pF
CPD	Power Dissipation Capacitance Outputs disabled			

SWITCHING CHARACTERISTICS⁽¹⁾

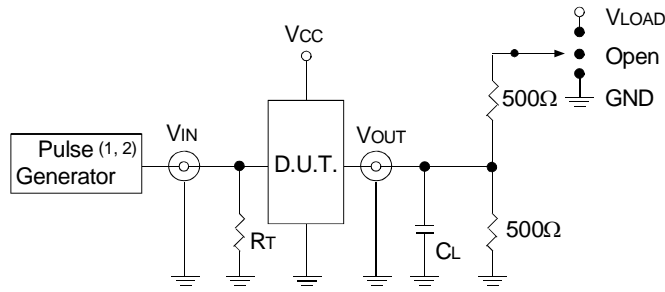
Symbol	Parameter	V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	
t _{PLH}	Propagation Delay	2	6.6	2	5.8	ns
t _{PHL}	CLK to Qx					
t _{PZH}	Output Enable Time	1.5	7.6	1.5	6.6	ns
t _{PZL}	\overline{OE} to Qx					
t _{PHZ}	Output Disable Time	1.5	5.9	1.5	5.6	ns
t _{PLZ}	\overline{OE} to Qx					
t _{SU}	Set-up Time, data before CLK↑	3.6	—	3.1	—	ns
t _{SU}	Set-up Time, \overline{CLKEN} before CLK↑	3.1	—	2.7	—	ns
t _H	Hold Time, data after CLK	0	—	0	—	ns
t _H	Hold Time, \overline{CLKEN} after CLK	0	—	0	—	ns
t _w	Pulse Duration, CLK HIGH or LOW	3.3	—	3.3	—	ns
t _{sk(0)}	Output Skew ⁽²⁾	—	—	—	500	ps

NOTES:
1. See TEST CIRCUITS AND WAVEFORMS. T_A = - 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} ⁽¹⁾ = 3.3V ± 0.3V	V _{CC} ⁽¹⁾ = 2.7V	V _{CC} ⁽²⁾ = 2.5V ± 0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF



LVC Link

Test Circuit for All Outputs

DEFINITIONS:

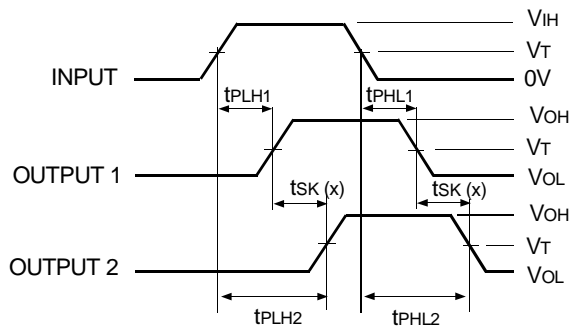
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other Tests	Open



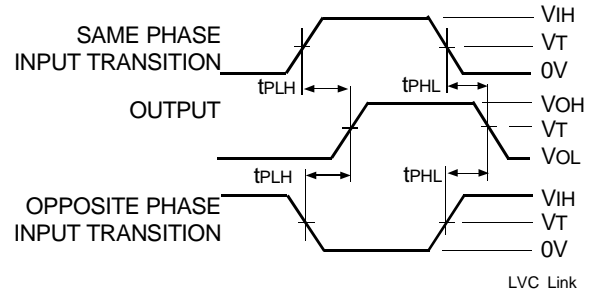
$$tsk(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

LVC Link

Output Skew - tsk(x)

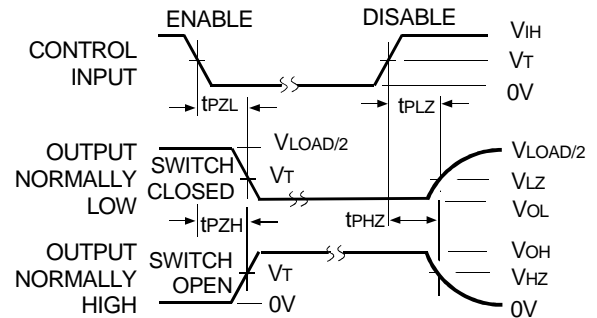
NOTES:

1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.



LVC Link

Propagation Delay

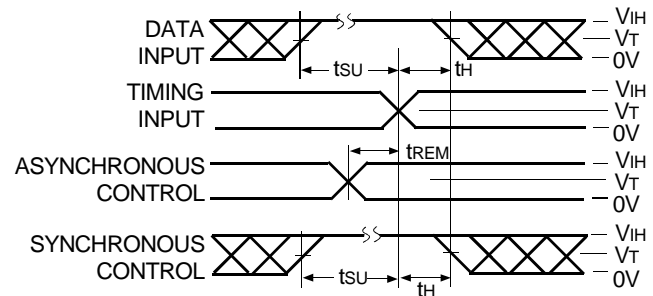


LVC Link

Enable and Disable Times

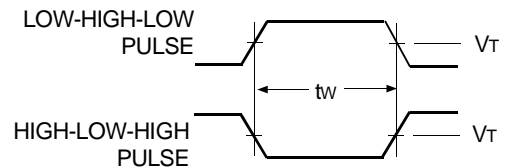
NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



LVC Link

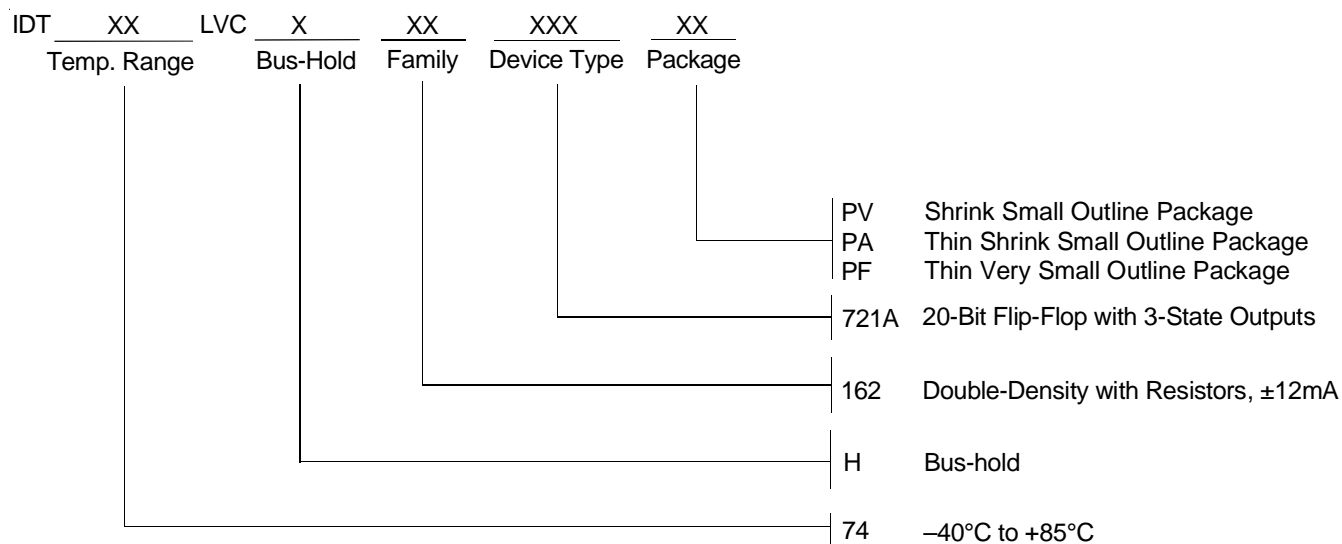
Set-up, Hold, and Release Times



LVC Link

Pulse Width

ORDERING INFORMATION



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