Integrated Circuit Systems, Inc.

ICS85401
2:1
DIFFERENTIAL-TO-LVDS MULTIPLEXER

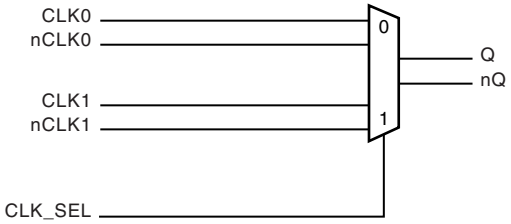
GENERAL DESCRIPTION

The ICS85401 is a high performance 2:1 Differential-to-LVDS Multiplexer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS85401 can also perform differential translation because the differential inputs accept LVPECL, CML as well as LVDS levels. The ICS85401 is packaged in a small 3mm x 3mm 16 VFQFN package, making it ideal for use on space constrained boards.

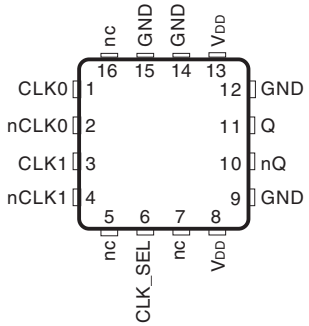
FEATURES

- 2:1 LVDS MUX
- 1 LVDS output
- 2 differential clock inputs can accept: LVPECL, LVDS, CML
- Maximum input/output frequency: >2.5GHz
- Translates LVCMOS/LVTTL input signals to LVDS levels by using a resistor bias network on nCLK0, nCLK1
- Propagation delay: 460ps (maximum)
- Part-to-part skew: 100ps (maximum)
- 3.3V operating supply
- -40°C to 85°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS85401
16-Lead VFQFN
3mm x 3mm x 0.95 package body
K Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	CLK0	Input	Pulldown	Non-inverting differential clock input.
2	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{DD}/2$ default when left floating.
3	CLK1	Input	Pulldown	Non-inverting differential clock input.
4	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{DD}/2$ default when left floating.
5, 7, 16	nc	Unused		Unused pins.
6	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1, nCLK1 inputs. When LOW, selects CLK0, nCLK0 inputs. LVCMOS / LVTTL interface levels.
8, 13	V_{DD}	Power		Positive supply pins.
9, 12, 14, 15	GND	Power		Power supply ground.
10, 11	nQ, Q	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			1		pF
R_{PULLUP}	Input Pullup Resistor			37		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			37		kΩ

TABLE 3. CONTROL INPUT FUNCTION TABLE

Input	Clock Out
CLK_SEL	CLK
0	CLK0, nCLK0
1	CLK1, nCLK1

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	51.5°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				40	mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK_SEL		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	CLK_SEL		-0.3		0.8	V
I_{IH}	Input High Current	CLK_SEL	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	CLK_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

NOTE: Outputs terminated with 50Ω to V_{DD}/2. See Parameter Measurement Information, "Output Load Test Circuit".

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0, CLK1	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		nCLK0, nCLK1	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	CLK0, CLK1	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		nCLK0, nCLK1	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15	0.8	1.2	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			1.2		V_{DD}	V

NOTE 1: Common mode input voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLKx, nCLKx is V_{DD} + 0.3V.

TABLE 4D. LVDS DC CHARACTERISTICS, V_{DD} = 3.3V±5%, T_A = -40°C TO 85°C

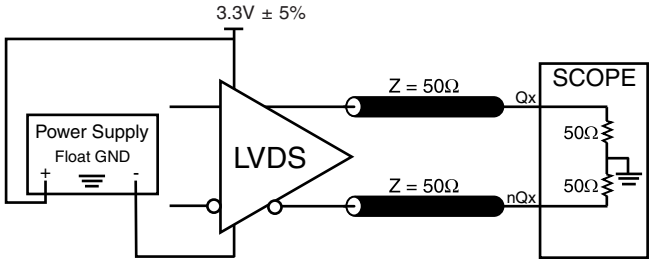
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		200	350	500	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.05	1.15	1.25	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

TABLE 5. AC CHARACTERISTICS, V_{DD} = 3.3V±5%, T_A = -40°C TO 85°C

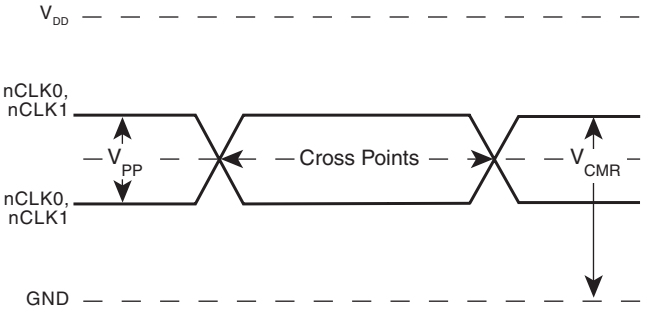
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				>2.5	GHz
t_{PD}	Propagation Delay; NOTE 1		260	360	460	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				100	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	125	160	200	ps
odc	Output Duty Cycle		49		51	%
	MUX Isolation			-55		dB

All parameters measured at ≤ 1GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

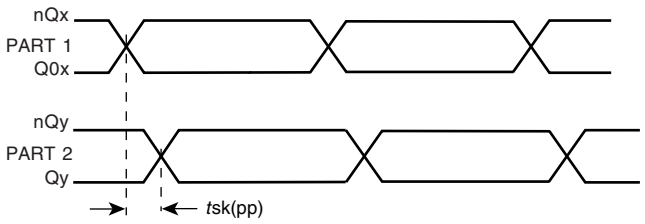
PARAMETER MEASUREMENT INFORMATION



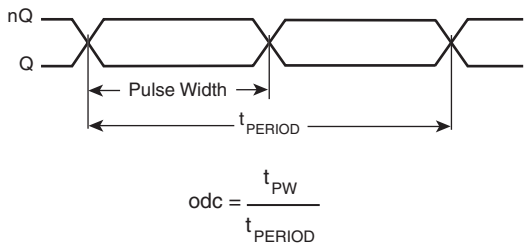
3.3V OUTPUT LOAD AC TEST CIRCUIT



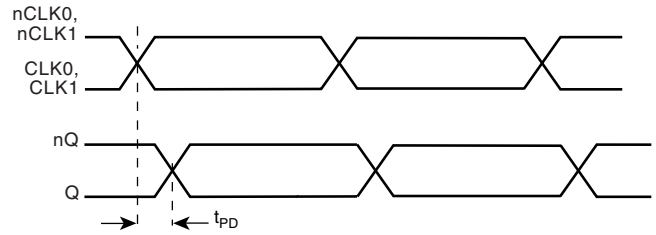
DIFFERENTIAL INPUT LEVEL



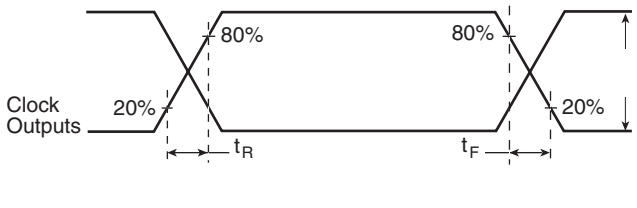
PART-TO-PART SKEW



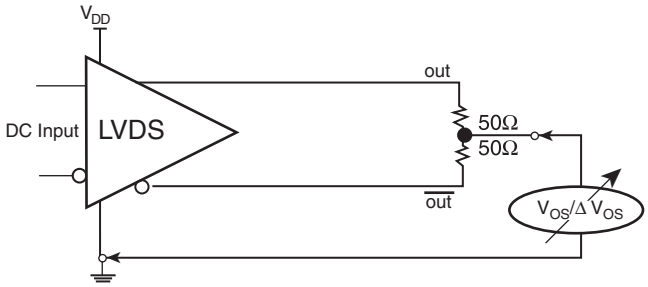
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



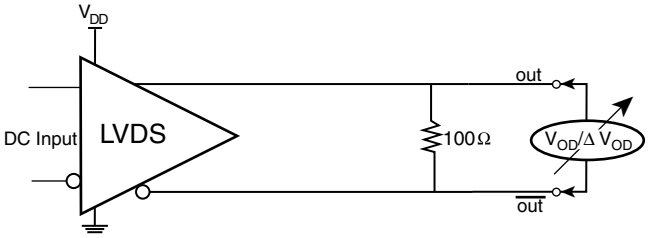
PROPAGATION DELAY



OUTPUT RISE/FALL TIME



OFFSET VOLTAGE SETUP



DIFFERENTIAL OUTPUT VOLTAGE SETUP

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

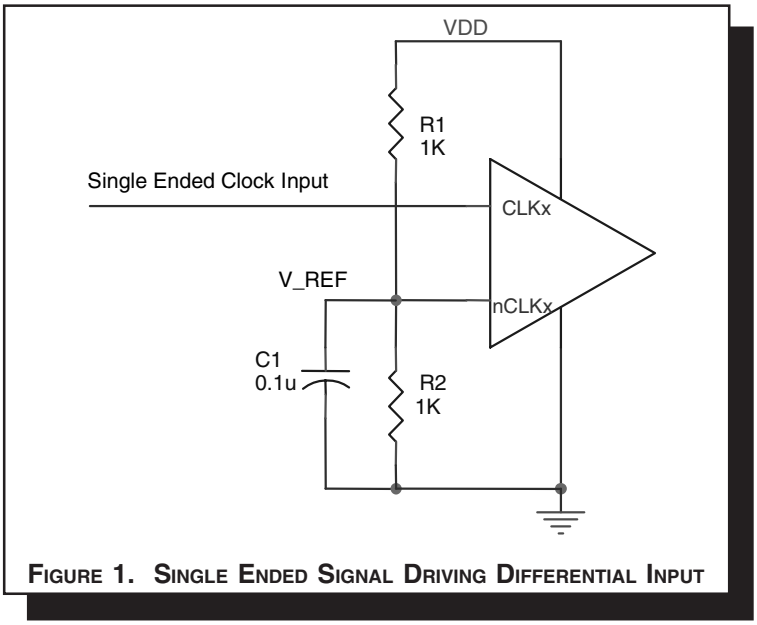


FIGURE 1. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

3.3V LVDS DRIVER TERMINATION

A general LVDS interface is shown in Figure 2. In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the un-used outputs.

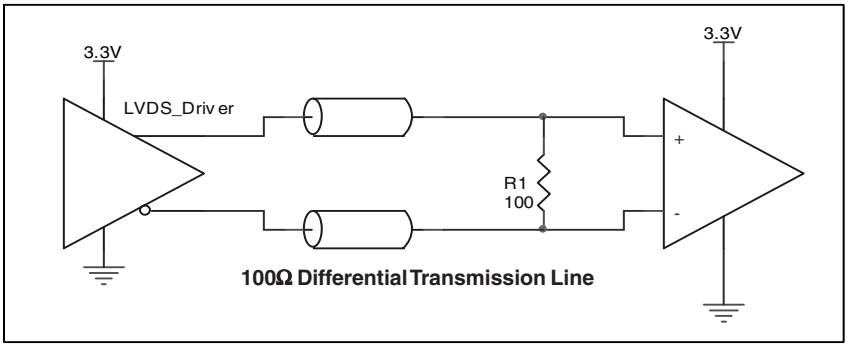


FIGURE 2. TYPICAL LVDS DRIVER TERMINATION

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3E* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

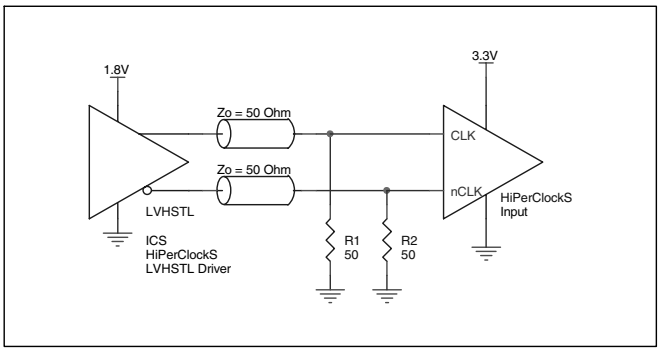


FIGURE 3A. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY ICS HIPERCLOCKS LVHSTL DRIVER

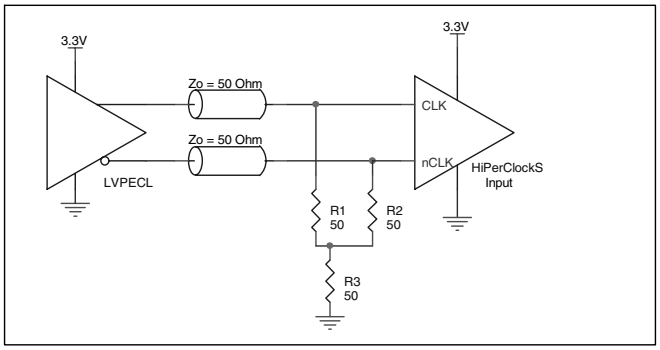


FIGURE 3B. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

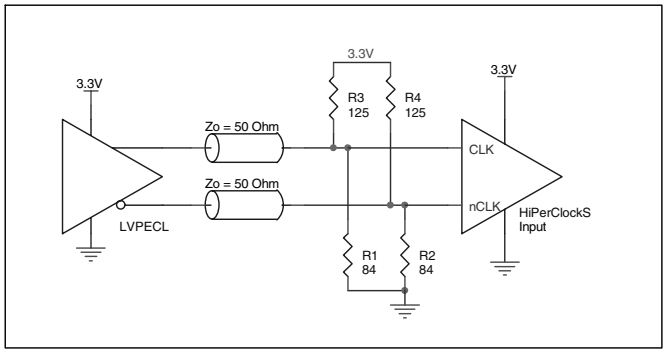


FIGURE 3C. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

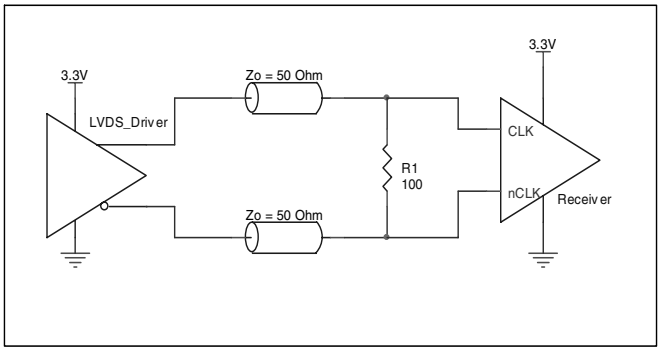


FIGURE 3D. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

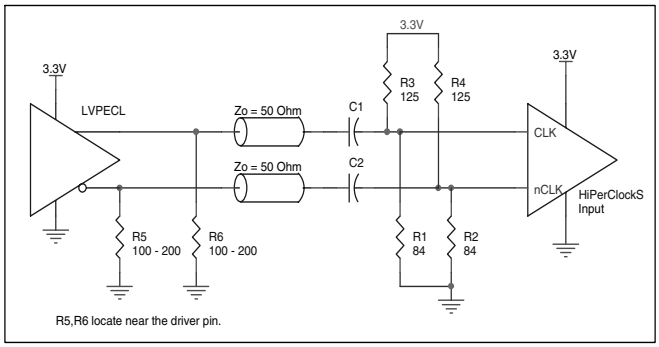


FIGURE 3E. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE

APPLICATION SCHEMATIC EXAMPLE

Figure 4 shows an example of ICS85401 application schematic. This device can accept different types of input signal. In this example, the input is driven by a LVDS driver. The decoupling capacitor should be located as close as possible to the power pin.

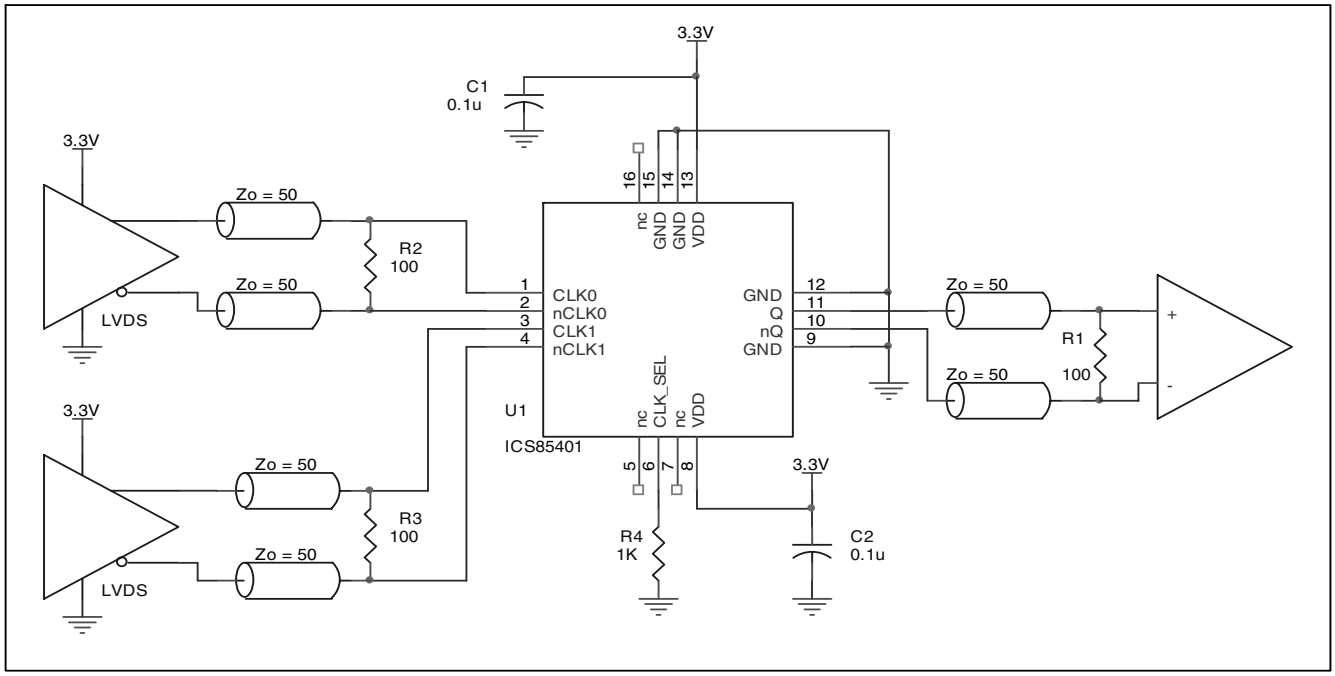


FIGURE 4. ICS85401 APPLICATION SCHEMATIC EXAMPLE

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD VFQFN

θ_{JA} by Velocity (Linear Feet per Minute)	
	0
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W

TRANSISTOR COUNT

The transistor count for ICS85401 is: 132

PACKAGE OUTLINE - K SUFFIX FOR 16 LEAD VFQFN

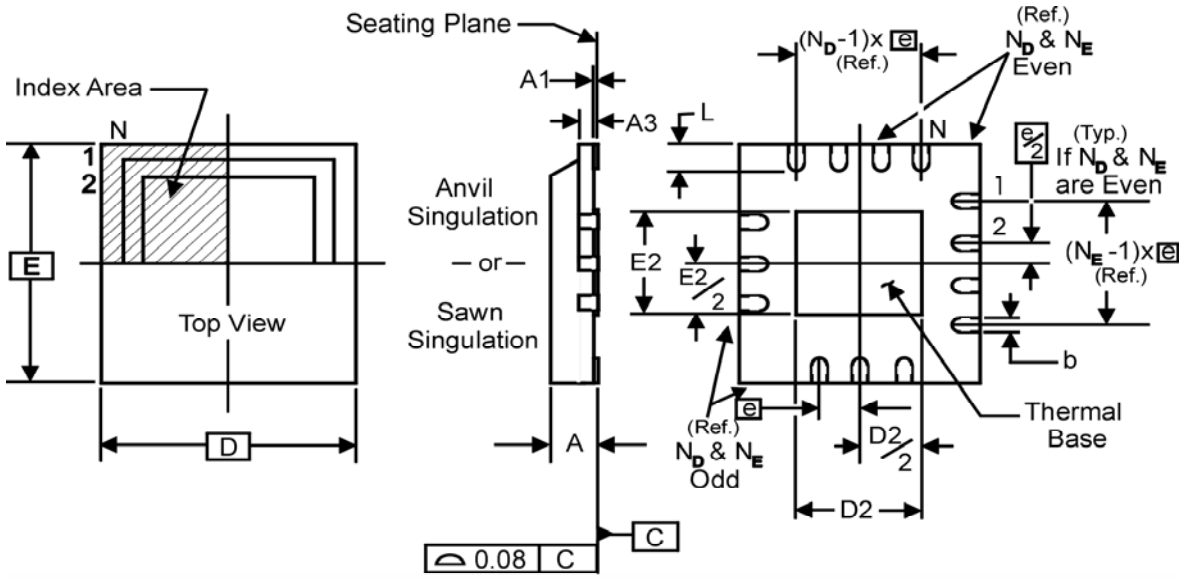


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**MINIMUM**	**MAXIMUM**
N	16	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	4	
N_E	4	
D	3.0	
D2	0.25	1.25
E	3.0	
E2	0.25	1.25
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS85401AK	401A	16 Lead VFQFN	Tray	-40°C to 85°C
ICS85401AKT	401A	16 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A		8	Add Schematic Layout.	8/23/04
A	T8	10	Corrected count in Ordering Information Table	11/17/04
A		1	Pin Assignment - corrected label on pin 2.	2/22/05