# HM62832H Series

32768-word × 8-bit High Speed CMOS Static RAM

HITACHI

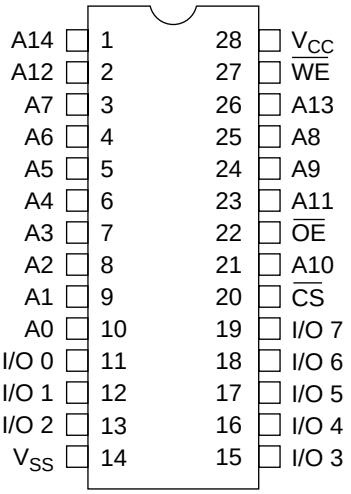
## Features

- High speed: Fast access time 25/35/45 ns (max)
- Low power
  Active: 300 mW (typ)
  Standby: 10 μW (typ) (L-version)
- Single 5 V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output – Three state output
- Directly TTL compatible – All inputs and outputs

## Ordering Information

| Type No. | Access Time | Package |
|---|---|---|
| HM62832HP-25 | 25 ns | 300-mil 28-pin plastic DIP (DP-28NA) |
| HM62832HP-35 | 35 ns | |
| HM62832HP-45 | 45 ns | |
| HM62832HLP-25 | 25 ns | |
| HM62832HLP-35 | 35 ns | |
| HM62832HLP-45 | 45 ns | |
| HM62832HJP-25 | 25 ns | 300-mil 28-pin plastic SOJ (CP-28DN) |
| HM62832HJP-35 | 35 ns | |
| HM62832HJP-45 | 45 ns | |
| HM62832HLJP-25 | 25 ns | |
| HM62832HLJP-35 | 35 ns | |
| HM62832HLJP-45 | 45 ns | |

## Pin Arrangement

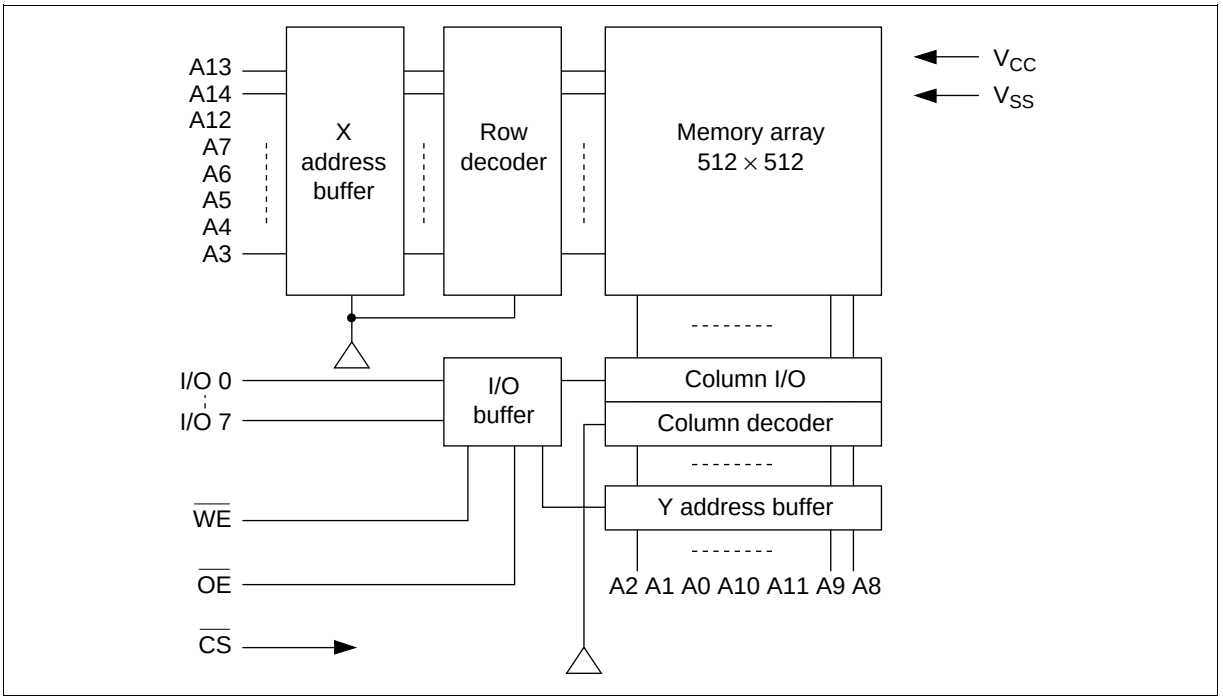



(Top view)

## Pin Description

| Pin Name | Function |
|---|---|
| A0 – A14 | Address |
| I/O0 – I/O7 | Input/output |
| $\overline{CS}$ | Chip select |
| $\overline{WE}$ | Write enable |
| $\overline{OE}$ | Output enable |
| $V_{CC}$ | Power supply |
| $V_{SS}$ | Ground |

## Block Diagram




## Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | $V_T$ | –0.5 [*1] to +7.0 | V |
| Power dissipation | $P_T$ | 1.0 | W |
| Operating temperature | Topr | 0 to +70 | °C |
| Storage temperature | Tstg | –55 to +125 | °C |
| Storage temperature under bias | Tbias | –10 to +85 | °C |

Note: 1. –2.5 V for pulse width ≤ 10 ns

## Function Table

| $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | Mode | $V_{cc}$ Current | I/O Pin | Ref. Cycle |
|---|---|---|---|---|---|---|
| H | X | X | Not selected | $I_{SB}$, $I_{SB1}$ | High-Z | |
| L | L | H | Read | $I_{CC}$ | Dout | Read cycle (1) to (3) |
| L | H | L | Write | $I_{CC}$ | Din | Write cycle (1) |
| L | L | L | | $I_{CC}$ | Din | Write cycle (2) |

Note: X: H or L

## Recommended DC Operating Conditions (Ta = 0 to +70°C)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| | $V_{SS}$ | 0 | 0 | 0 | V |
| Input voltage | $V_{IH}$ | 2.2 | — | 6.0 | V |
| | $V_{IL}$ | –0.5 *1 | — | 0.8 | V |

Note: 1. –2.0 V for pulse width ≤ 10 ns

## DC Characteristics (Ta = 0 to +70°C, $V_{CC}$ = 5 V ± 10%, $V_{SS}$ = 0 V)

| Parameter | Symbol | Min | Typ*1 | Max | Unit | Test Conditions | Note |
|---|---|---|---|---|---|---|---|
| Input leakage current | $\|I_{LI}\|$ | — | — | 2 | µA | Vin = $V_{SS}$ to $V_{CC}$ | |
| Output leakage current | $\|I_{LO}\|$ | — | — | 2 | µA | $\overline{CS}$ = $V_{IH}$ or $\overline{OE}$ = $V_{IH}$ or $\overline{WE}$ = $V_{IL}$, $V_{I/O}$ = $V_{SS}$ to $V_{CC}$ | |
| Operating power supply current | $I_{CC}$ | — | 60 | 120 | mA | Min cycle, duty = 100%, $\overline{CS}$ = $V_{IL}$, $I_{I/O}$ = 0 mA | |
| Standby power supply current | $I_{SB}$ | — | 15 | 30 | mA | $\overline{CS}$ = $V_{IH}$ | |
| Standby power supply current | $I_{SB1}$ | — | 0.02 | 2 | mA | $\overline{CS}$ ≥ $V_{CC}$ – 0.2 V, 0 V ≤ Vin ≤ 0.2 V or Vin ≥ $V_{CC}$ – 0.2 V | |
| | | — | 0.002 | 0.1 | mA | | L-version |
| Output voltage | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 8 mA | |
| | $V_{OH}$ | 2.4 | — | — | V | $I_{OH}$ = –4 mA | |

Note: 1. Typical values are at $V_{CC}$ = 5.0 V, Ta = +25°C and not guaranteed.

## Capacitance (Ta = 25°C, f = 1.0 MHz)*1

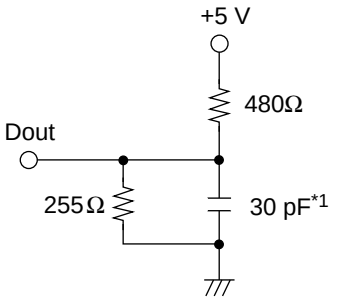
| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input capacitance | Cin | — | — | 6 | pF | Vin = 0 V |
| Input/output capacitance | $C_{I/O}$ | — | — | 10 | pF | $V_{I/O}$ = 0 V |

Note: 1. This parameter is sampled and not 100% tested.

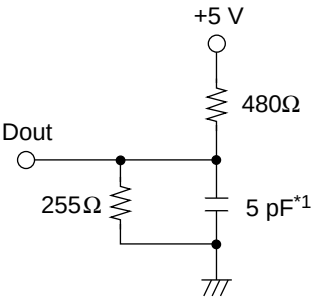
## AC Characteristics (Ta = 0 to +70°C, $V_{CC}$ = 5 V ± 10%, unless otherwise noted.)

### Test Conditions

- Input pulse levels: 0.0 V to 3.0 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures




Output load (A)




Output load (B)
(for $t_{CLZ}$, $t_{OLZ}$, $t_{CHZ}$, $t_{OHZ}$, $t_{WHZ}$ and $t_{OW}$)

Note: 1. Including scope and jig

### Read Cycle

| | | HM62832H-25 | | HM62832H-35 | | HM62832H-45 | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Note** |
| Read cycle time | $t_{RC}$ | 25 | — | 35 | — | 45 | — | ns | |
| Address access time | $t_{AA}$ | — | 25 | — | 35 | — | 45 | ns | |
| Chip select access time | $t_{ACS}$ | — | 25 | — | 35 | — | 45 | ns | |
| Output enable to output valid | $t_{OE}$ | — | 12 | — | 15 | — | 20 | ns | |
| Output hold from address change | $t_{OH}$ | 5 | — | 5 | — | 5 | — | ns | 6 |
| Chip selection to output in low-Z | $t_{CLZ}$ | 5 | — | 5 | — | 5 | — | ns | 1 |
| Output enable to output in low-Z | $t_{OLZ}$ | 0 | — | 0 | — | 0 | — | ns | 1 |
| Chip deselection to output in high-Z | $t_{CHZ}$ | 0 | 12 | 0 | 15 | 0 | 20 | ns | 1 |
| Output enable to output in high-Z | $t_{OHZ}$ | 0 | 12 | 0 | 15 | 0 | 20 | ns | 1 |

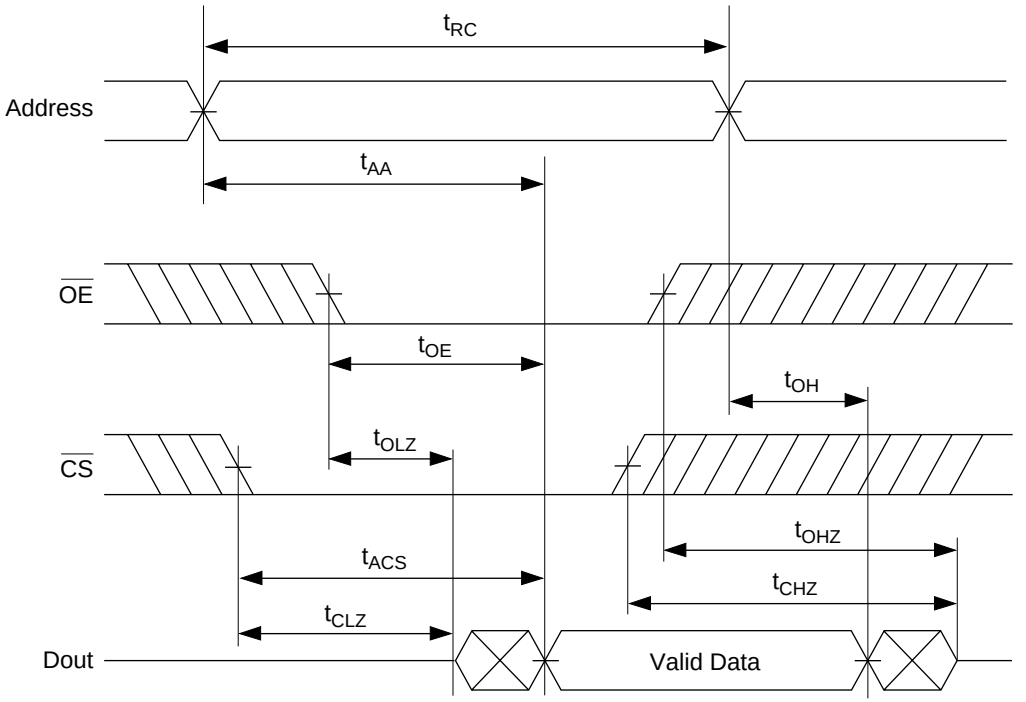
### Write Cycle

| | | HM62832H-25 | | HM62832H-35 | | HM62832H-45 | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| Write cycle time | $t_{WC}$ | 25 | — | 35 | — | 45 | — | ns | |
| Chip selection to end of write | $t_{CW}$ | 15 | — | 20 | — | 25 | — | ns | |
| Address valid to end of write | $t_{AW}$ | 20 | — | 30 | — | 40 | — | ns | |
| Address setup time | $t_{AS}$ | 0 | — | 0 | — | 0 | — | ns | |
| Write pulse width | $t_{WP}$ | 15 | — | 20 | — | 25 | — | ns | 3 |
| Write recovery time | $t_{WR}$ | 0 | — | 0 | — | 0 | — | ns | 4 |
| Write to output in high-Z | $t_{WHZ}$ | 0 | 12 | 0 | 15 | 0 | 20 | ns | 2, 5 |
| Data to write time overlap | $t_{DW}$ | 12 | — | 15 | — | 20 | — | ns | |
| Data hold from write time | $t_{DH}$ | 0 | — | 0 | — | 0 | — | ns | |
| Output disable to output in high-Z | $t_{OHZ}$ | 0 | 12 | 0 | 15 | 0 | 20 | ns | 2, 5 |
| Output active from end of write | $t_{OW}$ | 5 | — | 5 | — | 5 | — | ns | 2, 7 |

Notes:
1. Transition is measured ±200 mV from steady state voltage with load (B). This parameter is sampled and not 100% tested.
2. Transition is measured ±200 mV from high impedance voltage with load (B). This parameter is sampled and not 100% tested.
3. A write occurs during the overlap ($t_{WP}$) of a low $\overline{CS}$ and a low $\overline{WE}$.
4. $t_{WR}$ is measured from the ealier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
5. During this period, I/O pins are in the output state. The input signals out of phase must not be applied.
6. Dout is in the same phase of written data of this write cycle.
7. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The input signals out of phase must not be applied to I/O pins.

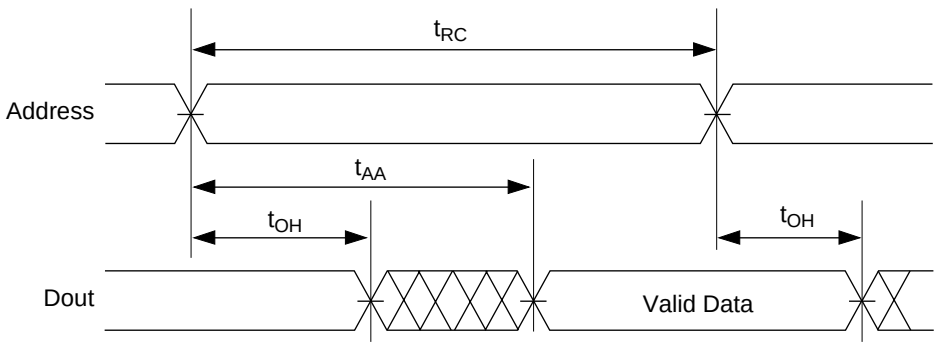
## Timing Waveforms

**Read Cycle Timing–1**[*1] ($\overline{WE}$ = $V_{IH}$)

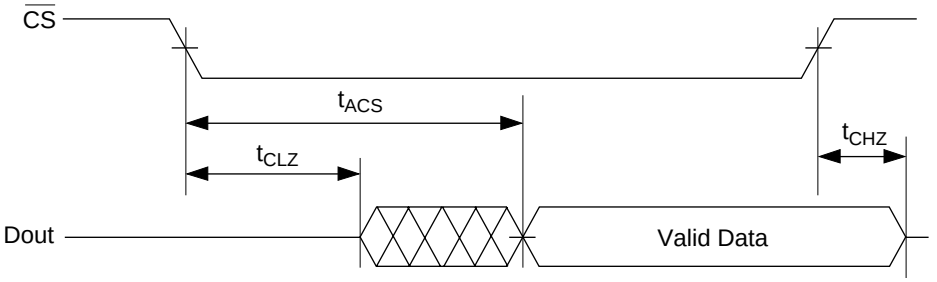



Note: 1. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

**Read Cycle Timing–2** ($\overline{WE}$ = $V_{IH}$, $\overline{CS}$ = $V_{IL}$, $\overline{OE}$ = $V_{IL}$)

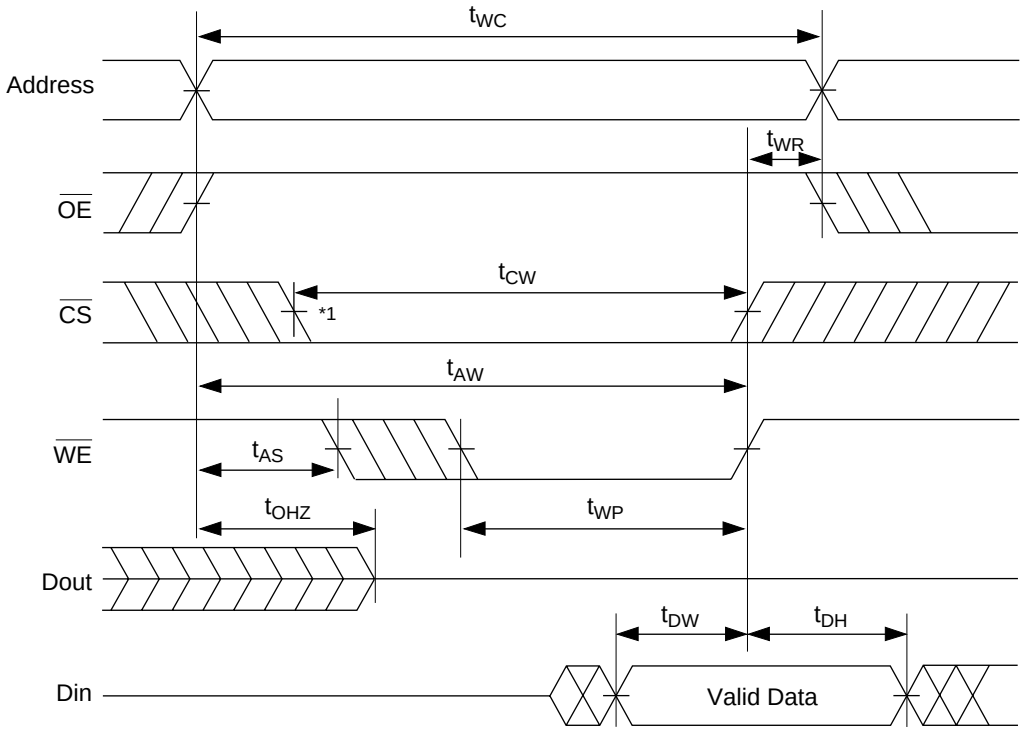


**Read Cycle Timing–3**[*1] ($\overline{WE}$ = $V_{IH}$, $\overline{OE}$ = $V_{IL}$)



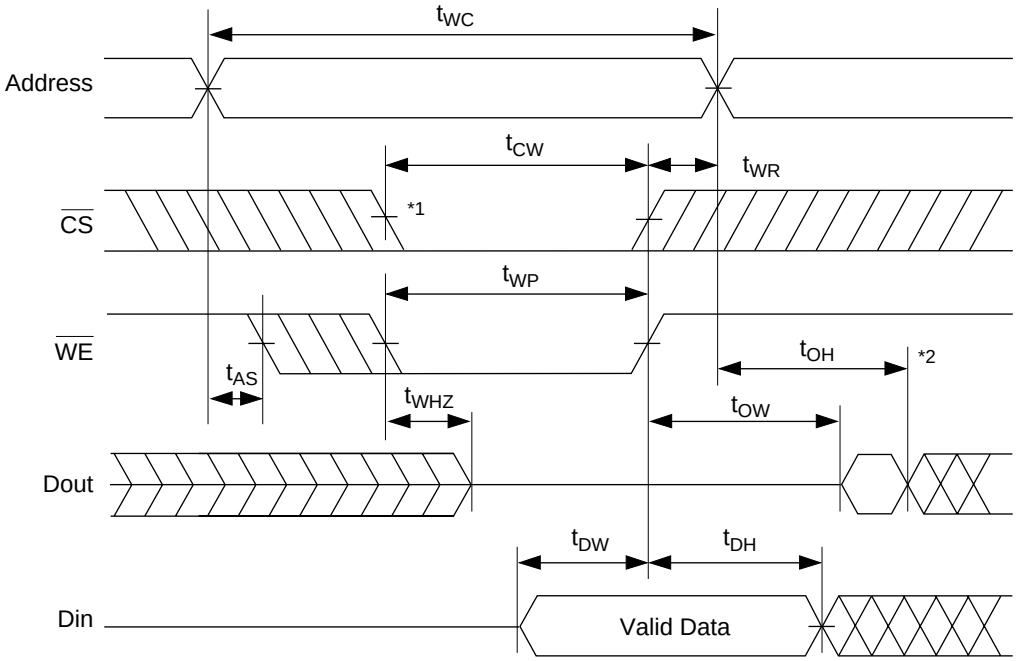

Notes: 1. Transition is measured ±200 mV from steady state voltage with load (B).
This parameter is sampled and not 100% tested.
2. Address should be valid prior to or coincident with $\overline{CS}$ transition low.

**Write Cycle Timing–1**[*2]




Notes: 1. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
2. $\overline{WE}$ must be high during all address transitions except when device is deselected with $\overline{CS}$.

**Write Cycle Timing–2**[*3] (OE Low Fixed)




Notes: 1. If the CS low transition occurs simultaneously with the WE low transition or after the WE low transition, outputs remain in a high impedance state.

2. Dout is the read data of next address.

3. WE must be high during all address transitions except when device is deselected with CS.

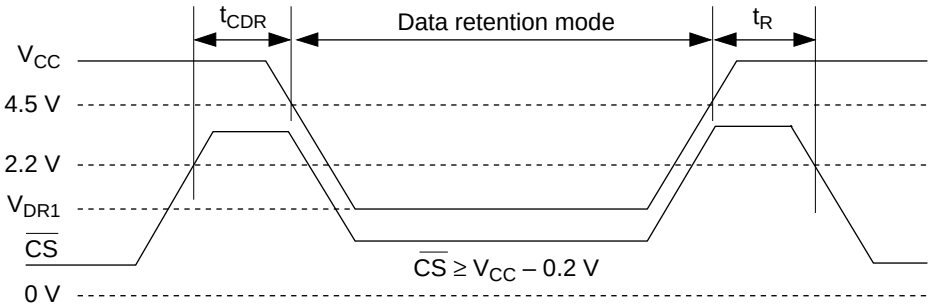
## Low $V_{CC}$ Data Retention Characteristics (Ta = 0 to +70°C)

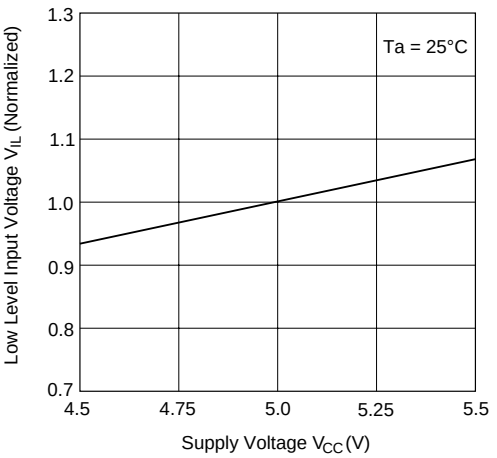
This characteristics is guaranteed only for L-version.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{CC}$ for data retention | $V_{DR}$ | 2.0 | — | — | V | $\overline{CS} \geq V_{CC} - 0.2$ V, Vin $\geq V_{CC} - 0.2$ V or 0 V ≤ Vin ≤ 0.2 V |
| Data retention current | $I_{CCDR}$ | — | 1 | 50*1 | µA | |
| Chip deselect to data retention time | $t_{CDR}$ | 0 | — | — | ns | |
| Operation recovery time | $t_R$ | 5 | — | — | ms | |

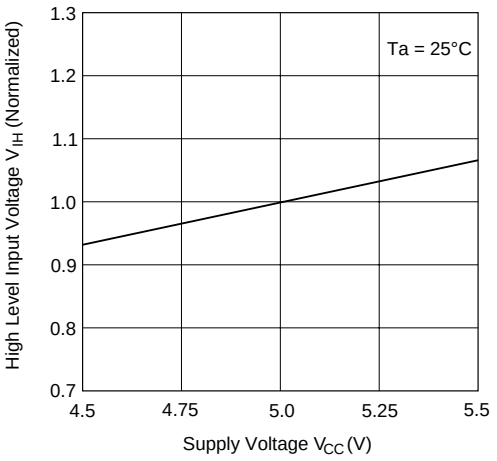
Note: 1. $V_{CC}$ = 3.0 V

### Low $V_{CC}$ Data Retention Timing Waveform

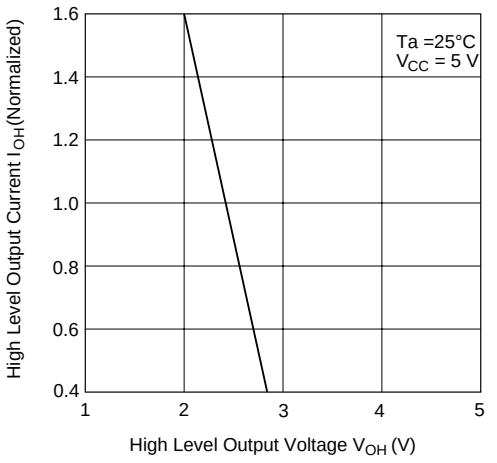


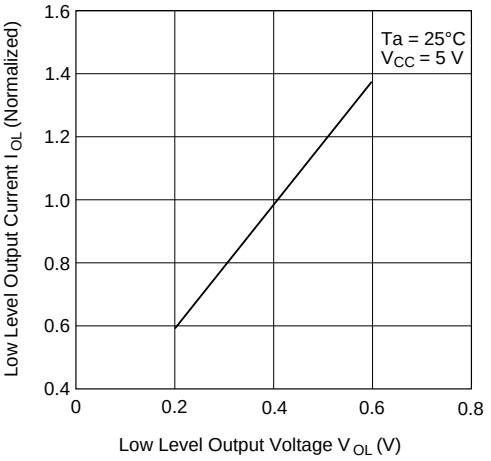

**Low Level Input Voltage vs. Supply Voltage**



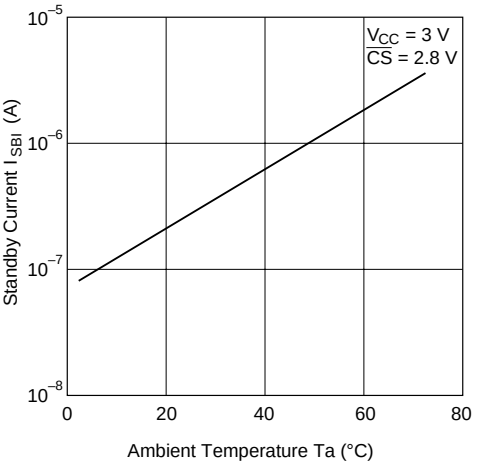

**High Level Input Voltage vs. Supply Voltage**



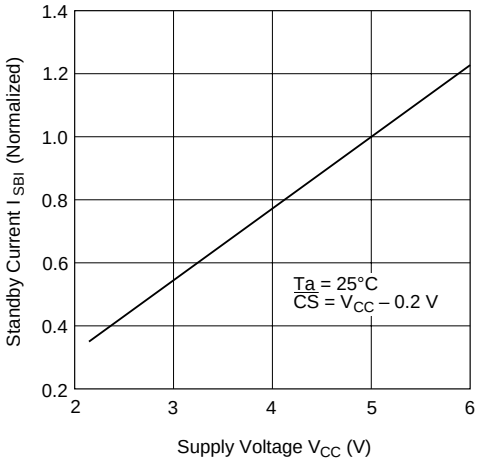

**High Level Output Current vs. High Level Output Voltage**



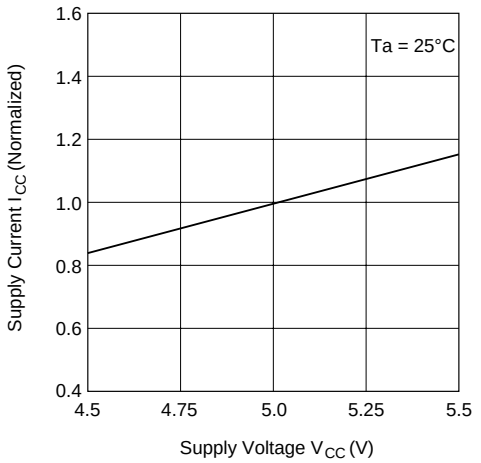

**Low Level Output Current vs. Low Level Output Voltage**



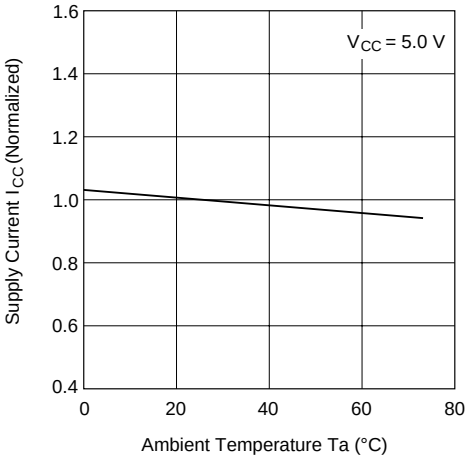

**Standby Current vs. Ambient Temperature**



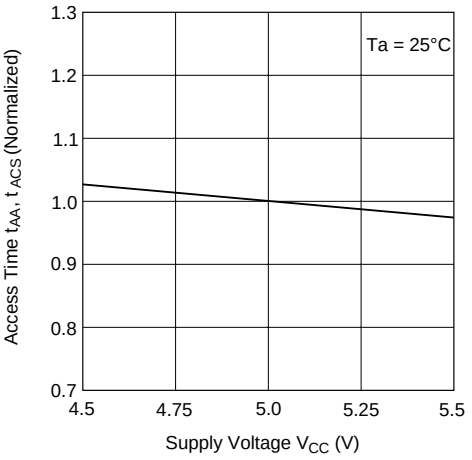

**Standby Current vs. Supply Voltage**



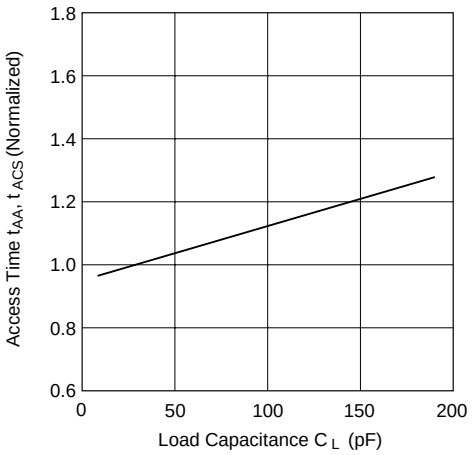

**Supply Current vs. Supply Voltage**



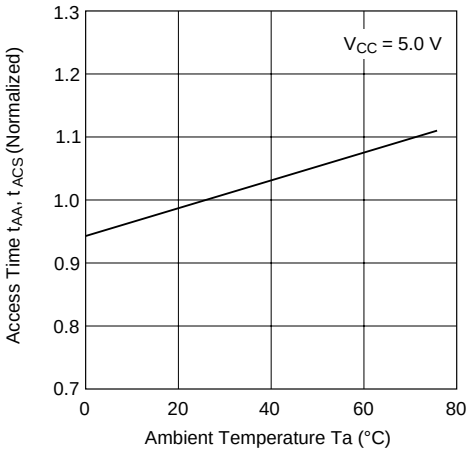

**Supply Current vs. Ambient Temperature**



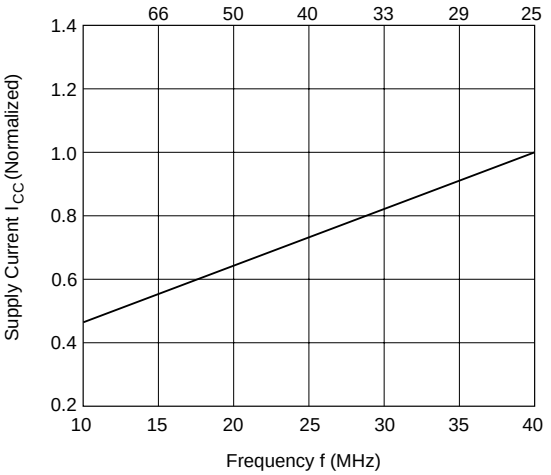

**Access Time vs. Supply Voltage**




**Access Time vs. Load Capacitance**



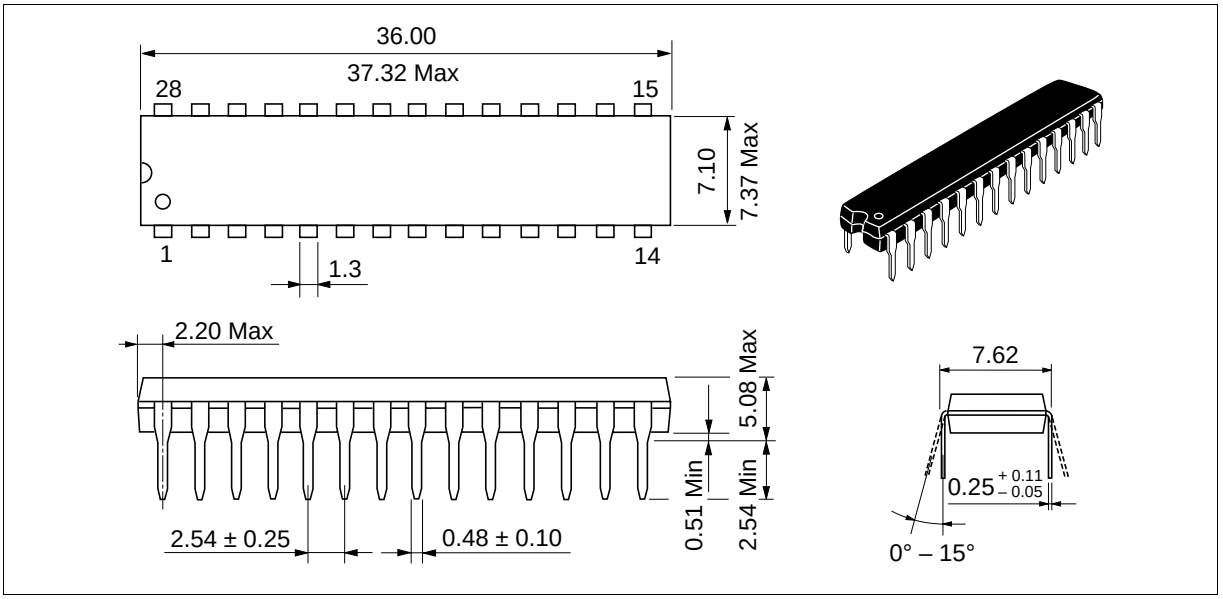

**Access Time vs. Ambient Temperature**




**Supply Current vs. Frequency**

## Package Dimensions

**HM62832HP/HLP Series** (DP-28NA) Unit: mm




**HM62832HJP/HLJP Series** (CP-28DN) Unit: mm