FM3808
256Kb Bytewide FRAM w/ Real-Time Clock

Features

256K bit Ferroelectric Nonvolatile RAM
- Organized as 32,752 x 8 bits
- High Endurance 100 Billion (10^{11}) Read/Writes
- 10 year Data Retention
- NoDelay™ Writes
- 70 ns Access Time/ 130 ns Cycle Time
- Built-in Low V_{DD} Protection

Real-Time Clock/Calendar Function
- Clock Registers in Top 16 bytes of Address Space
- Battery Backed Power
- Tracks Seconds through Centuries in BCD Format
- Tracks Leap Years through 2099
- Runs from a 32.768 kHz Timekeeping Crystal

System Supervisor Function
- Programmable Clock/Calendar Alarm
- Programmable Watchdog Timer
- Power Supply Monitor
- Interrupt Output - Programmable Active High/Low
- Control Settings Inherently Nonvolatile
- Generates either Processor Reset or Interrupt

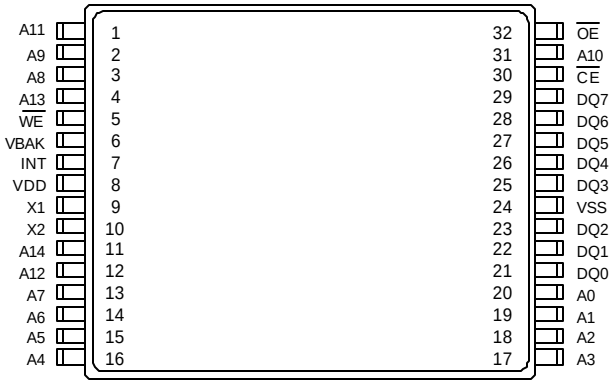
Low Power Operation
- 5V Operation for Memory and Clock Interface
- Backup Voltage as low as 2.5V
- 25 mA I_{DD} Active Current
- 1 µA I_{BAK} Clock Backup Current

Description

The FM3808 combines a 256Kb FRAM array with a real-time clock and a system supervisor function. An external 32.768 kHz crystal drives the timekeeping function. It maintains time and date settings in the absence of system power through the use of a backup battery power source. Data in the memory array does not depend on the backup source, it remains nonvolatile in FRAM. In addition to timekeeping, the FM3808 includes a system supervisor to manage low V_{DD} power conditions and a watchdog timer function. A programmable interrupt output pin allows the user to select the supervisor functions and the polarity of the signal.

Both the FRAM array and the timekeeping function are accessed through the memory interface. The upper 16-address locations of the memory space are allocated to the timekeeping registers rather than to memory. The FRAM array provides data retention for 10 years in the absence of system power, and is not dependent on the backup power source for the clock. This eliminates system concerns over data loss in a traditional battery-backed RAM solution. In addition, clock and supervisor control settings are implemented in FRAM rather than battery-backed RAM, making them more dependable. The FM3808 offers guaranteed operation over an industrial temperature range of -40°C to +85°C.

Pin Configuration



Ordering Information	
FM3808-70-T	70 ns access, 32-pin TSOP
FM3808DK	DIP module development kit

Documentation for the DIP module development kit is available separately.

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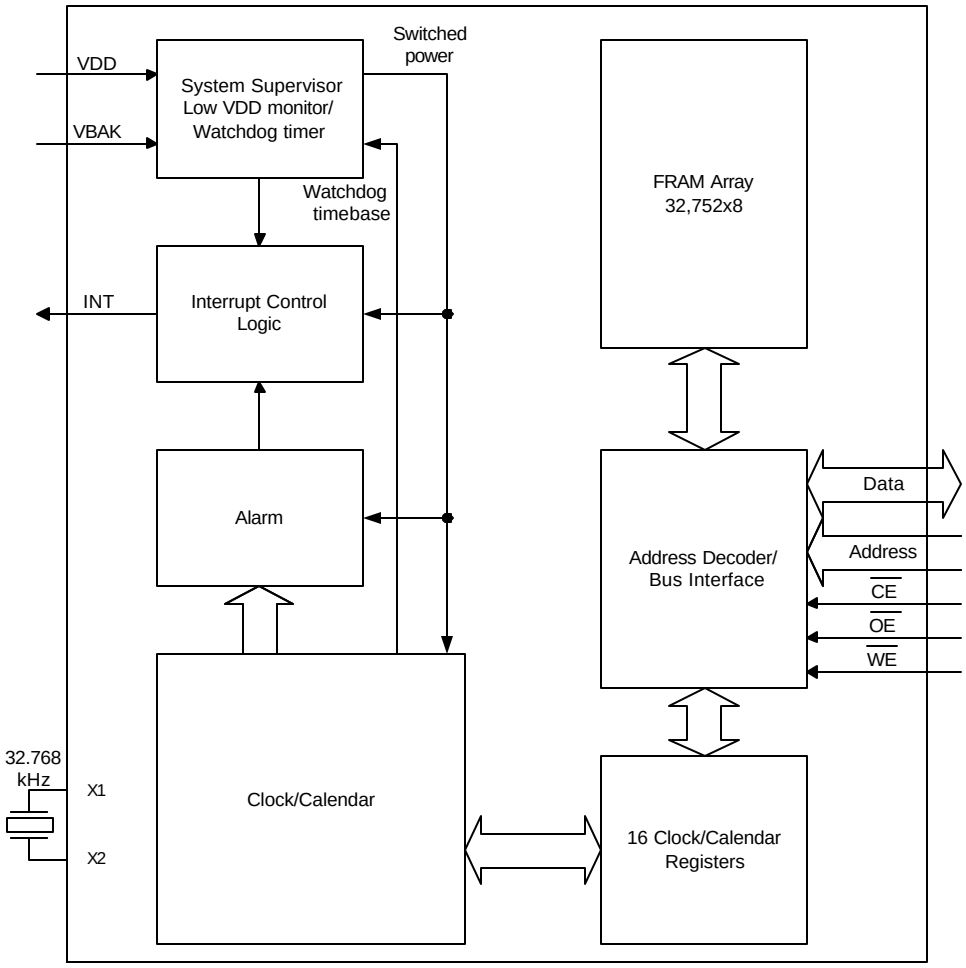


Figure 1. Block Diagram

Pin Description

Pin Name	I/O	Pin Description
A0-A14	Input	Address: The 15 address inputs select one of 32,752 bytes in the FRAM array or one of 16 bytes in the clock/calendar. The address is latched on the falling edge of /CE.
DQ(7:0)	I/O	Data: Bi-directional 8-bit data bus for accessing the FRAM array and clock.
/CE	Input	Chip Enable: The active low /CE input selects the device. The falling edge of /CE internally latches the address. Address changes that occur after /CE has transitioned low are ignored until the next falling edge occurs.
/OE	Input	Output Enable: The active low /OE input enables the data output buffers during read cycles. Deasserting /OE high causes the DQ pins to tri-state.
/WE	Input	Write Enable: The active low /WE low enables data on the DQ pins to be written to the address location latched by the falling edge of /CE.
X1, X2	Input	Connect 32.768 kHz crystal.
INT	Output	Interrupt output: This output can be programmed to respond to the clock/calendar alarm, the watchdog timer, and the power monitor. It is programmable to either active high (push/pull) or active low (open-drain).
V_{BAK}	Supply	Backup Supply Voltage: This supply is used to maintain power for the clock. It must remain above 2.5V to keep battery-backed functions active. V_{BAK} is supplied by a battery. Current I_{BAK} is drawn from V_{BAK} when V_{DD} is below the V_{BAK} voltage.
V_{DD}	Supply	Supply Voltage: 5V
V_{SS}	Supply	Ground.

Functional Truth Table

/CE	/WE	/OE	Function
H	X	X	Standby/Precharge
↘	X	X	Latch Address
L	H	L	Read
L	L	X	Write

Overview

The FM3808 integrates three complementary but distinct functions under a common interface in a single package. First, is the 32Kx8 FRAM memory block (minus 16 bytes), second is the real-time clock/calendar, and third is the system supervisor. The functions are integrated to enhance their individual performance, so that each provides better capability than three similar stand-alone devices. All functions use the same bytewide address/data interface and are memory mapped. Special functions, including the clock/calendar and supervisor system, are controlled via registers that reside in the top of the combined memory map. The register map is described below, followed by a detailed description of each functional block.

Register Map

The top 16 FRAM address locations control the clock/calendar, alarm, and supervisor functions. The registers contain timekeeping data, control bits, or information flags. A short description of each register follows. Detailed descriptions of each function follow the register summary.

Register Map Summary Table

				Data						
Address	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Function**	**Range**
7FFFh		10 years				years			Years	00-99
7FFEh	0	0	0	10 mo		months			Month	1-12
7FFDh	0	0	10 date			date			Date	1-31
7FFCh	0	0	0	0	0	day			Day	1-7
7FFBh	0	0	10 hours			hours			Hours	0-23
7FFAh	0	10 minutes				minutes			Minutes	0-59
7FF9h	0	10 seconds				seconds			Seconds	0-59
7FF8h	/OSCEN	reserved	reserved	CALS	CAL3	CAL2	CAL1	CAL0	Control-NV	
7FF7h	WDS	/WDW	WDT5	WDT4	WDT3	WDT2	WDT1	WDT0	Watchdog	
7FF6h	WIE	AIE	PFE	ABE	H/L	P/L	reserved	reserved	Interrupts	
7FF5h	/Match	0	Alarm 10 date			Alarm date			Alarm Date	1-31
7FF4h	/Match	0	Alarm 10 hours			hours			Alarm Hours	0-23
7FF3h	/Match	Alarm 10 minutes				Alarm minutes			Alarm Minutes	0-59
7FF2h	/Match	Alarm 10 seconds				Alarm seconds			Alarm Seconds	0-59
7FF1h									User-NV	
7FF0h	WDF	AF	PF	CF	TST	CAL	W	R	Flags/Control	

Note that the shaded register bits are implemented in FRAM, therefore data at these locations is retained even without backup power.

Table 1. Register Map

Address	Description							
7FFFh	**Timekeeping – Years**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	10 year.3	10 year.2	10 year.1	10 year.0	Year.3	Year.2	Year.1	Year.0
	Contains the lower two BCD digits of the year. Lower nibble contains the value for years; upper nibble contains the value for 10s of years. Each nibble operates from 0 to 9. The range for the register is 0-99.							
7FFEh	**Timekeeping – Months**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	0	10 Month	Month.3	Month.2	Month.1	Month.0
	Contains the BCD digits for the month. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (one bit) contains the upper digit and operates from 0 to 1. The range for the register is 1-12.							
7FFDh	**Timekeeping – Date of the month**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	10 date.1	10 date.0	Date.3	Date.2	Date.1	Date.0
	Contains the BCD digits for the date of the month. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 3. The range for the register is 1-31.							
7FFCh	**Timekeeping – Day of the week**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	0	0	0	Day.2	Day.1	Day.0
	Lower nibble contains a value that correlates to day of the week. Day of the week is a ring counter that counts from 1 to 7 then returns to 1. The user must assign meaning to the day value, as the day is not integrated with the date.							
7FFBh	**Timekeeping – Hours**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	10 hours.1	10 hours.0	Hours.3	Hours2	Hours.1	Hours.0
	Contains the BCD value of hours in 24-hour format. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the upper digit and operates from 0 to 2. The range for the register is 0-23.							
7FFAh	**Timekeeping – Minutes**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	10 min.2	10 min.1	10 min.0	Min.3	Min.2	Min.1	Min.0
	Contains the BCD value of minutes. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper minutes digit and operates from 0 to 5. The range for the register is 0-59.							
7FF9h	**Timekeeping – Seconds**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	10 sec.2	10 sec.1	10 sec.0	Seconds.3	Seconds.2	Seconds.1	Seconds.0
	Contains the BCD value of seconds. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 5. The range for the register is 0-59.							

Address	Description

7FF8h	Control-Nonvolatile							
	D7	D6	D5	D4	D3	D2	D1	D0
	$\overline{\text{OSCEN}}$	Reserved	Reserved	CALS	CAL.3	CAL.2	CAL.1	CAL.0
/OSCEN	/Oscillator Enable. When set to 1, the oscillator is halted. When set to 0, the oscillator runs. Disabling the oscillator saves battery power during storage. On a no-battery power up, this bit is set to 1. **The RTC will not run until the oscillator is enabled. Set this bit to 0 to activate the RTC.**							
Reserved	Do not use. Should remain set to 0.							
CALS	Calibration sign. Determines if the calibration adjustment is applied as an addition to or as a subtraction from the time-base. This bit is implemented in FRAM. Calibration is explained below							
CAL.3-0	These four bits control the calibration of the clock. These bits are implemented in FRAM.							

7FF7h	Watchdog Timer							
	D7	D6	D5	D4	D3	D2	D1	D0
	WDS	$\overline{\text{WDW}}$	WDT.5	WDT.4	WDT.3	WDT.2	WDT.1	WDT.0
WDS	Watchdog Strobe. Setting this bit to 1 reloads and restarts the watchdog timer. Setting the bit to 0 has no affect. The bit is cleared automatically once the watchdog timer is reset. The WDS bit is write only. Reading it always will return a 0.							
/WDW	Watchdog Write Enable. Setting this bit to 1 masks the watchdog timeout value (WDT.5-0) so it cannot be written. This allows the user to strobe the watchdog without disturbing the timeout value. Setting this bit to 0 allows bits 5-0 to be written on the next write to the Watchdog register. The new value will be loaded on the next internal watchdog clock after the write cycle is complete. This function is explained in more detail in the watchdog Timer section below.							
WDT.5-0	Watchdog Timeout selection. The watchdog timer interval is selected by the 6-bit value in this register. It represents a multiplier of the 32 Hz count (31.25 ms). The minimum range or timeout value is 31.25 ms (a setting of 1) and the maximum timeout is 2 seconds (setting of 3Fh). Setting the watchdog timer register to 0 disables the timer. These bits can be written only if the /WDW bit was cleared to 0 on a previous cycle.							

7FF6h	Interrupts							
	D7	D6	D5	D4	D3	D2	D1	D0
	WIE	AIE	PFE	ABE	H/$\overline{\text{L}}$	P/$\overline{\text{L}}$	Reserved	Reserved
WIE	Watchdog Interrupt Enable. When set to 1 and a watchdog timeout occurs, the watchdog timer drives the INT pin as well as the WDF flag. When set to 0, the watchdog timeout affects only the WDF flag.							
AIE	Alarm Interrupt Enable. When set to 1, the alarm match drives the INT pin as well as the AF flag. When set to 0, the alarm match only affects the AF flag.							
PFE	Power-Fail Enable. When set to 1, the power-fail monitor drives the pin as well as the PF flag. When set to 0, the power-fail monitor affects only the PF flag.							
ABE	Alarm Battery-backup Enable. When set to 1, the alarm interrupt (as controlled by AIE) will function even in battery backup mode. When set to 0, the alarm will occur only when VDD>VLO.							
H/L	High/Low. When set to a 1, the INT pin is push/pull active high. When set to a 0, the INT pin is open drain, active low.							
P/L	Pulse/Level. When set to a 1, the INT pin is driven active (determined by H/L) by an interrupt source for approximately 200 ms. When set to a 0, the INT pin is driven to an active level (as set by H/L) until the Flags/Control register is read.							

7FF5h	Alarm – Date of the month							
	D7	D6	D5	D4	D3	D2	D1	D0
	$\overline{\text{M}}$	0	10 date.1	10 date.0	Date.3	Date.2	Date.1	Date.0
	Contains the alarm value for the date of the month and the mask bit to select or deselect the date value.							
/M	Match. Setting this bit to 0 causes the date value to be used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the date value.							

Address	Description

7FF4h	**Alarm – Hours**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	$\overline{M}$	0	10 hours.1	10 hours.0	Hours.3	Hours2	Hours.1	Hours.0
	Contains the alarm value for the hours and the mask bit to select or deselect the hours value.							
/M	Match: Setting this bit to 0 causes the Hours value to be used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the Hours value.							

7FF3h	**Alarm – Minutes**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	$\overline{M}$	10 min.2	10 min.1	10 min.0	Min.3	Min.2	Min.1	Min.0
	Contains the alarm value for the minutes and the mask bit to select or deselect the minutes value							
/M	Match: Setting this bit to 0 causes the Minutes value to be used in the alarm match. Setting this bit to 1 causes the match circuit to ignore the Minutes value.							

7FF2h	**Alarm – Seconds**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	$\overline{M}$	10 sec.2	10 sec.1	10 sec.0	Seconds.3	Seconds.2	Seconds.1	Seconds.0
	Contains the alarm value for the seconds and the mask bit to select or deselect the minutes value.							
/M	Match: Setting this bit to 0 causes the Seconds value to be used in the alarm match. Setting this bit to1 causes the match circuit to ignore the Seconds value.							

7FF1h	**User-Nonvolatile**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	This register is an uncommitted nonvolatile register.							

7FF0h	**Flags/Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	WDF	AF	PF	CF	TST	CAL	W	R
WDF	Watchdog Timer Flag. This read-only bit is set to 1 when the watchdog timer is allowed to reach 0 without being reset by the user. It is cleared to 0 when the Flags/Control register is read.							
AF	Alarm Flag. This read-only bit is set to 1 when the time and date match the values stored in the alarm registers with the match bit(s) = 0. It is cleared when the Flags/Control register is read.							
PF	Power-fail Flag. This read-only bit is set to 1 when power falls below the power-fail interrupt threshold V_{TP}. It is cleared to 0 when the Flags/Control register is read.							
CF	Century Overflow Flag. This read-only bit is set to a 1 when the values in the years register overflows from 99 to 00. This indicates a new century, such as going from 1999 to 2000 or 2099 to 2100. The user should record the new century information as needed. This bit is cleared to 0 when the Flags/Control register is read.							
TST	Invokes factory test mode. Users should always set this bit to 0.							
CAL	Calibration Mode. When set to 1, the clock enters calibration mode. When CAL is set to 0, the clock operates normally.							
W	Write Time. Setting the W bit to 1 freezes updates of the timekeeping registers. The user can then write them with updated values. Setting the W bit to 0 causes the contents of the time registers to be transferred to the timekeeping counters. This bit affects registers 7FF9h - 7FFFh.							
R	Read Time. Setting the R bit to 1 copies a static image of the timekeeping registers and places them in a holding register. The user can then read them without concerns over changing values causing system errors. The R bit going from 0 to 1 causes the timekeeping capture, so the bit must be returned to 0 prior to reading again. This bit affects registers 7FF9h - 7FFFh.							

Real-Time Clock Operation

The real-time clock (RTC) consists of an oscillator, a clock divider, and a register system to access the information. It divides down the 32.768 kHz time-base to provide the user timekeeping resolution of one second (1Hz). *The RTC will not run until the oscillator is enabled. The ocillator enable bit is bit 7 of register 7FF8h and is automatically set to a one (disabled) when the device powers up without a backup supply.*

Static registers provide the user with read/write access to the time values. The synchronization of these registers with the timekeeper core is performed using R and W bits in register 7FF0h. Setting the R bit from 0 to 1 causes a transfer of the timekeeping information to holding registers that can be read by the user. If a timekeeper update is in progress when the R is set, the update will be completed prior to loading the registers. Another update cannot be performed unless the R bit is first cleared to 0 again.

Setting the W bit causes the timekeeper to freeze updates. Clearing it to 0 causes the values in the time registers to be written into the timekeeper core. Users should be sure not to load invalid values, such as FFh to any of the timekeeping registers.

Updates to the timekeeping core occur continuously except when frozen. A diagram of the timekeeping core is shown in Figure 2.

Backup Power

The real-time clock/calendar is intended for permanently powered operation. When primary system power fails, the V_{DD} voltage will drop. When it crosses the voltage on the V_{BAK} supply pin, the clock/calendar power will switch to the backup power supply V_{BAK}. The supervisor function, described below, controls the switchover process as part of a more complete power management circuit.

The following functions are powered from the backup power source when $V_{DD} < V_{BAK}$ (backup mode) :

- Clock/calendar core
- Alarm interrupt/comparator
- INT pin (determined by ABE & AIE bits); active low only
- Flags connected to related functions

The following functions are not powered and are disabled when $V_{DD} < V_{LO}$:

- User interface
- Watchdog timer
- Power monitor & band-gap ($V_{DD} < \approx 2.0V$)
- Flags connected to related functions
- All FRAM access & updates
- Calibration operation
- INT pin if programmed as active-high

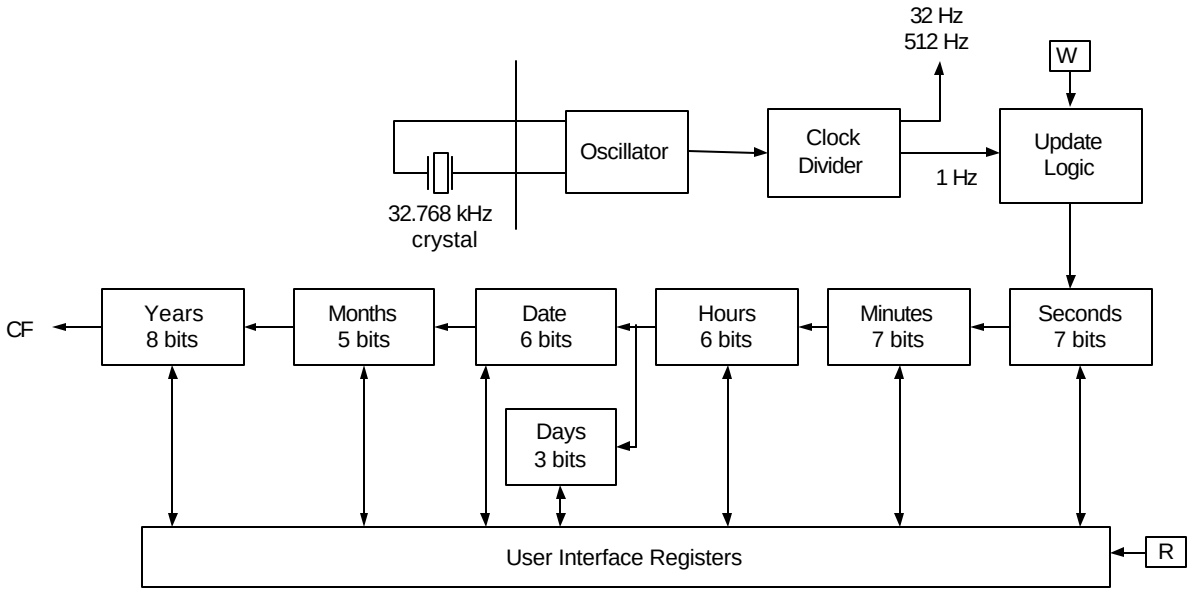


Figure 2. Real-Time Clock Core Block Diagram

Calibration

The RTC enters calibration mode when the CAL bit in register 7FF0h is set to 1. Interrupts are disabled in CAL mode. The RTC is calibrated by applying a digital correction to the RTC logic block. In CAL mode, the INT pin is driven with a 512.00 Hz nominal square wave. Based on the measured deviation from this frequency, a correction value must be written by the user into the calibration register 7FF8h. See Table 2 for the correction codes.

Positive ppm errors require a negative adjustment that removes pulses. Negative ppm errors require a positive correction that adds pulses. Positive ppm adjustments have the CALS bit set to 1, whereas negative ppm adjustments have CALS = 0. After calibration, the clock will have a maximum error of ± 4.34 ppm or ± 0.19 minutes per month at the calibrated temperature.

The calibration setting is nonvolatile and is stored in 7FF8h (bits D4-D0). This value only can be written when the CAL bit is set to a 1. To exit calibration mode, the user must clear the CAL bit to a 0.

When the calibration mode is entered, the user can measure the frequency error on the INT pin. This error expressed in ppm translates directly into timekeeping error. An offsetting calibration adjustment corrects this error. However, the correction is applied by adding or removing pulses on a periodic basis. Therefore, the correction will not appear on the 512 Hz output. The calibration correction must be applied using the values shown in Table 2. The timekeeping accuracy can be verified by comparing the FM3808 time to a reference source.

Table 2. Calibration Adjustments

	Measured Frequency Range		Error Range (ppm)		
	Min	Max	Min	Max	Program Calibration D4-D0
0	512.0000	511.9978	0	4.34	00000b
1	511.9978	511.9933	4.35	13.02	10001b
2	511.9933	511.9889	13.03	21.70	10010b
3	511.9889	511.9844	21.71	30.38	10011b
4	511.9844	511.9800	30.39	39.06	10100b
5	511.9800	511.9756	39.07	47.74	10101b
6	511.9756	511.9711	47.75	56.42	10110b
7	511.9711	511.9667	56.43	65.10	10111b
8	511.9667	511.9622	65.11	73.78	11000b
9	511.9622	511.9578	73.79	82.46	11001b
10	511.9578	511.9533	82.47	91.14	11010b
11	511.9533	511.9489	91.15	99.82	11011b
12	511.9489	511.9444	99.83	108.50	11100b
13	511.9444	511.9400	108.51	117.18	11101b
14	511.9400	511.9356	117.19	125.86	11110b
15	511.9356	511.9311	125.87	134.54	11111b
	Measured Frequency Range		Error Range (ppm)		
	Min	Max	Min	Max	Program Calibration D4-D0
0	512.0000	512.0022	0	4.34	00000b
1	512.0022	512.0067	4.35	13.02	00001b
2	512.0067	512.0111	13.03	21.70	00010b
3	512.0111	512.0156	21.71	30.38	00011b
4	512.0156	512.0200	30.39	39.06	00100b
5	512.0200	512.0244	39.07	47.74	00101b
6	512.0244	512.0289	47.75	56.42	00110b
7	512.0289	512.0333	56.43	65.10	00111b
8	512.0333	512.0378	65.11	73.78	01000b
9	512.0378	512.0422	73.79	82.46	01001b
10	512.0422	512.0467	82.47	91.14	01010b
11	512.0467	512.0511	91.15	99.82	01011b
12	512.0511	512.0556	99.83	108.50	01100b
13	512.0556	512.0600	108.51	117.18	01101b
14	512.0600	512.0644	117.19	125.86	01110b
15	512.0644	512.0689	125.87	134.54	01111b

Supervisor Operation

The Supervisor function includes a clock/calendar alarm, a watchdog timer, and a power monitor. A programmable interrupt pin (INT) provides maximum flexibility to the system designer. The INT pin is designed to allow either reset or interrupt capability to the host processor.

Alarm

The alarm function compares user-programmed values to the corresponding time-of-day values. When a match occurs, the alarm event occurs. The alarm drives an internal flag AF (7FF0 bit D6) and may drive the INT pin if desired.

There are four alarm match fields. They are Date, Hours, Minutes, and Seconds. Each of these fields also has a Match bit that is used to determine if the field is used in the alarm match logic. Setting the Match bit to '0' indicates that the corresponding field will be used in the match process.

Depending on the Match bits, the alarm can occur as specifically as one particular second on one day of the month, or as frequently as once per second continuously. The MSB of each Alarm register is a Match bit. Examples of the Match bit settings are shown in the table below. Selecting none of the match bits (all '1's) indicates that no match is required. The alarm occurs every second. Setting the match select bit for seconds to '0' causes the logic to match the seconds alarm value to the current time of day. Since a match will occur for only one value per minute, the alarm occurs once per minute. Likewise setting the seconds and minutes match select bits causes an exact match of these values. Thus, an alarm will occur once per hour. Setting seconds, minutes, and hours causes a match once per day. Lastly, selecting all match-values causes an exact time and date match. Selecting other bit combinations will not produce meaningful results, however the alarm circuit should follow the functions described.

There are two ways a user can detect an alarm event, by reading the AF flag or monitoring the INT pin. The AF flag in the register 7FF0h (bit D6) will indicate that a date/time match has occurred. The AF bit will be set to 1 when a match occurs. Reading the Flags/Control register clears the alarm flag bit (and all others). A hardware interrupt pin may be used to detect an alarm event. The AIE bit in the register 7FF6h The interrupt function is described below.

Alarm Match Bit Examples

Seconds	Minutes	Hours	Date	Alarm condition
1	1	1	1	No match required = alarm 1/second
0	1	1	1	Alarm when seconds match, = alarm 1/minute
0	0	1	1	Alarm when seconds, minutes match, = alarm 1/hour
0	0	0	1	Alarm when seconds, minutes, hours match, = alarm 1/day
0	0	0	0	Alarm when seconds, minutes, hours, date match, = alarm 1/month

Watchdog Timer

The Watchdog timer is a free running down counter that uses the 32 Hz clock (31.25 ms) derived from the crystal oscillator. The oscillator must be running (/OSCEN=0) for the watchdog to function. It begins counting down from the value loaded in the Watchdog Timer register (7FF7h).

The counter consists of a loadable register and a free running counter. On power up, the watchdog timeout value in 7FF7h is loaded into the counter load register. Counting begins on power up and restarts from the loadable value any time the Watchdog Strobe WDS bit (7FF7h bit D7) is set to 1. The counter is compared to terminal value of 0. If the counter reaches this value, it causes an internal flag and an optional interrupt output (see interrupts below). The user can prevent the timeout interrupt by setting WDS bit to 1 prior to the counter reaching 0. This causes the counter to be reloaded with the watchdog timeout value and to be restarted. As long as the user sets the WDS bit prior to the counter reaching the terminal value, the interrupt and flag never occurs.

New timeout values can be written by setting the watchdog write bit (7FF7h bit D6) to 0. When the /WDW bit is 0 (from a previous operation), new writes to the watchdog timeout value 7FF7h bits D5-D0 allow the timeout value to be modified. When /WDW is a 1, then writes to bits 7FF7h bits D4-D0 will be ignored. The /WDW function allows a user to set the WDS bit without concern that the watchdog timer value will be modified. A logical diagram of the watchdog timer is shown below. Note that setting the watchdog timeout value to 0 would be otherwise meaningless and therefore disables the watchdog function.

The output of the watchdog timer is a flag bit WDF (7FF0h bit D7) that is set if the watchdog is allowed to timeout. The flag is set upon a watchdog timeout and cleared when the Flags/Control register is read by the user. The user can also enable an optional interrupt source to drive the INT pin if the watchdog timeout occurs. The interrupt function is described on page 13.

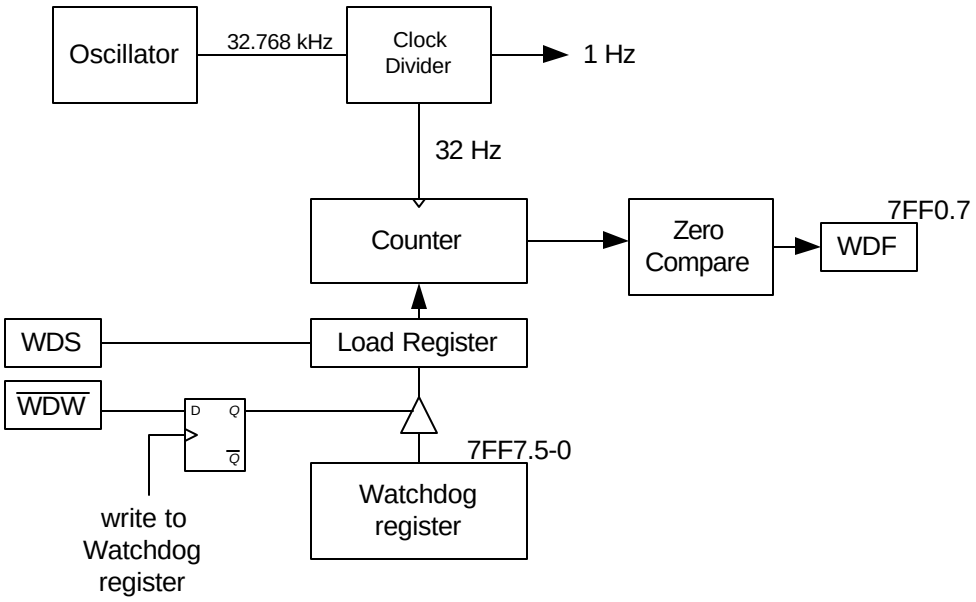


Figure 3. Watchdog Timer Block Diagram

Power Monitor

The FM3808 provides a power management scheme with either power-fail interrupt or processor-reset capability. It also controls the internal switch to backup power for the timekeeper and protects the memory from low-V_{DD} access. The power monitor is based on an internal band-gap reference circuit that compares the V_{DD} voltage to various thresholds.

The power monitor compares V_{DD} to three thresholds. The first is an interrupt threshold (V_{TP}). When V_{DD} drops below the V_{TP} level, the event will set the power fail flag PF (7FF0h bit D5). It also can drive the INT pin as described in the Interrupts section.

The second threshold is the low V_{DD} memory lockout voltage V_{LO}. This level prevents low voltage writes to the FRAM array, which may otherwise result in corrupted data. At this point, access to the memory array and clock registers will be blocked until V_{DD} rises above V_{LO}. The lockout voltage V_{LO} always trips below V_{TP}. When V_{DD} drops below V_{LO}, all inputs will be ignored. On power up, the chip enable input will be ignored while V_{DD} is below V_{LO}, but must be pulled high prior to V_{DD} reaching V_{LO}.

At the third threshold, the internal supply switches from V_{DD} to V_{BAK} for the timekeeper. This switchover will occur at the level when V_{DD} is less than V_{BAK}. When switchover occurs, the clock will begin to draw power from V_{BAK} rather than V_{DD}. This event may be above or below the V_{TP} or V_{LO} level depending on the battery voltage.

To conserve the life of the backup source, the power monitor circuit is only operated from V_{DD}. When V_{DD} has dropped too low for the monitor to work, it ceases operation. However, the power monitor will reenergize as V_{DD} rises on power up. On power-up, after the band-gap energizes, the reverse sequence will occur. As soon as the band gap is functional, it will re-assert both selections for switch over and power fail. As the V_{DD} rises further, the device will revert to the primary power source V_{DD}, allowing memory access and clock operation. As the V_{DD} rises above V_{TP}, the power-fail condition will be removed. Note that the PF flag will not be cleared until the Flags/Control register is read.

The following figure illustrates the various events tracked by the power monitor.

Figure 4. Power Monitor Events

In the diagram, V_{RST} is the voltage at which an active-low interrupt will have sufficient drive strength to pull the INT pin low.

Interrupts

The supervisor was designed to serve diverse applications. Its sophistication and programmability make the supervisor function highly configurable for the host system. The interrupt block is capable of providing system interrupt or reset conditions, and can even power up a system at a preprogrammed time. Although the INT pin is described as an interrupt, the pin may be used as a reset source as well.

The supervisor provides three potential interrupt sources. They include the watchdog timer, the power monitor, and the clock/calendar alarm. Each can be individually enabled and assigned to drive the INT pin. In addition, each has an associated flag bit that the host processor can use to determine the cause of the interrupt.

Some of the sources have additional control bits that determine functional behavior. In addition, the pin driver has three bits that specify its behavior when an interrupt occurs. A functional diagram of the interrupt logic is shown below.

The three interrupts each have a source and an enable. Both the source and the enable must be active (true high) in order to generate an interrupt output. Only one source is necessary to drive the pin. The user can identify the source by reading the Flags/Control register, which contains the flags associated with each source. All flags are cleared to 0 when the register is read. The cycle must be a complete read cycle (/WE high), otherwise the flags will not be cleared. The power monitor has two programmable settings that are explained above in the power monitor section.

Once an interrupt source is active, the pin driver determines the behavior of the output. It has two programmable settings as shown below. Pin driver control bits are located in the Interrupts register 7FF6h bits D3-D2.

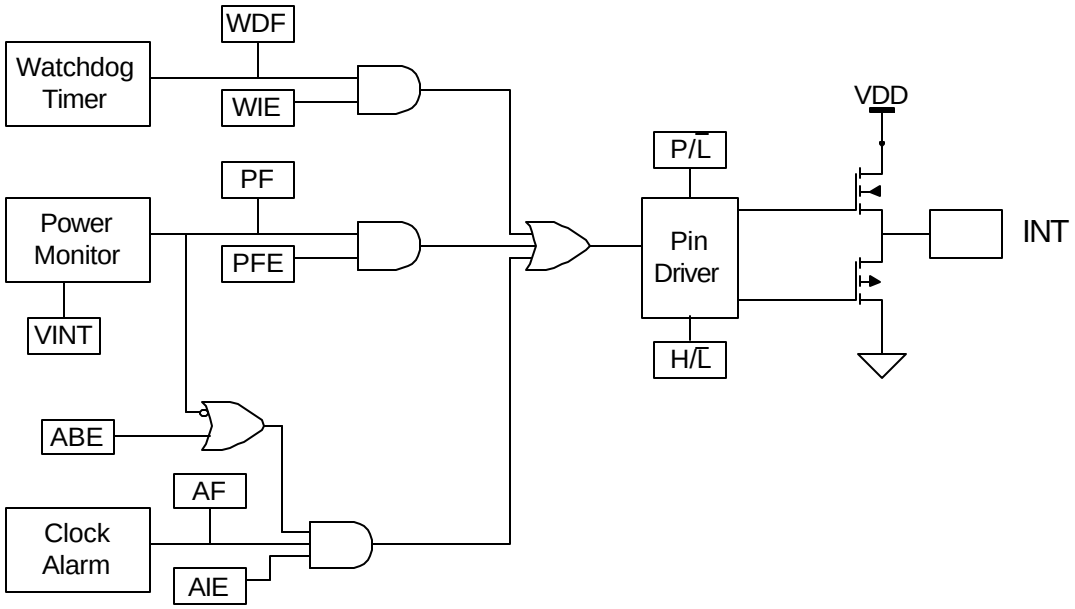


Figure 5. Interrupt Block Diagram

According to the programming selections, the pin can be driven in the backup mode for an alarm interrupt. In addition, the pin can be an active low (open-drain) or active high (push-pull) driver. If programmed for operation during backup mode, it can only be active low. Lastly, the pin can provide a one-shot function so that the active condition is a pulse, or a level condition. In One-Shot mode, the pulse width is internally fixed at approximately 200 ms. This mode is intended to reset a host microcontroller. In Level mode, the pin goes to its active polarity until the Flags/Control register is read by the user. This mode is intended to be used as an interrupt to a host microcontroller. The control bits are summarized as follows.

Watchdog Interrupt Enable - WIE. When set to 1, the watchdog timer drives the INT pin as well as an internal flag when a watchdog timeout occurs. When

WIE is set to 0, the watchdog timer affects only the internal flag.

Alarm Interrupt Enable – AIE. When set to 1, the alarm match drives the INT pin as well as an internal flag. When set to 0, the alarm match only affects the internal flag.

Power-fail Interrupt Enable - PFE. When set to 1, the power-fail monitor drives the pin as well as an internal flag. When set to 0, the power-fail monitor affects only the internal flag.

Alarm Battery-backup Enable - ABE. When set to 1, the clock alarm interrupt (as controlled by AIE) will function even in battery backup mode. When set to 0, the alarm will occur only when $V_{DD} > V_{LO}$. AIE should only be set when the INT pin is programmed for active low operation. In addition, it only functions with the clock alarm, not the watchdog. If enabled, the power monitor will drive the interrupt during all normal V_{DD} conditions regardless of the ABE bit. The application for ABE is intended for power control, where a system powers up at a predetermined time. Depending on the application, it may require dedicating the INT pin to this function.

High/Low – H/L. When set to a 1, the INT pin is active high and the driver mode is push-pull. The INT pin can drive high only when $V_{DD}>V_{LO}$. When set to a 0, the INT pin is active low and the driver mode is open-drain. Active low (open drain) is operational even in battery backup mode.

Pulse/Level – P/L. When set to a 1 and an interrupt occurs, the INT pin is driven for approximately 200 ms. When P/L is set to a 0, the INT pin is driven high or low (determined by H/L) until the Flags/Control register is read.

When an enabled interrupt source activates the INT pin, an external host can read the Flags/Control register to determine the cause. Remember that all flags will be cleared when the register is read. If the INT pin is programmed for Level mode, then the condition will clear and the INT pin will return to its inactive state. If the pin is programmed for Pulse mode, then reading the flag also will clear the flag and the pin. The pulse will not complete its specified duration if the Flags/Control register is read. If the INT pin is used as a host reset, then the Flags/Control register cannot be read during a reset. Care should be taken in reading the flags as a new source may occur after the pin goes active but before the register is read.

During a power-on reset with no battery, the interrupt register is automatically loaded with the value 24h. This causes power-fail interrupt to be enabled with an active-low pulse. See INT Timing at Power Up diagram on page 25.

Recommended Power-Up Sequence

The FM3808 registers must be programmed in order for the device to operate properly. The chip also must be power sequenced properly. The following is the recommended sequence:

1. Apply V_{BAK}
2. Apply V_{DD}
3. Remove V_{DD} (while V_{BAK} is still applied)
4. Apply V_{DD} (while V_{BAK} is still applied)
5. Program registers via 2-wire interface

The V_{DD} power supply may be removed once the RTC oscillator is enabled (running) and RTC/Alarm set. Interrupt enable bits may be set as desired.

CAUTION: If V_{DD} power is applied without a battery, there is no guarantee that I_{BAK} will be less than 1 µA. This will reduce the expected life of the battery since I_{BAK} could be much greater than 1 µA.

If the FM3808 is stored for days/weeks with battery attached and the clock/calendar values are not important, you should disable the RTC oscillator by setting the /OSCEN bit to a 1.

FRAM Memory Operation

The memory array is logically organized as 32,768 x 8 with the upper 16 bytes disabled and allocated to the RTC and supervisor control settings. It is accessed using an industry standard SRAM-type parallel interface. It is virtually identical to the 32Kx8 FM1808 in function. The memory array in the FM3808 is inherently nonvolatile via its unique ferroelectric process. All data written to the part is immediately nonvolatile with no delay. Functional operation of the FRAM memory is similar to SRAM type devices. The major operating difference between the FRAM array and an SRAM (besides nonvolatile storage) is that the FM3808 latches the address on the falling edge of /CE.

Users access 32,752 memory locations each with 8 data bits through a parallel interface. The complete 15-bit address specifies each of 32,768 bytes uniquely, with the upper 16 locations allocated to timekeeping functions. Internally, the memory array is organized into 32 blocks of 8Kb each. The 5 most-significant address lines decode one of 32 blocks. This block segmentation has no effect on operation, however the user may wish to group data into blocks by its endurance requirements as explained in a later section.

The access and cycle time are the same for read and write memory operations. Writes occur immediately at the end of the access with no delay. A precharge operation, where /CE goes inactive, is a part of every memory cycle. Thus unlike SRAM, the access and cycle times are not equal.

The FM3808 is designed to operate in a manner very similar to other bytewide memory products. For users familiar with BBSRAM, the performance is comparable but the bytewide interface operates in a slightly different manner as described below. For users familiar with EEPROM, the obvious differences result from the higher write-performance of FRAM technology including NoDelay writes and much higher write-endurance.

Read Operation

A read operation begins on the falling edge of /CE. At this time, the address bits are latched and a memory cycle is initiated. Once started, a full memory cycle will be completed internally even if the /CE is taken inactive. Data becomes available on the bus after the access time has been satisfied.

After the address has been latched, the address value may be changed upon satisfying the hold time parameter. Unlike an SRAM, changing address values will have no effect on the memory operation after the address is latched.

The FM3808 will drive the data bus when /OE is asserted low. If /OE is asserted after the memory access time has been satisfied, the data bus will be driven with valid data. If /OE is asserted prior to completion of the memory access, the data bus will not be driven until valid data is available. This feature minimizes supply current in the system by eliminating transients due to invalid data. When /OE is inactive, the data bus will remain tri-stated.

Write Operation

Writes occur in the FM3808 in the same time interval as reads. The FM3808 supports both /CE and /WE controlled write cycles. In all cases, the address is latched on the falling edge of /CE.

In a /CE controlled write, the /WE signal is asserted prior to beginning the memory cycle. That is, /WE is low when /CE falls. In this case, the part begins the memory cycle as a write. The FM3808 will not drive the data bus regardless of the state of /OE.

In a /WE controlled write, the memory cycle begins on the falling edge of /CE. The /WE signal falls after the falling edge of /CE. Therefore, the memory cycle begins as a read. The data bus will be driven according to the state of /OE until /WE falls. The timing of both /CE and /WE controlled write cycles is shown in the electrical specifications.

Write access to the array begins asynchronously after the memory cycle is initiated. The write access terminates on the rising edge of /WE or /CE, whichever is first. Data set-up time, as shown in the electrical specifications, indicates the interval during which data cannot change prior to the end of the write access.

Unlike other truly nonvolatile memory technologies, there is no write delay with FRAM. Since the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory operation occurs in a single bus cycle. Therefore, any operation including read or write can occur immediately following a write. Data polling, a technique used with EEPROMs to determine if a write is complete, is unnecessary.

Precharge Operation

The precharge operation is an internal condition where the state of the memory is prepared for a new access. All memory cycles consist of a memory

access and a precharge. The precharge is user initiated by taking the /CE signal high or inactive. It must remain high for at least the minimum precharge timing specification. The user dictates the beginning of this operation since a precharge will not begin until /CE rises. However, the device has a maximum /CE low time specification that must be satisfied.

Memory Architecture

FRAM memory internally operates with a read and restore mechanism. Therefore, each read and write cycle involves a change of state. The memory architecture is based on an array of rows and columns. Each access causes an endurance cycle for an entire 32-bit row (4 bytes). The memory array is divided into 32 blocks, each 1Kx8. The 5-upper address lines decode the block selection as shown in Figure 6. Data targeted for significantly different numbers of cycles should be located in separate blocks since memory rows do not extend across block boundaries.

Each block of 1Kx8 consists of 256 rows and 4 column address locations. The address lines A0-A7 decode row selection and A8-A9 lines decode column selection. This scheme facilitates a relatively uniform distribution of cycles across the rows of a block. By allowing the address LSBs to decode row selection, the user avoids applying multiple cycles to the same row when accessing sequential data. For example, 256 bytes can be accessed sequentially without accessing the same row twice. In this example, one cycle would be applied to each row. An entire block of 1Kx8 can be read or written with only four cycles applied to each row. Figure 7 illustrates the organization within a memory block.

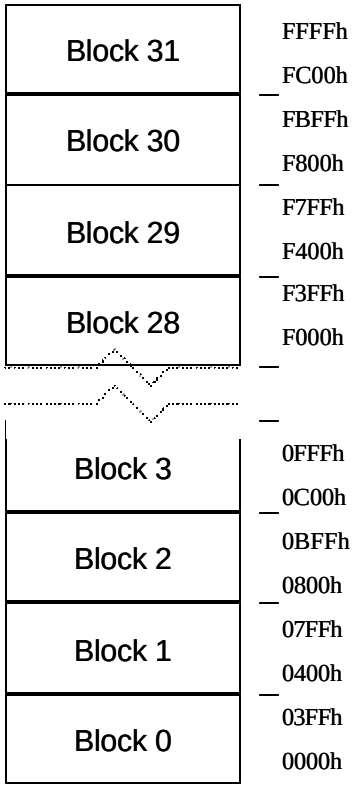


Figure 6. Address Blocks

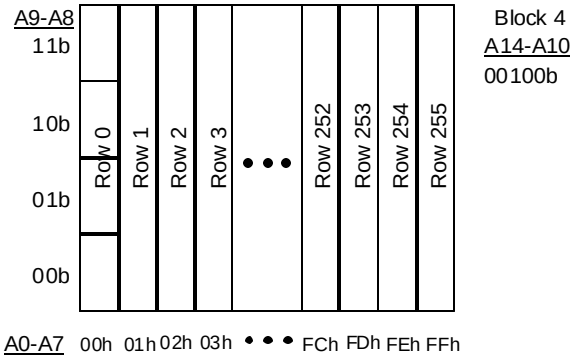


Figure 7. Row and Column Organization

FRAM Design Considerations

SRAM and FRAM alike begin each read/write cycle with a new address being driven prior to the chip enable transition low. The falling edge of chip enable latches the address and a memory access starts. For subsequent memory accesses, SRAMs allow /CE to remain low while the address bus changes. FRAM devices do not allow this signalling. Every FRAM access requires a falling edge of /CE, therefore users cannot ground this pin as you might with SRAM.

Users who are modifying existing designs to use FRAM should examine the memory controller for timing compatibility of address and control pins.

Each memory access must be qualified with a low transition of /CE. In many cases, this is the only change required. An example of the signal relationships is shown in Figure 8 below. Also shown is a common SRAM signal relationship that will not work for the FRAM devices.

The reason for /CE to strobe for each address is two-fold: it latches the new address and creates the necessary precharge period while /CE is high.

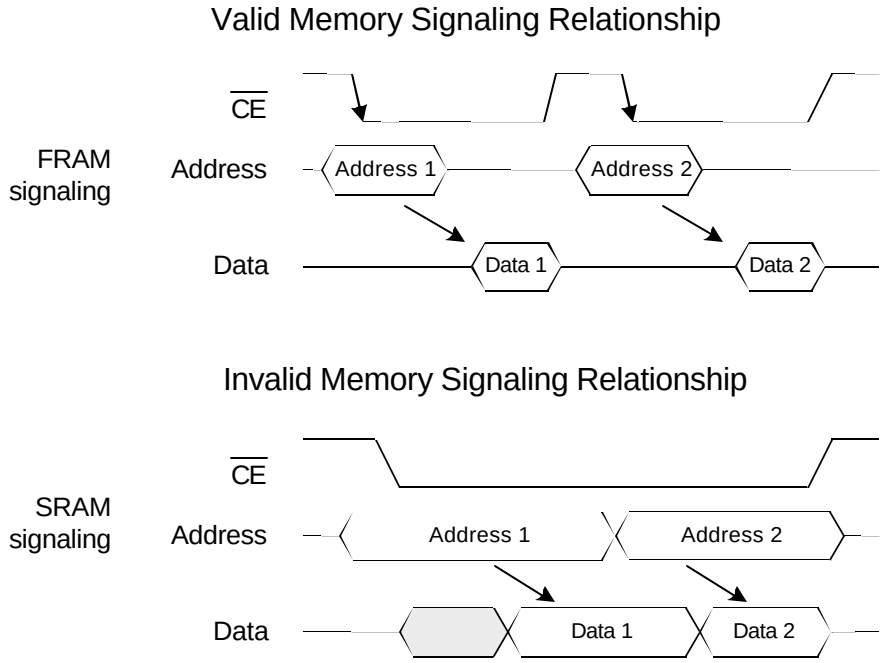


Figure 8. Memory Address and /CE Relationships

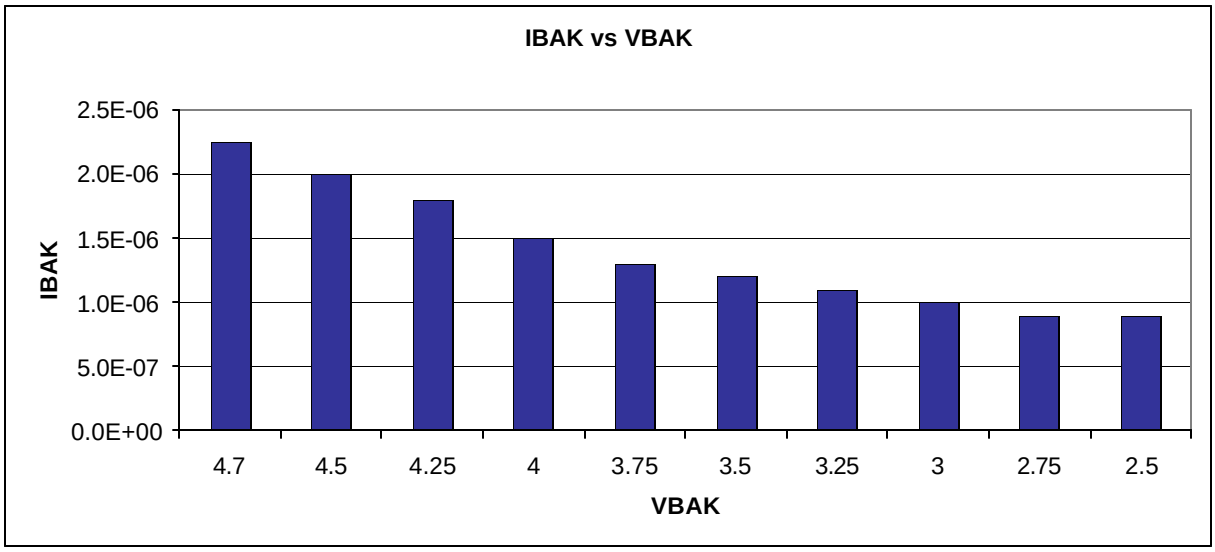


Figure 9. Backup Current vs. Voltage

Crystal Selection

The second passive component needed for the RTC function is the timekeeping crystal. A 32.768 kHz time-base is required, and the FM3808 is designed to accept a low cost crystal. The major parameters associated with the crystal are timekeeping accuracy and backup current. The FM3808 is designed to accept a crystal with a characteristic capacitance of 6 pF. Deviations from this specification will lead to different accuracy and IBAK from the specified values. Though accuracy is unlikely to improve, the IBAK may go up or down from the specified value as a function of the capacitive load.

The timekeeping accuracy is also a strong function of the operating temperature due to errors in crystal frequency. Temperature behavior of timekeeping crystals is well known and it follows a curve like the one shown below. The specific crystal manufacturer should be consulted for the behavior of their specific device. Note the error in frequency ppm. One ppm is roughly 2.6 seconds per month in timekeeping error.

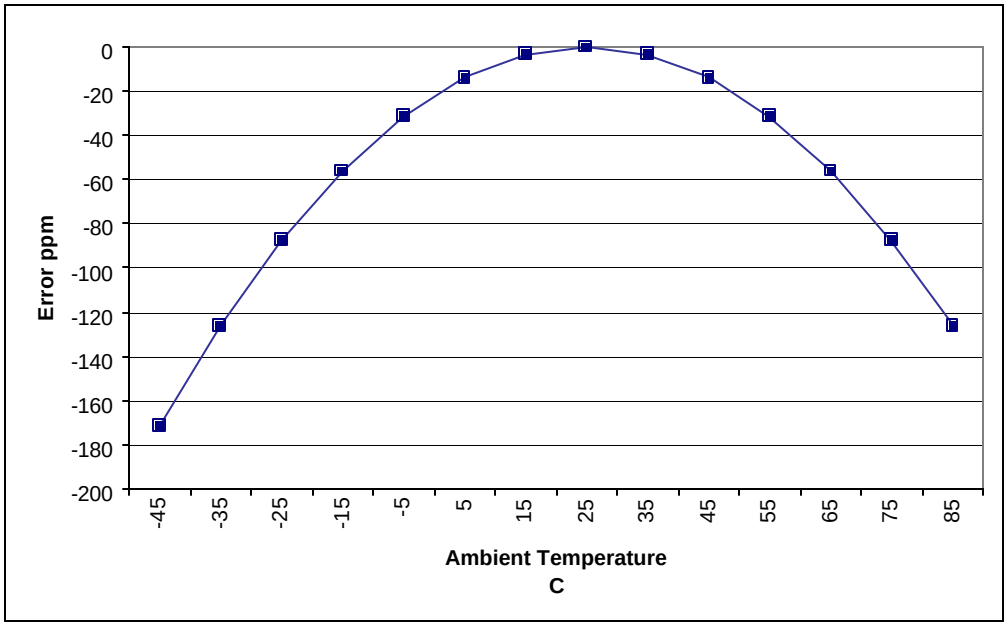


Figure 10. Typical Crystal Error vs. Temperature

Electrical Specifications

Absolute Maximum Ratings

Symbol	Description	Ratings
V_{DD}	Power Supply Voltage with respect to V_{SS}	-1.0V to +7.0V
V_{IN}	Voltage on any signal pin with respect to V_{SS}	-1.0V to +7.0V and V_{IN} < V_{DD}+1.0V
T_{STG}	Storage temperature	-55°C to + 125°C
T_{LEAD}	Lead temperature (Soldering, 10 seconds)	300° C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC Operating Conditions (T_A = -40° C to + 85° C, V_{DD} = 4.5V to 5.5V unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	
I_{DD}	V_{DD} Supply Current – Active		10	25	mA	1
I_{SB1}	Standby Current – TTL			500	µA	2
I_{SB2}	Standby Current – CMOS			150	µA	3
V_{BAK}	Clock Backup Voltage	2.5	3.0	V_{DD}	V	
I_{BAK}	Clock backup current			1	µA	4
V_{TP}	V_{DD} trip point voltage that activates INT pin	4.35		4.65	V	
V_{LO}	V_{DD} Lockout Voltage	4.2		4.49	V	8
V_{SW}	V_{DD} Voltage that causes switch to V_{BAK}		V_{BAK}		V	5
V_{RST}	V_{DD} Voltage for Active INT pin	1.2			V	6
I_{LI}	Input Leakage Current			10	µA	7
I_{LO}	Output Leakage Current			10	µA	7
V_{IH}	Input High Voltage	2.0		V_{DD} + 0.5	V	
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{OH}	Output High Voltage (I_{OH} = -2.0mA)	2.4			V	
V_{OL}	Output Low Voltage (I_{OL} = 4.2mA)			0.4	V	
V_{OLB}	Output Low Voltage (INT pin) Device in backup mode (V_{DD}<V_{BAK})			0.7	V	9

Notes

1. V_{DD} = 5.5V, /CE cycling at minimum cycle time. All inputs at CMOS levels, all outputs unloaded.
2. V_{DD} = 5.5V, /CE at V_{IH}, All other inputs and DQ pins at TTL levels.
3. V_{DD} = 5.5V, /CE at V_{IH}, All other inputs and DQ pins at CMOS levels.
4. V_{BAK} = 3.0V, V_{DD} < V_{BAK}; oscillator running. This parameter is characterized, not 100% tested.
5. V_{SW} occurs when V_{DD} drops below V_{BAK}. V_{SW} is also the point at which the timekeeper draws current from the V_{BAK} pin, rather than from V_{DD}. V_{SW} is not otherwise used for control signals or functions.
6. INT pin conditions are I_{OL} = 80 uA and V_{OL} = 0.4V.
7. V_{IN}, V_{OUT} between V_{DD} and V_{SS}.
8. Memory and register access is blocked when V_{DD} < V_{LO}.
9. V_{DD}=0, V_{BAK} = 3.0V, I_{OL} = 4.2 mA.

Read Cycle AC Parameters (T_A = -40° C to + 85° C, V_{DD} = 4.5V to 5.5V unless otherwise specified)

Symbol	Parameter	Min	Max	Units	Notes
t_{CE}	Chip Enable Access Time (to data valid)		70	ns	
t_{CA}	Chip Enable Active Time	70	2,000	ns	
t_{RC}	Read Cycle Time	130		ns	
t_{PC}	Precharge Time	60		ns	
t_{AS}	Address Setup Time	0		ns	
t_{AH}	Address Hold Time	10		ns	
t_{OE}	Output Enable Access Time		10	ns	
t_{HZ}	Chip Enable to Output High-Z		15	ns	1
t_{OHZ}	Output Enable to Output High-Z		15	ns	1

Write Cycle AC Parameters (T_A = -40° C to + 85° C, V_{DD} = 4.5V to 5.5V unless otherwise specified)

Symbol	Parameter	Min	Max	Units	Notes
t_{CA}	Chip Enable Active Time	70	2,000	ns	
t_{CW}	Chip Enable to Write High	70		ns	
t_{WC}	Write Cycle Time	130		ns	
t_{PC}	Precharge Time	60		ns	
t_{AS}	Address Setup Time	0		ns	
t_{AH}	Address Hold Time	10		ns	
t_{WP}	Write Enable Pulse Width	30		ns	
t_{DS}	Data Setup	30		ns	
t_{DH}	Data Hold	5		ns	
t_{WZ}	Write Enable Low to Output High Z		15	ns	1
t_{WX}	Write Enable High to Output Driven	10		ns	1
t_{HZ}	Chip Enable to Output High-Z		15	ns	1
t_{WS}	Write Setup	0		ns	2
t_{WH}	Write Hold	0		ns	2

Notes

1 This parameter is periodically sampled and not 100% tested.

2 The relationship between /CE and /WE determines if a /CE- or /WE-controlled write occurs. There is no timing specification associated with this relationship.

Power Cycle Timing (T_A = -40° C to + 85° C)

Symbol	Parameter	Min	Max	Units	Notes
t_{INT}	INT signal active after V_{TP}		100	ns	1,2
t_{PD}	Last Access Complete to V_{LO}	0		ns	1,3
t_{RI}	VLO to inputs recognized on power-up	1		µs	1,4
t_R	Rise time of V_{DD} from V_{BG} to V_{LO}	100		µs	1,5
t_F	Fall time of V_{DD} from V_{LO} to V_{BG}	100		µs	1,5

Notes

1 This parameter is periodically sampled and not 100% tested.

2 If power monitor is programmed to generate INT.

3 Access is blocked at V_{LO}. The last access should be complete prior to reaching V_{LO}. The early warning power fail interrupt may be useful in accomplishing this.

4 Failing to satisfy t_{RI} may result in the first access being ignored. Failure to raise /CE to a logic high prior to $V_{DD}>V_{LO}$ may result in improper operation.

5 Slew rate for proper transition between the locked-out condition and normal operation.

Supervisor AC Parameters (T_A = -40° C to + 85° C, V_{DD} = 4.5V to 5.5V unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
t_{IPU}	INT output pulse width	150	200	300	ms	1
t_{FCO}	Flags/Control register access to INT pin clear	-		100	ns	2

Notes

1 P/L = 1; pulse mode.

2 P/L= 0; level mode. From the end of the access where the Flags/Control register is read and the flag cleared.

Data Retention (V_{DD} = 4.5V to 5.5V unless otherwise specified)

Parameter	Min	Units	Notes
Data Retention	10	Years	

Capacitance (T_A = 25° C, f=1.0 MHz, V_{DD} = 5V)

Symbol	Parameter	Max	Units	Notes
C_{IO}	Input/output capacitance (DQ)	8	pF	1
C_I	Input capacitance	6	pF	1
C_{XTAL}	X1, X2 Crystal pin capacitance	12	pF	1, 2

Notes

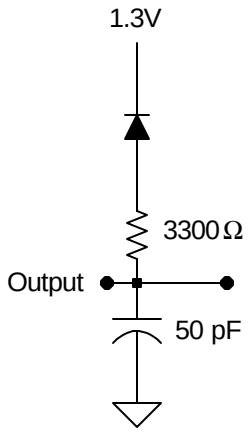
1 This parameter is periodically sampled and not 100% tested.

2 The crystal attached to the X1/X2 pins must be rated as 6pF max.

AC Test Conditions

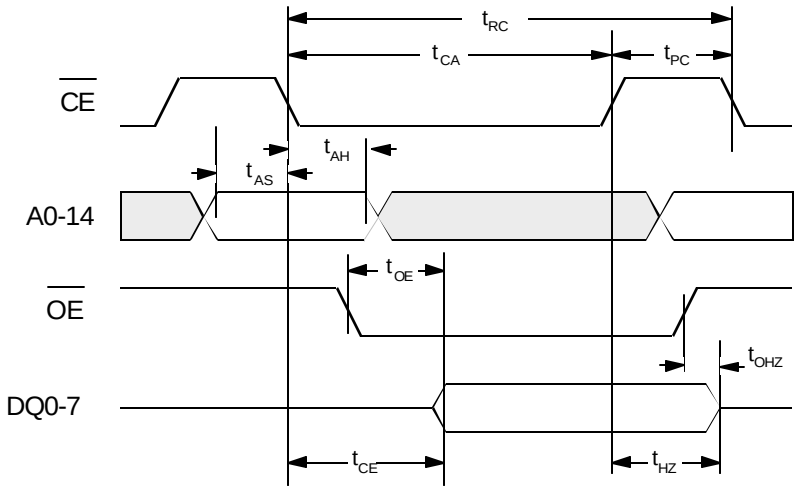
Input Pulse Levels	0 to 3V
Input rise and fall times	10 ns
Input and output timing levels	1.5V

Equivalent AC Load Circuit

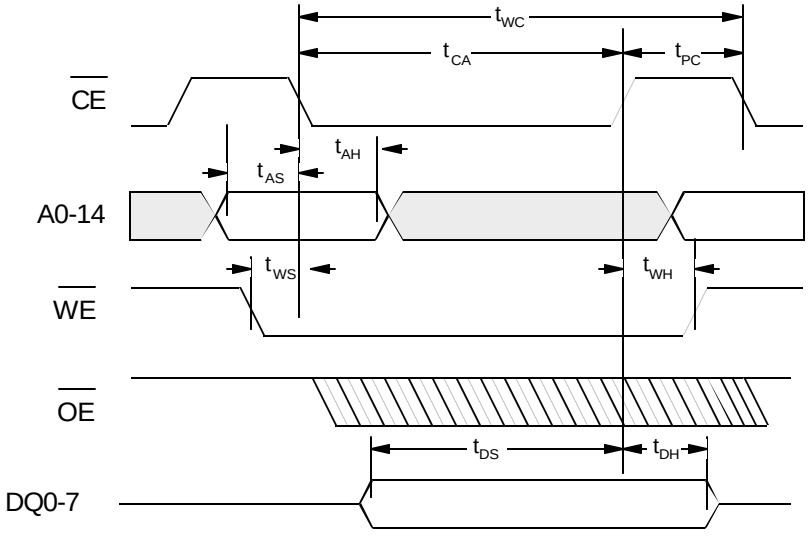


Timing Diagrams

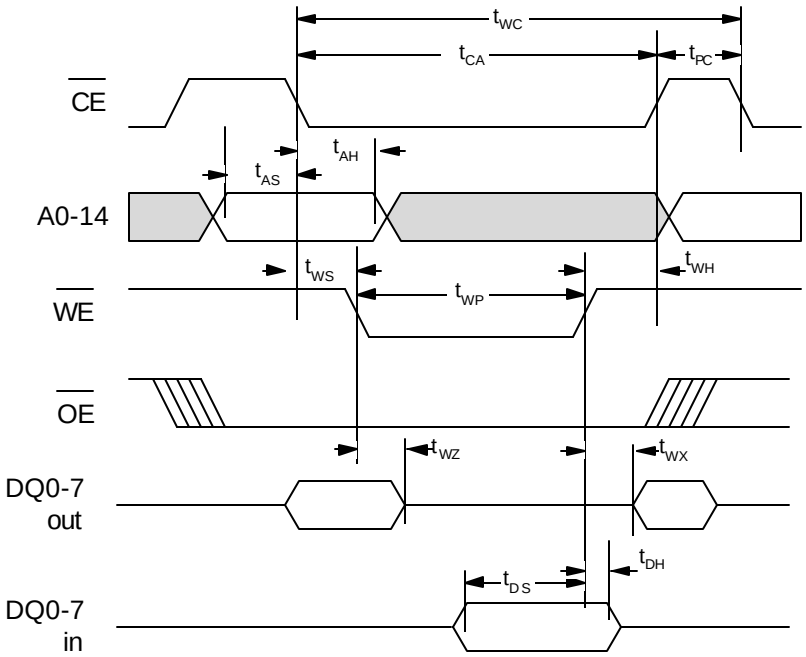
Read Cycle Timing



/CE-Controlled Write Cycle Timing

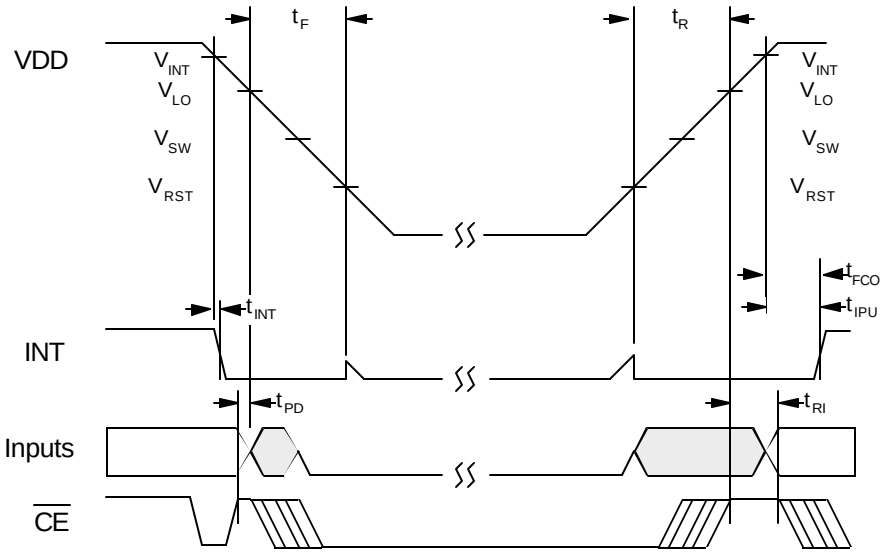


/WE-Controlled Write Cycle Timing

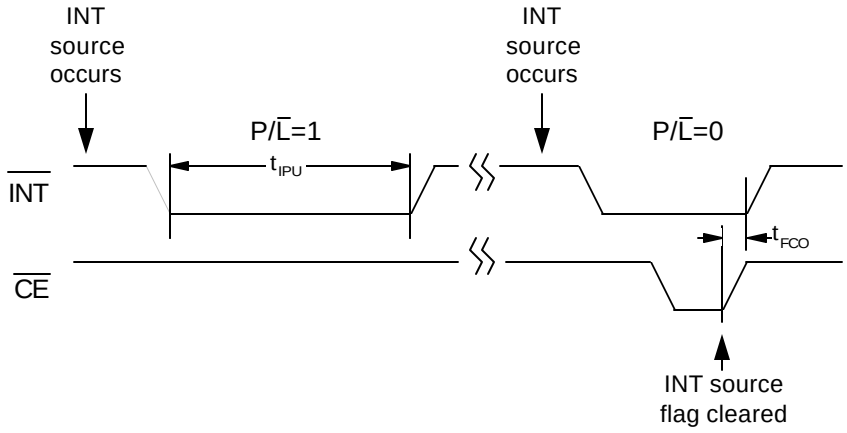


Power Cycle Timing

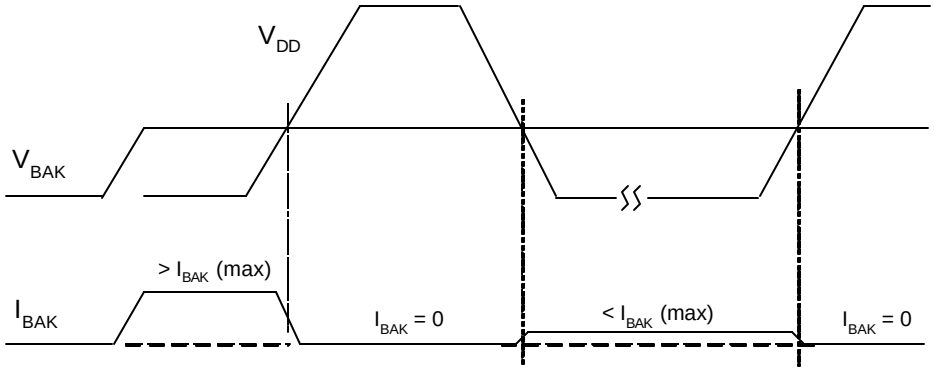
Picture assumes $V_{SW} < V_{INT}$



INT Pin Timing

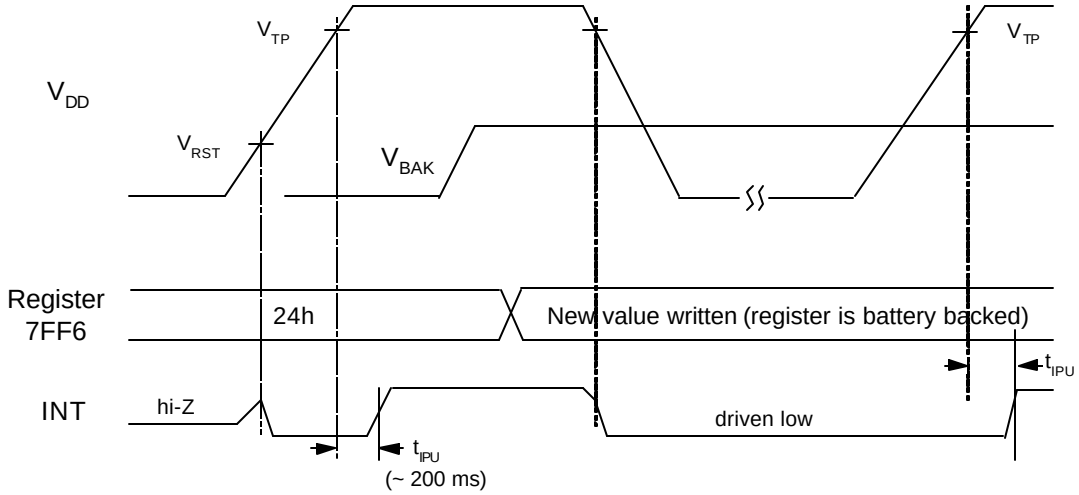


Recommended Power Up Sequence



The backup power supply V_{BAK} must be applied prior to V_{DD} power up. Once a battery is inserted and V_{DD} is cycled on and off, the current drain on the battery is guaranteed to be < I_{BAK}(max). When V_{DD} power is applied, there is no backup current drawn from the battery.

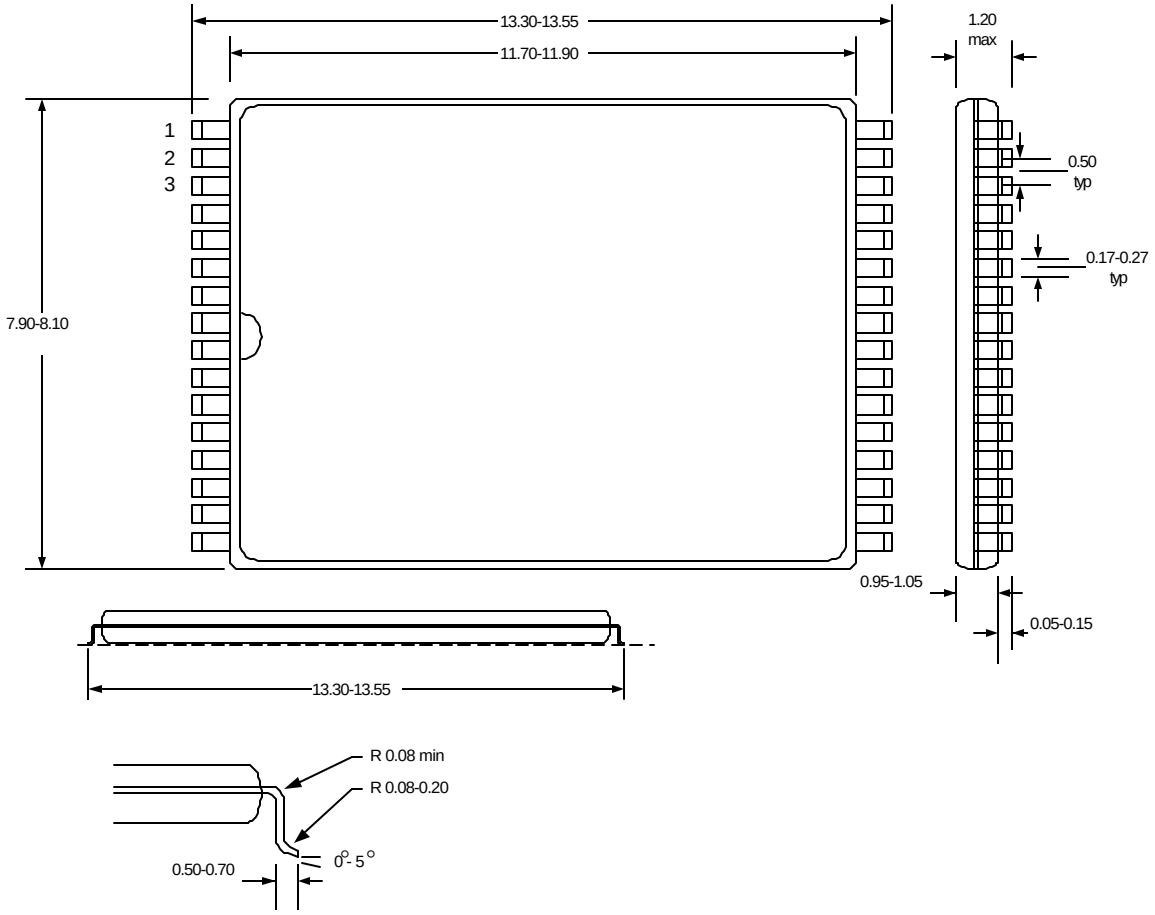
INT pin Timing at Power Up



It is <u>not recommended</u> that V_{DD} power be applied before V_{BAK}, however the timing diagram above illustrates what happens if this occurs. The drawing shows the behavior of the INT at power-up first without a backup supply V_{BAK} then with a backup supply. On power-up without a backup power supply, the device will initialize with the Power Fail bit enabled (PFE=1) and the INT pin will be active low (open drain) and pulse output mode (P/L=1). The Interrupt register 7FF6h defaults to the value 24h. Once V_{DD} is established, the register 7FF6h may be written to a different value to change the behavior of the INT pin. When a battery is used as a backup source, V_{DD} must be applied prior to inserting the battery to prevent battery drain. Once V_{DD} is applied and a battery is inserted, the current drain on the battery is guaranteed to be I_{BAK}(max).

Mechanical Drawing

32-pin Shrunk TSOP-I (8.0 x 13.4 mm)
All dimensions in millimeters



Revision History

Revision	Date	Summary of Changes
0.1	Dec 19, 2000	Initial Release
0.2	Sept 19, 2001	Changed I_{SB} spec, redefined crystal capacitance specs, data retention temperature condition. General cleanup.
1.0	July 31, 2002	Fixed shading in Table 1, registers 7FF1h–7FF4h. Increased storage temperature range. Changed input data hold time t_{DH} to 5ns.
1.1	May 2, 2003	Changed t_{CA} (max) spec. Reworded notes 2 and 3 in DC Operating table.
1.2	Feb 11, 2004	Removed all references to the use of a capacitor as a backup source. Added Recommended Power-Up Sequence section. Changed Mechanical Drawing title.