65,536-Word-by-18-Bit High-Speed CMOS Synchronous Static RAM
Preliminary

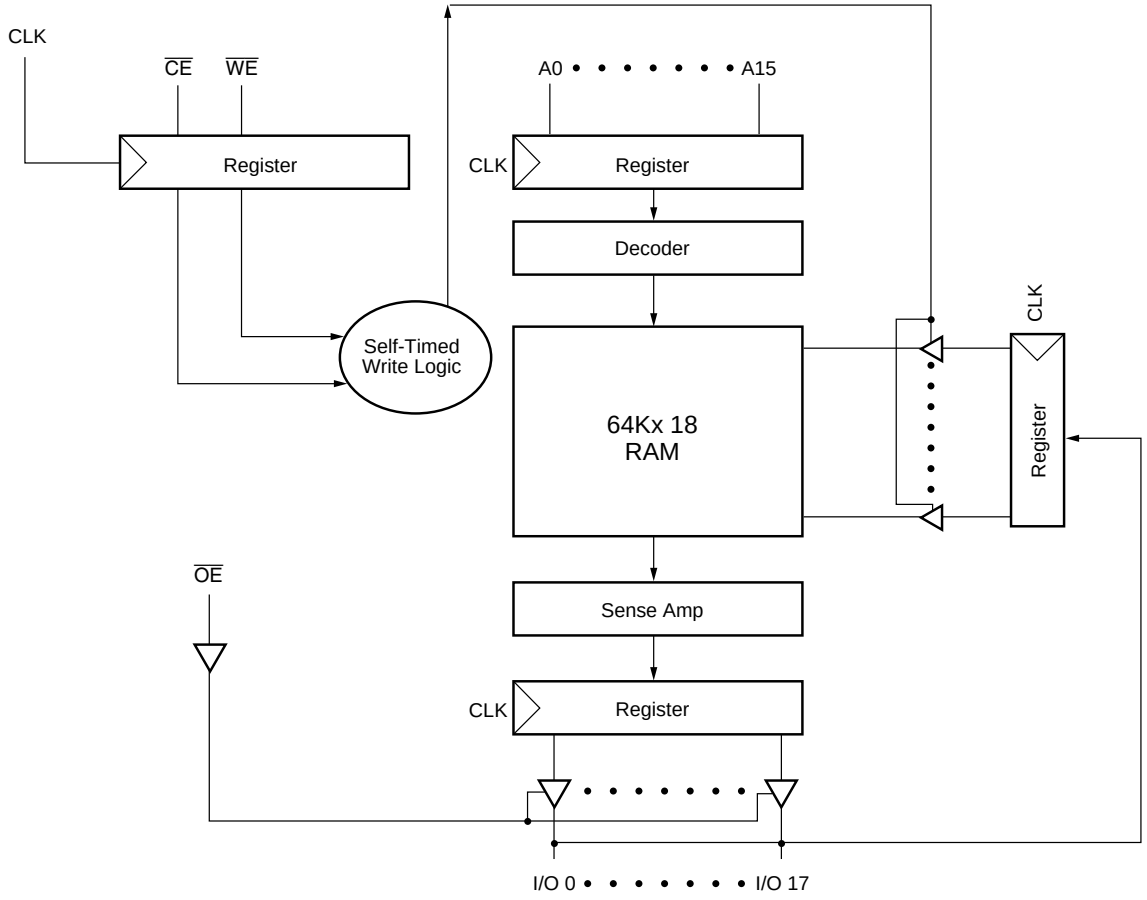
Description

The CXK77V1810GB/TM is a high-speed CMOS synchronous static RAM with common I/O pins, organized as 65,536-words-by-18-bits. This synchronous SRAM integrates input registers, high-speed SRAM and output registers onto a single monolithic IC. All input signals, except $\overline{OE}$, are latched at the positive edge of an external clock (CLK). The RAM data from the previous cycle is presented at the positive edge of the subsequent clock cycle. Write operation is initiated by the positive edge of CLK and is internally self-timed. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals. Asynchronous $\overline{OE}$ adds the flexibility of data bus control. 100MHz operation is obtained from a single 3.3V power supply.

Features

- High speed, low power consumption
- Single +3.3V power supply: 3.3V ± 5%
- Inputs and outputs are LVTTL/LVCMOS-compatible
- Byte Select capability
- Asynchronous $\overline{OE}$
- Common data input and output
- 9ns cycle time (110MHz)
- All inputs (except $\overline{OE}$) and outputs are registered on a single clock edge
- Self-timed write cycle
- Package line-up:
  - GB: 7 x 17 Plastic Ball Grid Array with 50mil pitch
  - TM: 400mil, 50-pin TSOP II with .8mm pitch

Functional Block Diagram

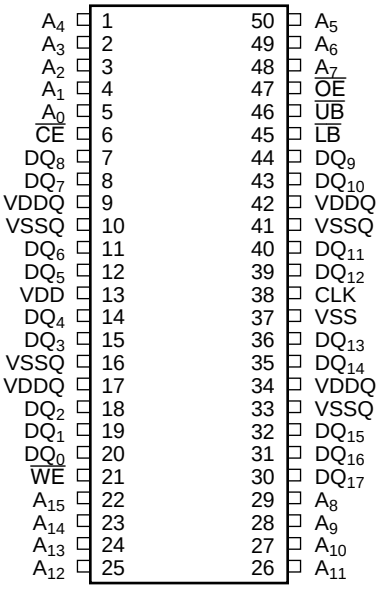


Pin Configuration (top view)

CXK77V1810GB

	1	2	3	4	5	6	7
A	VDDQ	A0	A2	NC	A4	A5	VDDQ
B	NC	NC	NC	NC	NC	NC	NC
C	NC	A1	A3	VDD	A6	A7	NC
D	DQ8	NC	VSS	NC	VSS	DQ9	NC
E	NC	DQ7	VSS	$\overline{CE}$	VSS	NC	DQ10
F	VDDQ	NC	VSS	$\overline{OE}$	VSS	DQ11	VDDQ
G	NC	DQ6	$\overline{LB}$	NC	NC	NC	DQ12
H	DQ5	NC	VSS	NC	VSS	DQ13	NC
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	NC	DQ4	VSS	CLK	VSS	NC	DQ14
L	DQ3	NC	NC	NC	$\overline{UB}$	DQ15	NC
M	VDDQ	DQ2	VSS	$\overline{WE}$	VSS	NC	VDDQ
N	DQ1	NC	VSS	A12	VSS	DQ16	NC
P	NC	DQ0	VSS	A11	VSS	NC	DQ17
R	NC	A15	NC	VDD	NC	A8	NC
T	NC	A14	A13	NC	A10	A9	NC
U	VDDQ	NC	NC	NC	NC	NC	VDDQ

CXK77V1810TM



Pin Description

Symbol	Description	Symbol	Description
A0 to A15	Address input	CLK	Clock input
DQ0 to DQ8	Lower Byte Data input/output	$\overline{LB}$	Lower Byte enable input
DQ9 to DQ17	Upper Byte Data input/output	$\overline{UB}$	Upper Byte enable input
V_{DD}	+3.3V power supply	$\overline{CE}$	Chip Enable input
V_{DDQ}	+3.3 output power supply	$\overline{WE}$	Write Enable input
V_{SSQ}	Output ground	$\overline{OE}$	Output Enable input
V_{SS}	Ground		

Separate V_{SSQ} are available only in CXK77V1810TM.
For proper operation, $V_{DD} \geq V_{DDQ}$ at all times, including power up.

Absolute Maximum Ratings

(Ta = +25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{DD}	–0.5 to +4.6	V
Input voltage	V_{IN}	–0.5 to V_{CC} + 0.5 (4.6V max.)	V
Output voltage	V_O	–0.5 to V_{CC} + 0.5 (4.6V max.)	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	–55 to +150	°C
Soldering temperature • time	T_{solder}	260 • 10	°C • sec

Truth Table

$\overline{CE}$ (t_n)	$\overline{WE}$ (t_n)	$\overline{UB}$ (t_n)	$\overline{LB}$ (t_n)	$\overline{OE}$	Mode	DQ_{0-17} (t_n)	DQ_{0-17} (t_{n+1})	V_{DD} Current
H	X	X	X	X	Deselect	Don't care	Hi Z	I_{SB}
L	H	X	X	H	Read, output Hi-Z	Don't care	Hi - Z	I_{CC}
L	H	H	H	X				
L	H	L	L	L	Read bits 0-17	Don't care	$D_{OUT}(t_n)$	I_{CC}
L	H	H	L	L	Read bits 0-8	Don't care	$D_{OUT}(t_n)$	I_{CC}
L	H	L	H	L	Read bits 9-17	Don't care	$D_{OUT}(t_n)$	I_{CC}
L	L	L	L	X	Write bits 0-17	$D_{IN}(t_n)$	Hi-Z	I_{CC}
L	L	H	L	X	Write bits 0-8	$D_{IN}(t_n)$	Hi-Z	I_{CC}
L	L	L	H	X	Write bits 9-17	$D_{IN}(t_n)$	Hi-Z	I_{CC}

DC Recommended Operating Conditions

(Ta = +25°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	3.15	3.3	3.45	V
Output supply voltage	V_{DDQ}*	3.15	3.3	3.45	V
Input high voltage	V_{IH}	2.0	—	V_{DD} + 0.3**	V
Input low voltage	V_{IL}	–0.3**	—	0.8	V

*V_{DDQ} must be ≤ V_{DD} at all times, including power up.

**V_{IL} = –1.5V min. and V_{IH} = V_{DD} +1.5V for pulse width less than 5ns.

Electrical Characteristics

DC and Operating Characteristics

(V_{CC} = 3.3V ± 10%, GND = 0V, Ta = 0 to = +70°C)

Item	Symbol	Test Conditions	Min.	Typ*	Max.	Unit
Input leakage current	I_{LI}	V_{IN} = GND to V_{DD}	–1	—	1	µA
Output leakage current	I_{LO}	V_O = GND to V_{CC} $\overline{OE}$ = V_{IH}	–1	—	1	µA
Operating power supply current	I_{DD}	Cycle = min. Duty = 100% I_{OUT} = 0mA	—	—	220	mA
Standby current	I_{SB}	$\overline{CE}$ ≥ V_{IH} Cycle = min. Duty = 100% I_{OUT} = 0mA	—	—	150	mA
Output high voltage	V_{OH}	I_{OH} = –2.0mA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 2.0mA	—	—	0.4	V

*V_{CC} = 3.3V, Ta = +25°C

I/O Capacitance

(Ta = +25°C, f = 1MHz)

Item	Symbol	Test Conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	5	pF
Output capacitance	C_{OUT}	V_{OUT} = 0V	—	7	pF

Note: These parameters are sampled and are not 100% tested.

AC Electrical Characteristics

Item	Symbol	-9		-10		-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Clock period	t_{CP}	9	—	10	—	12.5	—	ns
Clock pulse high	t_{CH}	3.5	—	4	—	4	—	ns
Clock pulse low	t_{CL}	3.5	—	4	—	4	—	ns
Setup time	t_S	2.0	—	2.5	—	2.5	—	ns
Hold time	t_H	0.5	—	0.5	—	0.5	—	ns
Clock to output	t_{CQ}	2	5.5	2	6	2	7	ns
Clock to output high impedance	t_{HZ}*2	—	5.5	—	6	—	6	ns
Clock to output low impedance	t_{HZ}*2	2	—	2	—	2	—	ns
$\overline{OE}$ to output	t_{OE}	1	5	1	5	1	6	ns
$\overline{OE}$ to output high impedance	t_{OHZ}*2	—	4.5	—	5	—	5	ns
$\overline{OE}$ to output low impedance	t_{OLZ}*2	1	—	1	—	1	—	ns

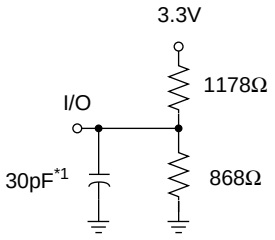
1. All parameters are specified over the range 0 to +70°C.
2. These parameters are sampled and are not 100% tested.

AC Characteristics

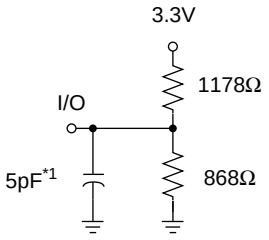
AC Test Conditions (V_{DD} = 3.3V ± 5%, Ta = 0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH} = 2.4V
Input pulse low level	V_{IL} = 0.4V
Input rise time	t_r = 2ns
Input fall time	t_f = 2ns
Input reference level	1.4V
Output reference level	1.4V
Output load conditions	Figure 1

Output Load (1)



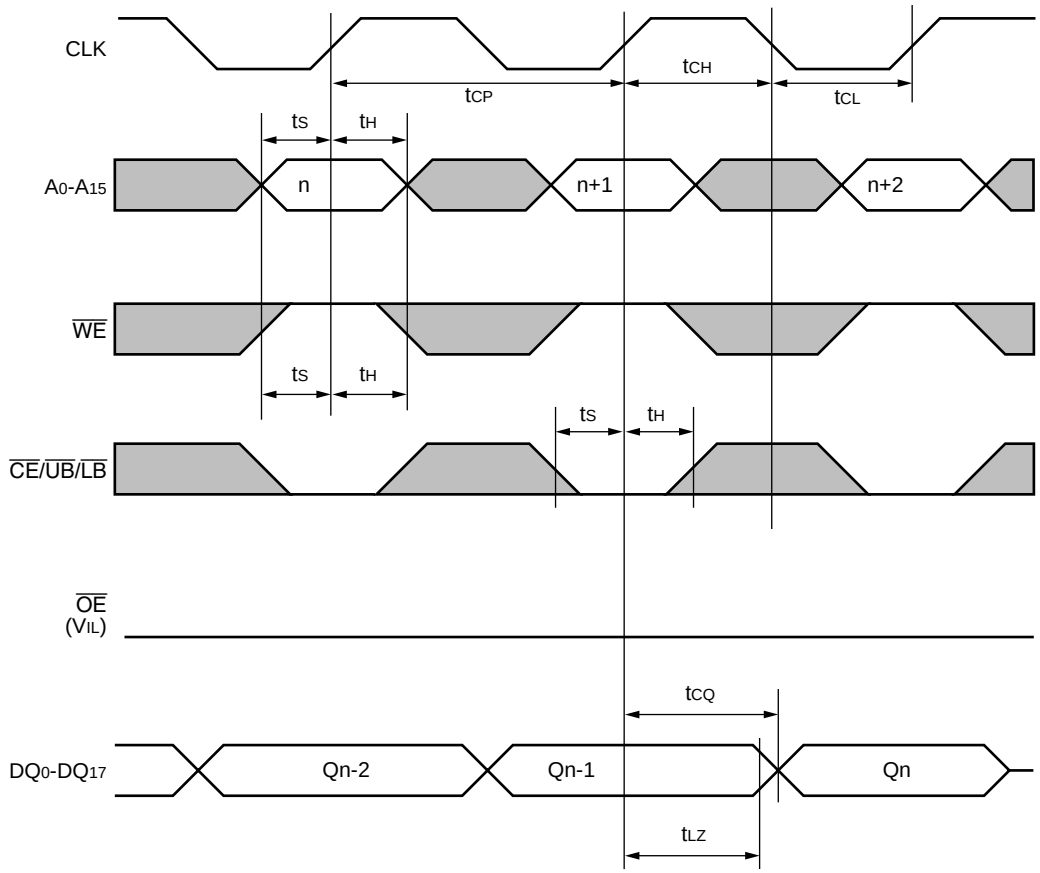
Output Load*2 (2)



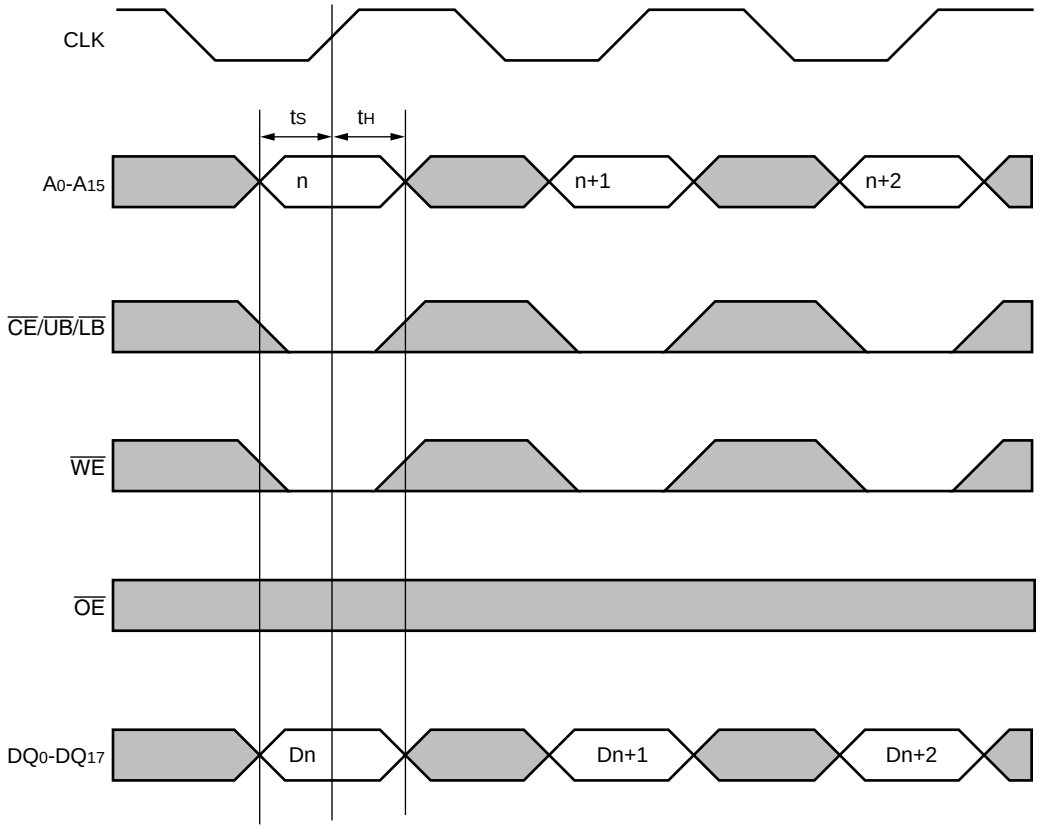
*1. Including scope and jig capacitance.
*2. For t_{LZ}, t_{HZ}

Figure 1

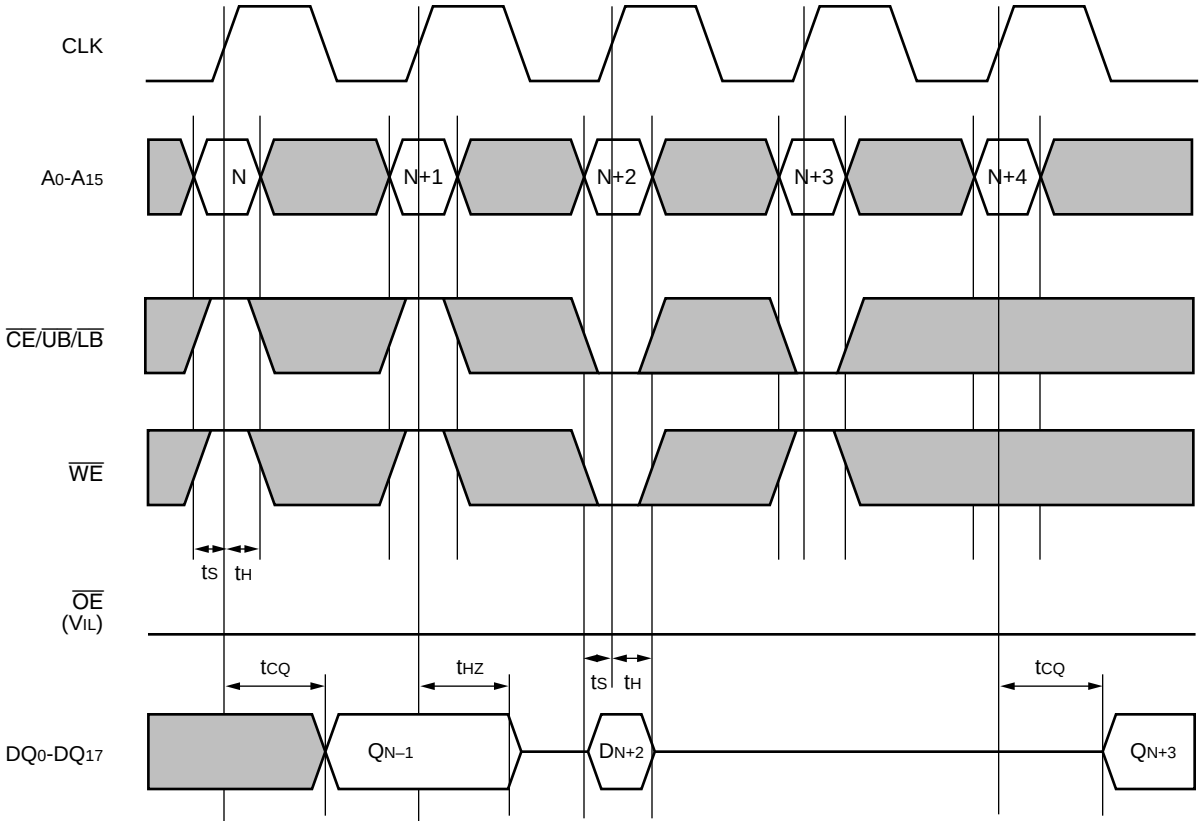
Timing Waveform of Read Cycle



Timing Waveform of Write Cycle



Timing Waveform of Read-Write-Read Cycle I ($\overline{CE}$/$\overline{UB}$/$\overline{LB}$ Control)



Timing Waveform of Read-Write-Read Cycle II ($\overline{OE}$ Control)