# 1.5A,Step-Up/Down Inverting Switching Regulators

DESCRIPTION

The AV34063 is a monolithic control circuit containing the primary functions required for DC-to-DC converters. This device consists of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit,driver and high current output switch. This device was specifically designed to be incorporated in Step-Down and Step-Up and Voltage-inverting applications with a minimum number of external components.

FEATURES

- Operation from 3.0 to 40V input
- Low standby current
- Current limiting
- Output switch current of 1.5A
- Output voltage adjustable
- Frequency of operation from 100Hz to 100KHz
- Precision 2% reference

DIP-8

SOP-8

BLOCK DIAGRAM

(Bottom View)

(Top View)
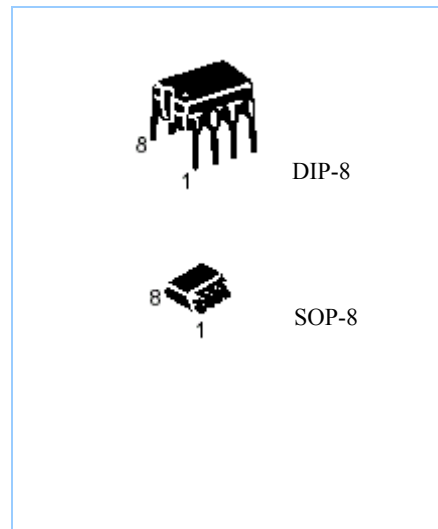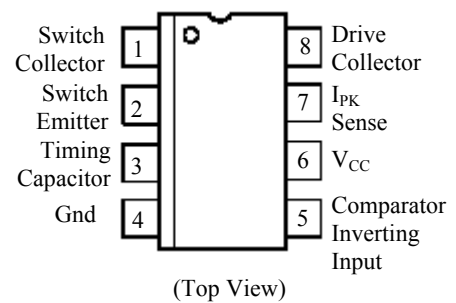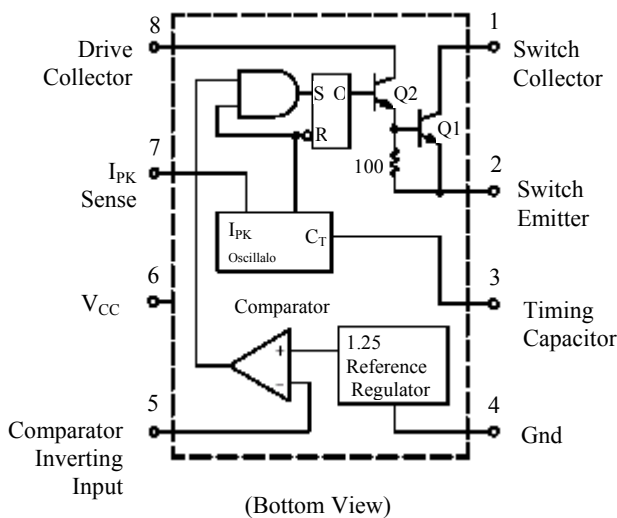
ORDERING INFORMATION

Part Number	Operating Temperature Range	Package Type
AV34063	0℃~+70℃	DIP-8
AV34063S	0℃~+70℃	SOP-8

 Website: _http://www.avictek.com_

MAXIMUM RATING

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	
Comparator Input Voltage Range	V_{IR}	-0.3 to +40	
Switch Collector Voltage	$V_{C(switch)}$	40	
Switch Emitter Voltage (V_{PIN1}=40V)	$V_{E(switch)}$	40	V
Switch Collector toEmitter Voltage	$V_{CE(switch)}$	40	
Driver Collector Voltage	$V_{C(driver)}$	40	
Driver Collector Current (Note1)	$I_{C(driver)}$	100	mA
Switch Current	I_{SW}	1.5	A

Power Dissipation and Thermal Charcteristics
     Plastic Package T_A =25℃
 Thermal Resistance
     SOIC Package T_A =25℃
 Thermal Resistance
	P_D
	 $R_{\theta JA}$
	 P_D
	 $R_{\theta JA}$
		1.25
		 100
		 0.625
		 100
			W
			 ℃/ W
			 W
			 ℃/ W

Operating Juncton Temperature	T_J	+150	℃
Operating Ambient Temperature Range	T_A	0 to +70	℃
Storage Temperature Range	T_{stg}	-60~150	℃

Notes: 1. Maximum package power dissipation limits must be observed.
      2.ESD data available upon request.

ELECTRICAL CHARACTETRISTICS

(V_{CC}=5.0V, T_A=T_{low} to T_{high} [Note1], unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency(V_{pin5}=0V, C_T =1.0nF, T_A =25℃)	F_{OSC}	24	33	42	KHz
Charge Current (V_{CC}=5.0V to 40V, T_A =25℃)	I_{chg}	24	35	42	μA
Discharge Current (V_{CC}=5.0V to 40V, T_A =25℃)	I_{dischg}	140	220	260	μA
Discharge to Charge Current Ratio (Pin 7 to V_{CC}, T_A =25℃)	I_{dischg}/ I_{chg}	5.2	6.5	7.5	-
Current Limit Sense Voltage ($I_{chg=}$ $I_{dischg,}$ T_A =25℃)	$V_{ipk(sence)}$	250	300	350	mV
OUTPUT SWITCH (NOTE 2)					
Saturation Voltage, Darlington Connection (Note 3) (I_{SW} =1.0A, Pins 1,8 connected)	$V_{CE(sat)}$	-	1.0	1.3	V
Saturation Voltage, Darlington Connection (I_{SW} =1.0A, R_{pin8} =82Ω to $V_{CC,}$ Forced β≈20)	$V_{CE(sat)}$	-	0.45	0.7	V
DC Current Gain (I_{SW} =1.0A, V_{CE}=5.0V, T_A =25℃)	H_{EF}	50	75	-	-
Collector Off-State Current (V_{CE}=40V)	$I_{C(Off)}$	-	0.01	100	μA
COMPARATOR					
Threshold Voltage (T_A =25℃) (T_A = T_{low} to T_{high})	V_{th}	1.238 1.225	1.25 -	1.262 1.275	V
Threshold Voltage Line Regulation (V_{CC}=3.0V to 40V)	Reg_{line}	-	1.4	5.0	mV
Input Bias Current (V_{in}=0V)	I_{IB}	-	-20	-400	nA
TOTAL DEVICE					
Supply Current ((V_{CC}=5.0V to 40V, C_T =1.0nF, (Pin 7 to $V_{CC,}$ (Pin 5> $V_{th,}$ (Pin 2=Gnd, remaining pins open)	I_{CC}	-	-	4.0	mA

Notes: 1. T_{low} =0℃ T_{high} =+70℃

2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

3. If the output switch is driven into hard saturation (non-Darlington) at low switch current (≤300mA) and high driver currents (≥30mA),it may take up to 2.0 μs for it to come out of saturation. This condition will shorten the off time at frequencies ≥30KHz, and is magnified at high temperature. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non-Darlington configuration is used, the following output drive condition is recommended :

Forced β of output switch : (I_C output/(I_C driver - 7.0mA)≥10)

* The 100Ω resister in the emitter of the driver device requires about 7.0mA before the output switch conducts.
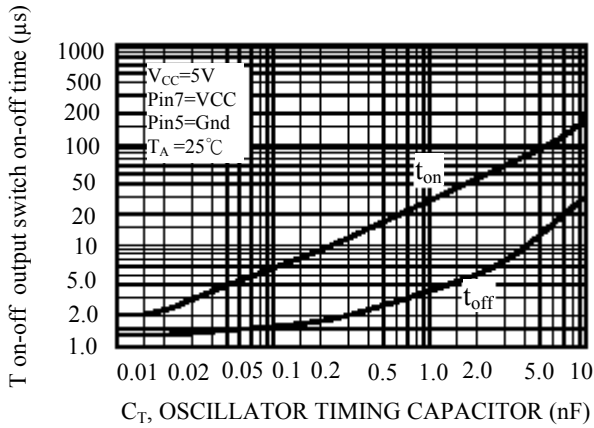
Typical Characteristics

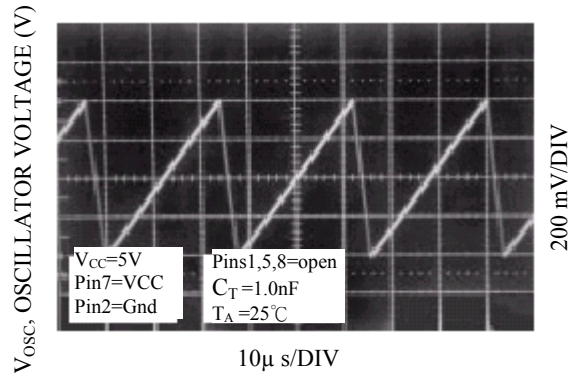Figure 1. Output Switch On–Off Time versus Oscillator Timing Capacitor
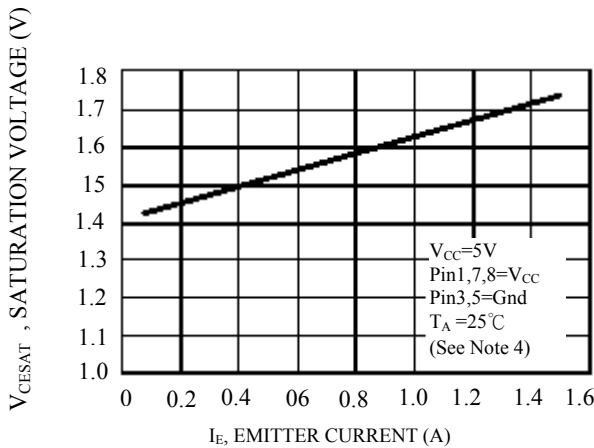

Figure2. Timing Capacitor Waveform

Figure 3. Emitter Follower Configuration Output Saturation Voltage versus Emitter Current
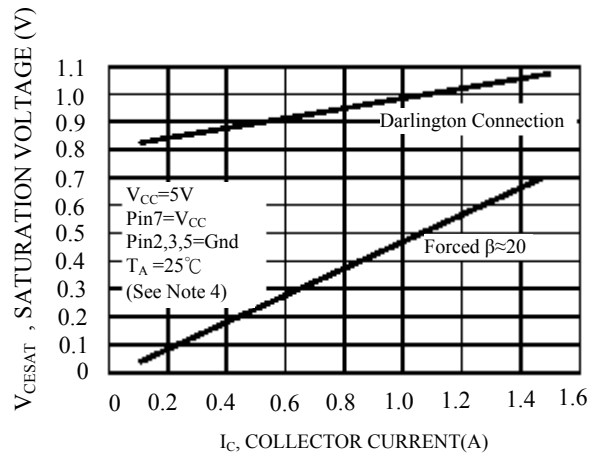

Figure 4. Common Emitter Configuration Output Switch Saturation Voltage versus Collector Current
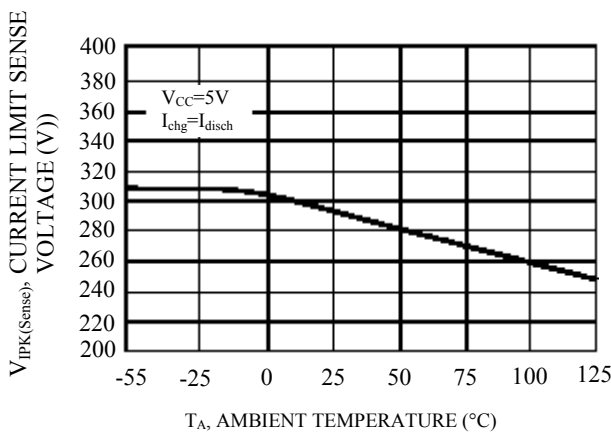

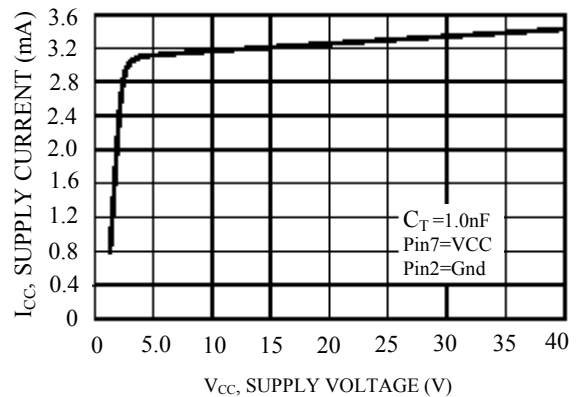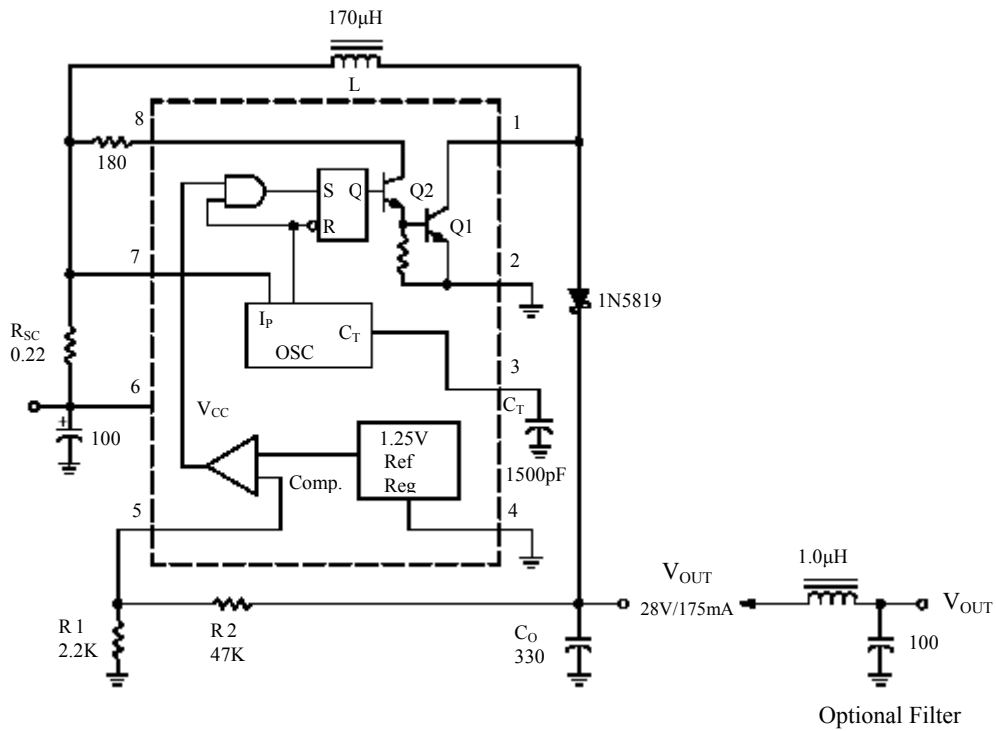Figure 5. Current Limit Sense Voltage versus Temperature

Figure 6. Standby Supply Current versus Supply Voltage

Test	Conditions	Results
Line Regulation	Vin = 8.0 V to 16 V, I_O = 175 mA	30 mV = ±0.05%
Load Regulation	Vin = 12 V, I_O = 75 mA to 175 mA	10 mV = ±0.017%
Output Ripple	Vin = 12 V, I_O = 175 mA	400 mVpp
Effciency	Vin = 12 V, I_O = 175 mA	87.7%
Output Ripple With Optional Filter	Vin = 12 V, I_O = 175 mA	40 mVpp

Figure 7. Step–Up Converter

8a. External NPN Switch

8b. External NPN Saturated Switch
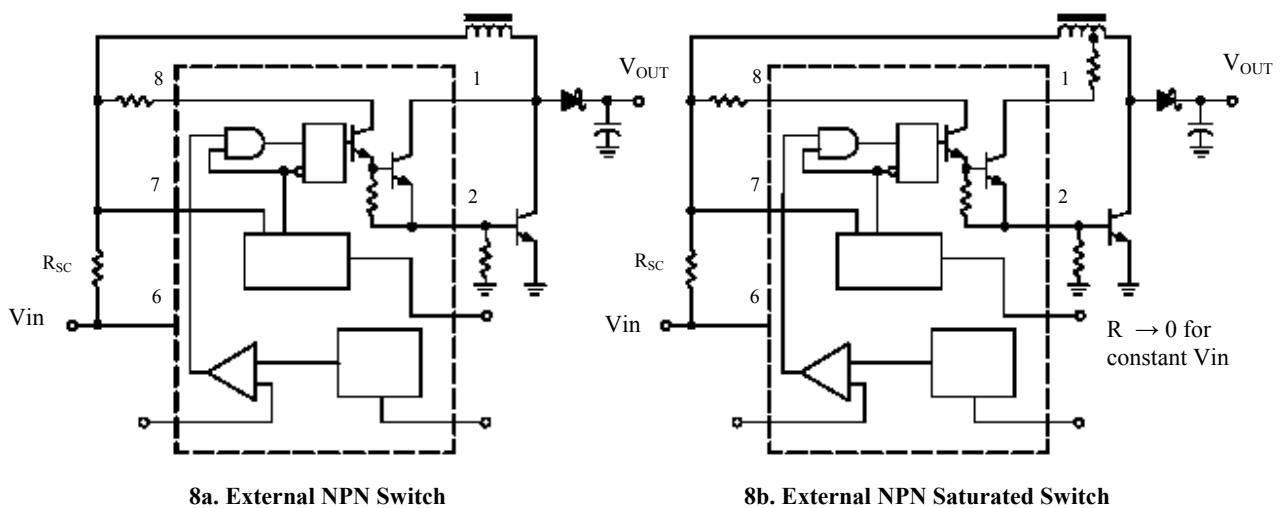
Figure 8. External Current Boost Connections for I_C Peak Greater than 1.5 A

Figure9. Step–Down Converter
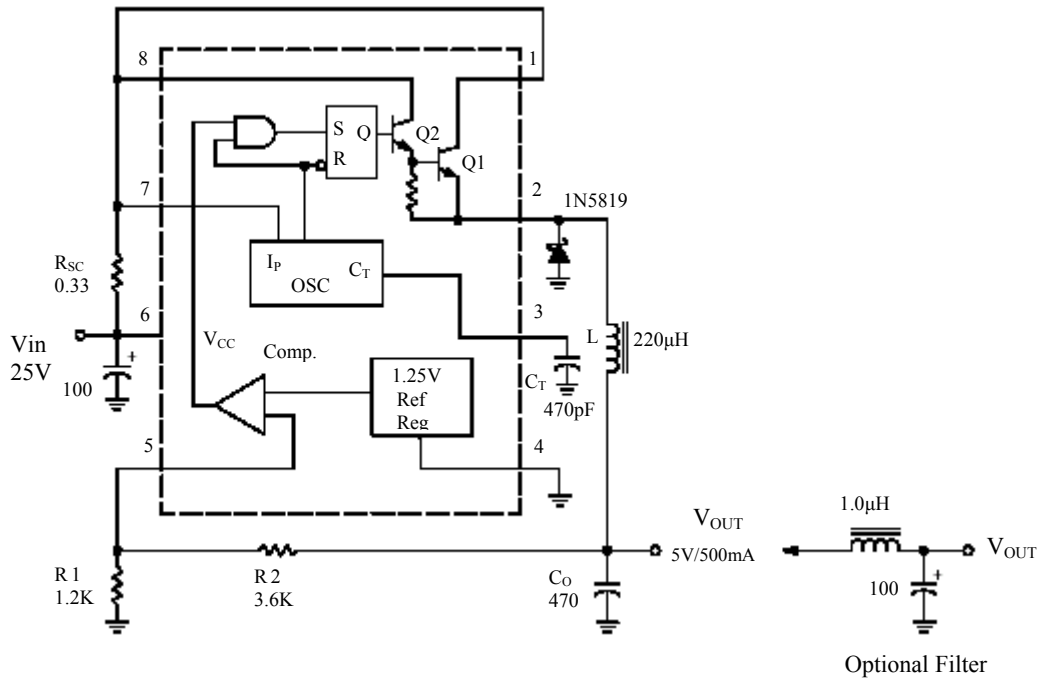
Test	Conditions	Results
Line Regulation	Vin = 15 V to 25 V, I_O = 500 mA	12 mV = ±0.12%
Load Regulation	Vin = 25 V, I_O = 50 mA to 500 mA	3.0 mV = ±0.03%
Output Ripple	Vin = 25 V, I_O = 500 mA	120 mVpp
Short Circuit Current	V in = 25 V, RL = 0.1Ω	1.1A
Effciency	Vin = 25 V, I_O = 500 mA	83.7%
Output Ripple With Optional Filter	Vin = 25 V, I_O = 500 mA	40 mVpp
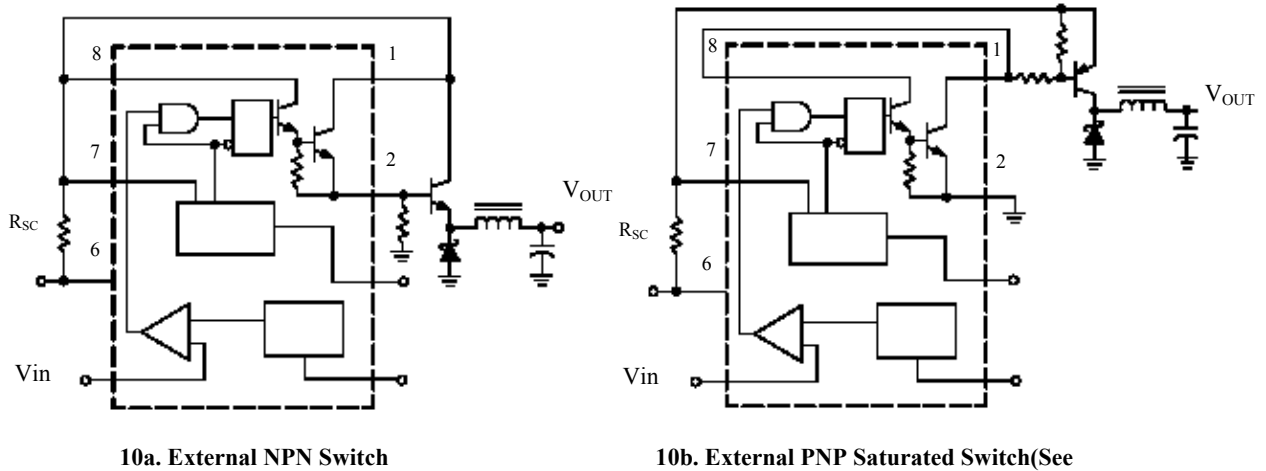
10a. External NPN Switch **N t 5)**

10b. External PNP Saturated Switch(See

Figure10. External Current Boost Connections for I_C Peak Greater than 1.5 A

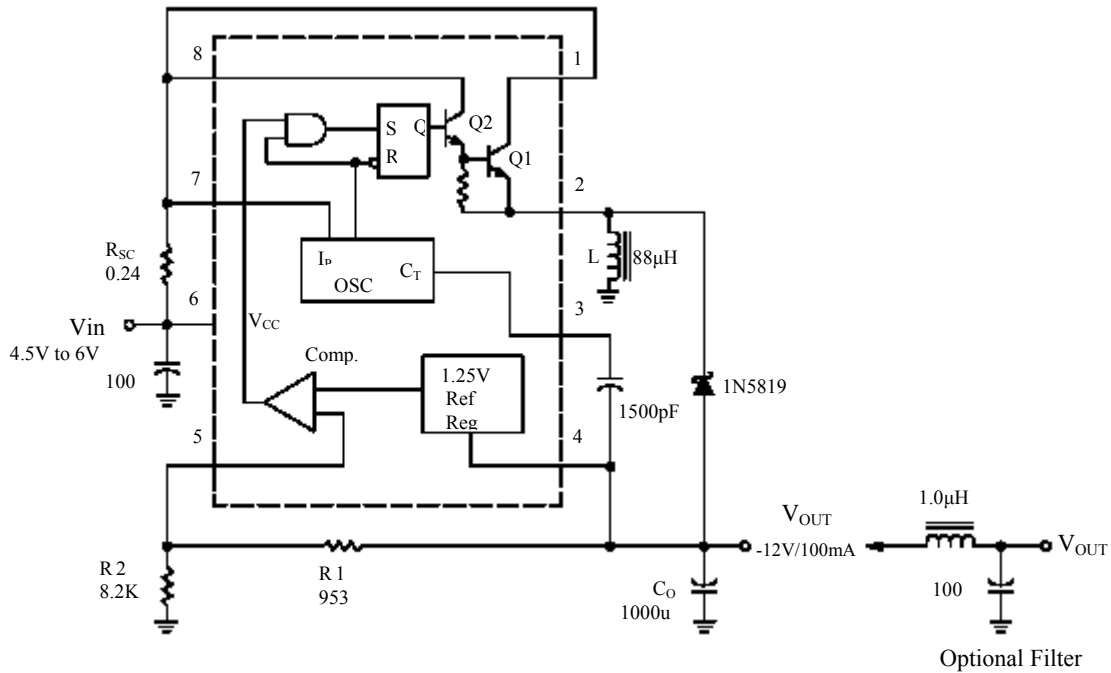| Test	Conditions	Results
Line Regulation	Vin = 4.5 V to 6 V, I_O = 100 mA	3.0 mV = ±0.012%
Load Regulation	Vin = 5.0 V, I_O = 10 mA to 100 mA	0.022 mV = ±0.09%
Output Ripple	Vin = 5.0 V, I_O = 100 mA	500 mVpp
Short Circuit Current	V in = 5.0 V, RL = 0.1Ω	910mA
Effciency	Vin = 5.0 V, I_O = 100 mA	62.6%
Output Ripple With Optional Filter	Vin = 5.0 V, I_O = 100 mA	70 mVpp

Figure11. Step–Down Converter

12a. External NPN Switch
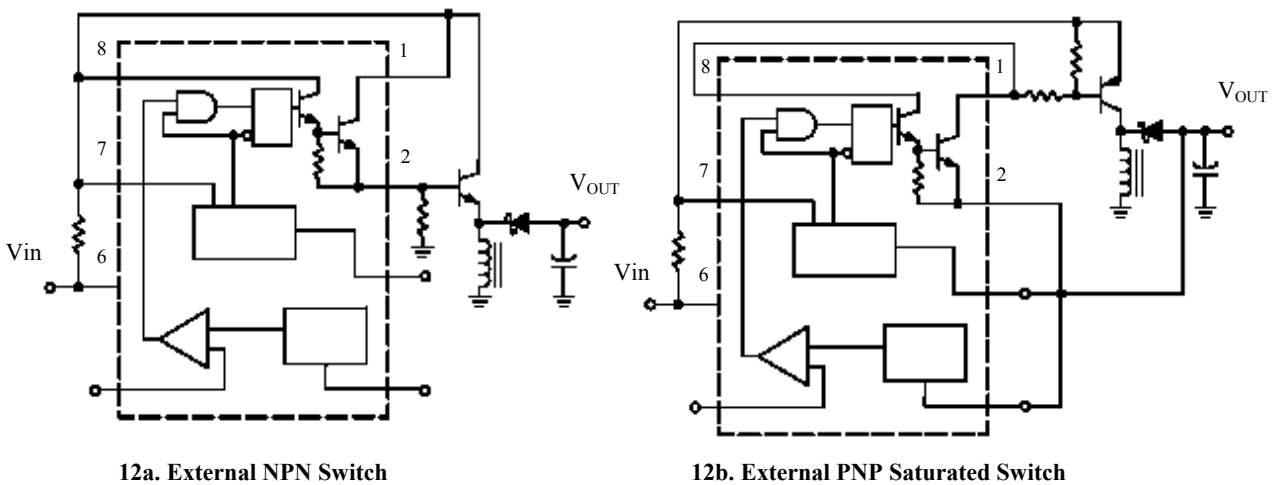

12b. External PNP Saturated Switch

Figure12. External Current Boost Connections for I_C Peak Greater than 1.5 A

Note 5 : If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents (≤300mA) and high driver currents (≥30mA), it may take up to 2.0μs to come out of sturation. This condition will shorten the off time at frequencies ≥30KHz, and is magnified at high temperatures. This condition does not occur with a darlington configuration, since the output switch cannot saturate. If a non-darlington is used, the following output drive condition is recommended.

Calculation	Step–Up	Step–Down	Voltage–Inverting
t_{on}/t_{off}	$\dfrac{V_{out}+V_F-V_{in(min)}}{V_{in(min)}-V_{sat}}$	$\dfrac{V_{out}+V_F}{V_{in(min)}-V_{sat}-V_{out}}$	$\dfrac{|V_{out}|+V_F}{V_{in}-V_{sat}}$
$(t_{on}+t_{off})$	$\dfrac{1}{f}$	$\dfrac{1}{f}$	$\dfrac{1}{f}$
t_{off}	$\dfrac{t_{on}+t_{off}}{\dfrac{t_{on}}{t_{off}}+1}$	$\dfrac{t_{on}+t_{off}}{\dfrac{t_{on}}{t_{off}}+1}$	$\dfrac{t_{on}+t_{off}}{\dfrac{t_{on}}{t_{off}}+1}$
t_{on}	$(t_{on}+t_{off})-t_{off}$	$(t_{on}+t_{off})-t_{off}$	$(t_{on}+t_{off})-t_{off}$
C_T	$4.0\times10^{-5}\,t_{on}$	$4.0\times10^{-5}\,t_{on}$	$4.0\times10^{-5}\,t_{on}$
$I_{pk(switch)}$	$2I_{out(max)}\left(\dfrac{t_{on}}{t_{off}}+1\right)$	$2I_{out(max)}$	$2I_{out(max)}\left(\dfrac{t_{on}}{t_{off}}+1\right)$
R_{sc}	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$
$L_{(min)}$	$\left(\dfrac{V_{in(min)}-V_{sat}}{I_{pk(switch)}}\right)t_{on(max)}$	$\left(\dfrac{V_{in(min)}-V_{sat}-V_{out}}{I_{pk(switch)}}\right)t_{on(max)}$	$\left(\dfrac{V_{in(min)}-V_{sat}}{I_{pk(switch)}}\right)t_{on(max)}$
C_O	$9\dfrac{I_{out}t_{on}}{V_{ripple(pp)}}$	$\dfrac{I_{pk(switch)}(t_{on}+t_{off})}{8V_{ripple(pp)}}$	$9\dfrac{I_{out}t_{on}}{V_{ripple(pp)}}$

Figure13. Design Formula Table

V_{sat}=Saturation voltage of the output switch.
V_F =Forward voltage drop of the output rectifier.
The following power supply characteristics must be chosen:
V_{in} -Nominal input voltage.
V_{out} -Desired output voltage, $V_{out} = 1.25(1+R2/R1)$.
I_{out} - Desired output current.
F_{min} -Minimum desired output switching frequency at the selected valued of Vin an Io.
$V_{ripple(p-p)}$ - Desired peak-to-peak output ripple voltage.In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout.The ripple voltage should be kept to a low value since it will directiy affect the line and load regulation.