Features

- **Fast Read Access Time - 90 ns**
- **Five-Volt-Only Reprogramming**
- **Page Program Operation**
    - **Single Cycle Reprogram (Erase and Program)**
    - **Internal Address and Data Latches for 64 Bytes**
- **Internal Program Control and Timer**
- **Hardware and Software Data Protection**
- **Fast Program Cycle Times**
    - **Page (64 Byte) Program Time - 10 ms**
    - **Chip Erase Time - 10 ms**
- **DATA Polling for End of Program Detection**
- **Low Power Dissipation**
    - **80 mA Active Current**
    - **300 µA CMOS Standby Current**
- **High Reliability CMOS Technology**
    - **1000 Erase/Program Cycles**
    - **10-Year Data Retention**
- **Single 5 V ± 10% Supply**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Full Military, Commercial, and Industrial Temperature Ranges**

256K (32K x 8) 5-Volt Only CMOS Flash PEROM
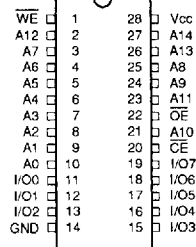
Description

The AT29C256 is a five-volt-only in-system Flash Programmable and Erasable Read Only Memory (PEROM). Its 256K of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 90 ns with power dissipation of just 440 mW. When the device is deselected, the CMOS standby current is less than 300 µA. *continued on next page*

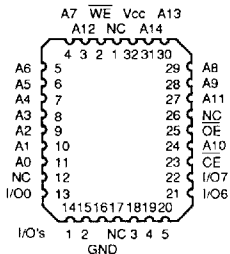# Pin Configurations

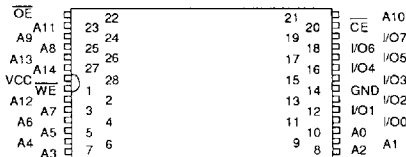| Pin Name	Function
A0 - A14	Addresses
CE	Chip Enable
OE	Output Enable
WE	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

DIP Top View

PLCC and LCC Top View

TSOP Top View
Type 1

Note. PLCC package pins 1 and 17 are DON'T CONNECT.

Description (Continued)

To allow for simple in-system reprogrammability, the AT29C256 does not require high input voltages for programming. Five-volt-only commands determine the operation of the device. Reading data out of the device is similar to reading from a static RAM. Reprogramming the AT29C256 is performed on a page basis; 64 bytes of data are loaded into the device and then simultaneously programmed. The contents of the entire device may be erased by using a six-byte software code (although erasure before programming is not needed).

During a reprogram cycle, the address locations and 64 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a program cycle, the device will automatically erase the page and then program the latched data using an internal control timer. The end of a program cycle can be detected by $\overline{DATA}$ polling of I/O7. Once the end of a program cycle has been detected a new access for a read, program or chip erase can begin.

Block Diagram
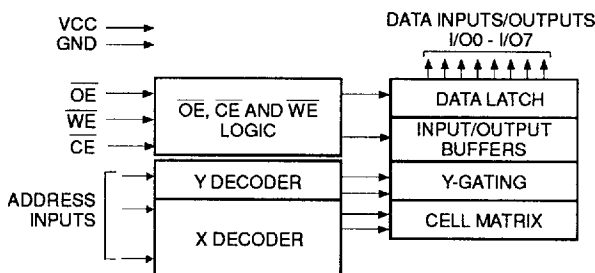
Device Operation

READ: The AT29C256 is accessed like a static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

BYTE LOAD: A byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Byte loads are used to enter the 64 bytes of a page to be programmed or the software codes for data protection and chip erasure.

PROGRAM: The device is reprogrammed on a page basis. If a byte of data within a page is to be changed, data for the entire page must be loaded into the device. Any byte that is not loaded during the programming of its page will be erased to read FFh. Once the bytes of a page are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data byte has been loaded into the device, successive bytes are entered in the same manner. Each new byte to be programmed must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150 µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding byte. If a high to low transition is not detected within 150 µs of the last low to high transition, the load period will end and the internal programming period will start. A6 to A14 specify the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A5 specify the byte address within the page. The bytes may be loaded in any order; sequential loading is not required.

SOFTWARE DATA PROTECTION: A software controlled data protection feature is available on the AT29C256. Once the software protection is enabled a software algorithm must be issued to the device before a program may be performed. The software protection feature may be enabled or disabled by the user; when shipped from Atmel, the software data protection feature is disabled. To enable the software data protection, a series of three program commands to specific addresses with specific data must be performed. After the software data protection is enabled the same three program commands must begin each program cycle in order for the programs to occur. All software program commands must obey the page program timing specifications. Once set, the software data protection feature remains active unless its disable command is issued. Power transitions will not reset the software data protection feature, however the software feature will guard against inadvertent program cycles during power transitions.

Once set, software data protection will remain active unless the disable command sequence is issued.

After setting SDP, any attempt to write to the device without the three-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of twc, a read operation will effectively be a polling operation.

After the software data protection's three-byte command code is given, a byte load is performed by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high.

1074177 0006897 904

Device Operation (Continued)

The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. The 64 bytes of data must be loaded into each sector by the same procedure as outlined in the program section under device operation.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT29C256 in the following ways: (a) V_{CC} sense— if V_{CC} is below 3.8 V (typical), the program function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 5 ms (typical) before programming. (c) Program inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter— pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer and may be accessed by a hardware operation. For details, see Operating Modes or Product Identification.

DATA POLLING: The AT29C256 features $\overline{DATA}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{DATA}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ polling the AT29C256 provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

OPTIONAL CHIP ERASE MODES: The entire device may be erased by either using a six-byte software code or high voltage. For details, please contact Atmel.

Absolute Maximum Ratings*

Temperature Under Bias ....-55°C to +125°C

Storage Temperature......................-65°C to +150°C

All Input Voltages
(including N.C. Pins)
with Respect to Ground .... -0.6 V to +6.25 V

All Output Voltages
with Respect to Ground .. ..-0.6 V to V_{CC} +0.6 V

Voltage on $\overline{OE}$
with Respect to Ground . .. . -0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Capacitance   (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	$V_{IN} = 0$ V
C_{OUT}	8	12	pF	$V_{OUT} = 0$ V

Note: 1. This parameter is characterized and is not 100% tested.

D.C. and A.C. Operating Range

		AT29C256-90	AT29C256-12	AT29C256-15	AT29C256-20	AT29C256-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V± 10%	5 V± 10%	5 V± 10%	5 V ± 10%	5 V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	Ai	D_{OUT}
Program[2]	V_{IL}	V_{IH}	V_{IL}	Ai	D_{IN}
5V Chip Erase	V_{IL}	V_{IH}	V_{IL}	Ai	
Standby/Write Inhibit	V_{IH}	X[1]	X	X	High Z
Write Inhibit	X	X	V_{IH}		
Write Inhibit	X	V_{IL}	X		
Output Disable	X	V_{IH}	X		High Z
High Voltage Chip Erase	V_{IL}	V_H [3]	V_{IL}	X	High Z
Product Identification					
Hardware	V_{IL}	V_{IL}	V_{IH}	A1-A14 = V_{IL}, A9 = V_H, A0 = V_{IL}	Manufacturer Code[4]
				A1-A14 = V_{IL}, A9 = V_H, A0 = V_{IH}	Device Code[4]
Software[5]				A0 = V_{IL}	Manufacturer Code[4]
				A0 = V_{IH}	Device Code[4]

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. V_H = 12.0 V ± 0.5 V.
4. Manufacturer Code: 1F, Device Code: DC
5. See details under Software Product Identification Entry/Exit.

D.C. Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0 V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC}-0.3 V to V_{CC}		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0 V to V_{CC}		3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		80	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5 V	4.2		V

A.C. Read Characteristics

| Symbol	Parameter	AT29C256-90		AT29C256-12		AT29C256-15		AT29C256-20		AT29C256-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		90		120		150		200		250	ns
t_{CE} [1]	$\overline{CE}$ to Output Delay		90		120		150		200		250	ns
t_{OE} [2]	$\overline{OE}$ to Output Delay	0	40	0	50	0	70	0	80	0	100	ns
t_{DF} [3,4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	0	30	0	40	0	50	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, CE or Address, whichever occurred first	0		0		0		0		0		ns

A.C. Read Waveforms
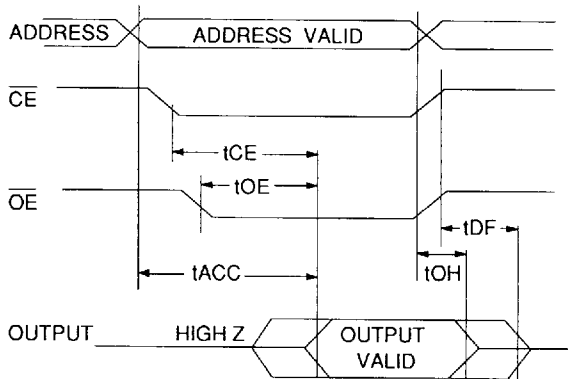
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.

3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first ($C_L = 5pF$).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level
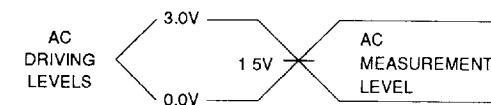
t_R, $t_F < 5$ ns

Output Test Load

5
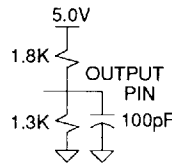
A.C. Byte Load Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	90		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{WPH}	Write Pulse Width High	100		ns

A.C. Byte Load Waveforms- $\overline{WE}$ Controlled
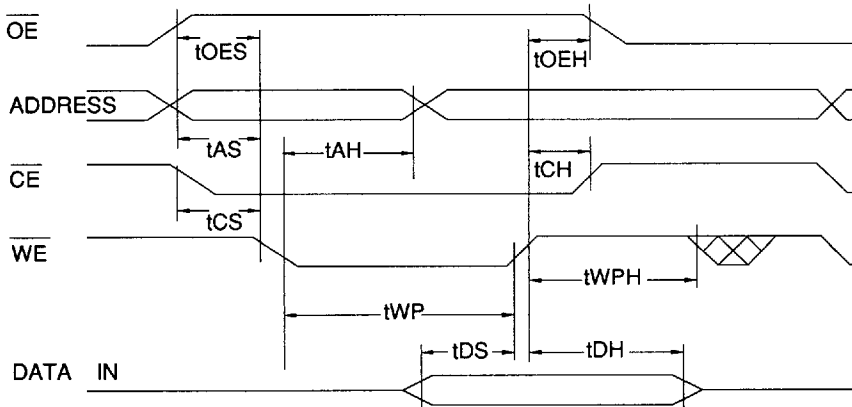
A.C. Byte Load Waveforms- $\overline{CE}$ Controlled
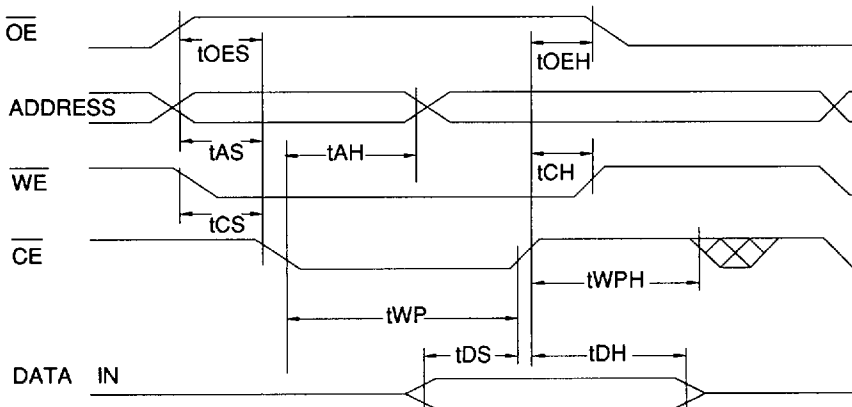
Program Cycle Characteristics

Symbol	Parameter	Min	Max	Units
twc	Write Cycle Time		10	ms
tAS	Address Set-up Time	0		ns
tAH	Address Hold Time	50		ns
tDS	Data Set-up Time	50		ns
tDH	Data Hold Time	0		ns
twP	Write Pulse Width	90		ns
tBLC	Byte Load Cycle Time		150	μs
twPH	Write Pulse Width High	100		ns

Program Cycle Waveforms
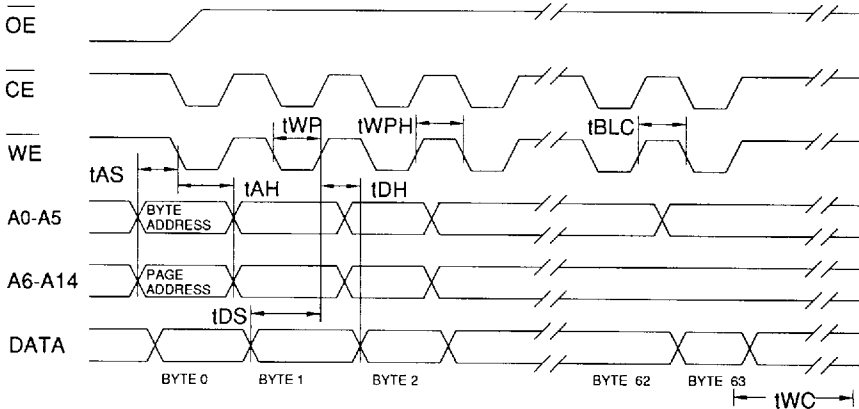
Notes: A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).

$\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.

All bytes that are not loaded within the page being programmed will be erased to FF.

7

Software Data Protection Enable Algorithm [1]

```
┌─────────────────┐
│  LOAD DATA AA   │
│       TO        │
│  ADDRESS 5555   │
└────────┬────────┘
         ↓
┌─────────────────┐
│  LOAD DATA 55   │
│       TO        │
│  ADDRESS 2AAA   │
└────────┬────────┘
         ↓
┌─────────────────┐
│  LOAD DATA A0   │
│       TO        │
│  ADDRESS 5555   │   WRITES ENABLED [2]
└────────┬────────┘
         ↓
┌─────────────────┐
│   LOAD DATA     │
│       TO    (4) │   ENTER DATA
│ PAGE (64 BYTES) │   PROTECT STATE
└─────────────────┘
```

Notes for software program code:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Data Protect state will be activated at end of program cycle.
3. Data Protect state will be deactivated at end of program period.
4. 64 bytes of data must be loaded.

Software Data Protection Disable Algorithm [1]

```
┌─────────────────┐
│  LOAD DATA AA   │
│       TO        │
│  ADDRESS 5555   │
└────────┬────────┘
         ↓
┌─────────────────┐
│  LOAD DATA 55   │
│       TO        │
│  ADDRESS 2AAA   │
└────────┬────────┘
         ↓
┌─────────────────┐
│  LOAD DATA 80   │
│       TO        │
│  ADDRESS 5555   │
└────────┬────────┘
         ↓
┌─────────────────┐
│  LOAD DATA AA   │
│       TO        │
│  ADDRESS 5555   │
└────────┬────────┘
         ↓
┌─────────────────┐
│  LOAD DATA 55   │
│       TO        │
│  ADDRESS 2AAA   │
└────────┬────────┘
         ↓
┌─────────────────┐
│  LOAD DATA 20   │
│       TO        │   EXIT DATA
│  ADDRESS 5555   │   PROTECT STATE [3]
└────────┬────────┘
         ↓
┌─────────────────┐
│   LOAD DATA     │
│       TO    (4) │
│ PAGE (64 BYTES) │
└─────────────────┘
```
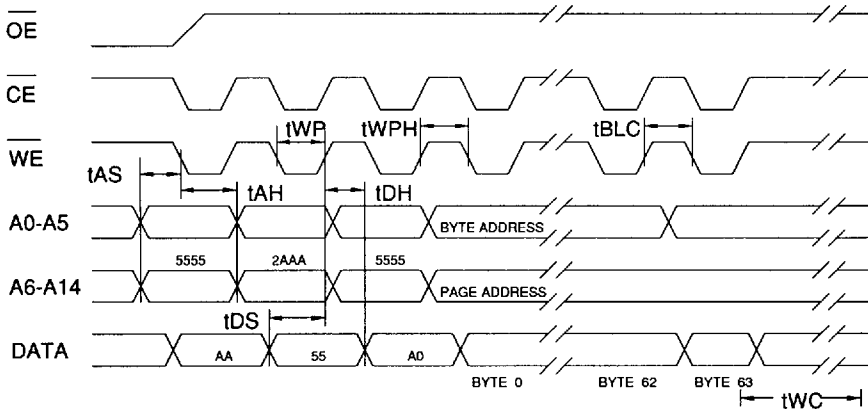
Software Protected Program Cycle Waveform

Notes:
1. A6 through A14 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
2. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
3. All bytes that are not loaded within the page being programmed will be erased to FF.

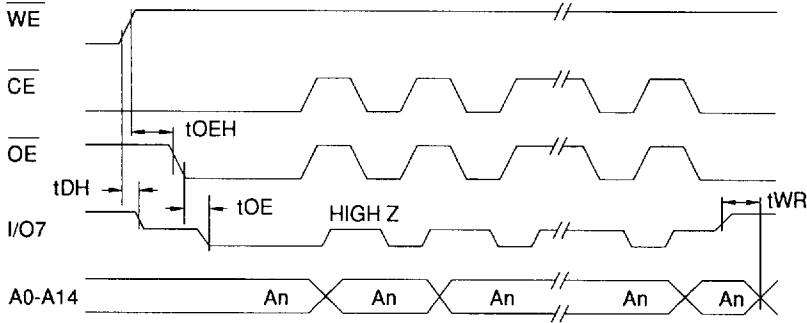## $\overline{\text{Data}}$ Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{\text{OE}}$ Hold Time	10			ns
t_{OE}	$\overline{\text{OE}}$ to Output Delay[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in A.C. Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{\text{OE}}$ Hold Time	10			ns
t_{OE}	$\overline{\text{OE}}$ to Output Delay[2]				ns
t_{OEHP}	$\overline{\text{OE}}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
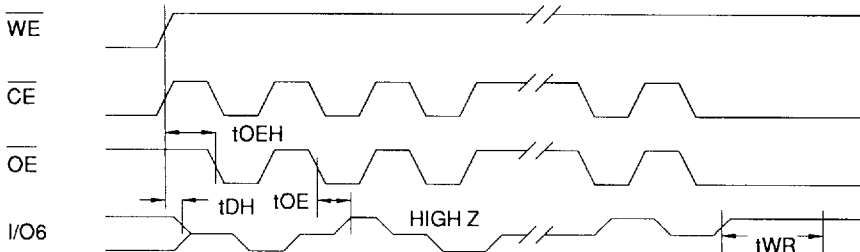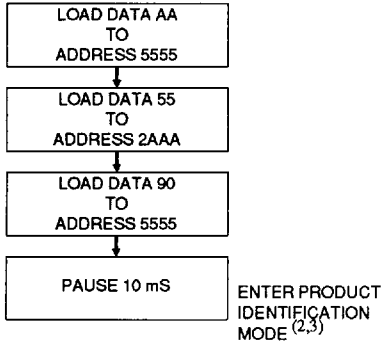2. See t_{OE} spec in A.C. Read Characteristics.

Toggle Bit Waveforms

Notes:
1. Toggling either $\overline{\text{OE}}$ or $\overline{\text{CE}}$ or both $\overline{\text{OE}}$ and $\overline{\text{CE}}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry [1]

```
┌─────────────────┐
│  LOAD DATA AA   │
│       TO        │
│  ADDRESS 5555   │
└────────┬────────┘
┌────────┴────────┐
│  LOAD DATA 55   │
│       TO        │
│  ADDRESS 2AAA   │
└────────┬────────┘
┌────────┴────────┐
│  LOAD DATA 90   │
│       TO        │
│  ADDRESS 5555   │
└────────┬────────┘
┌────────┴────────┐
│   PAUSE 10 mS   │      ENTER PRODUCT
│                 │      IDENTIFICATION
└─────────────────┘      MODE [2,3]
```

Software Product Identification Exit [1]

```
┌─────────────────┐
│  LOAD DATA AA   │
│       TO        │
│  ADDRESS 5555   │
└────────┬────────┘
┌────────┴────────┐
│  LOAD DATA 55   │
│       TO        │
│  ADDRESS 2AAA   │
└────────┬────────┘
┌────────┴────────┐
│  LOAD DATA F0   │
│       TO        │
│  ADDRESS 5555   │
└────────┬────────┘
┌────────┴────────┐
│   PAUSE 10 mS   │      EXIT PRODUCT
│                 │      IDENTIFICATION
└─────────────────┘      MODE [4]
```
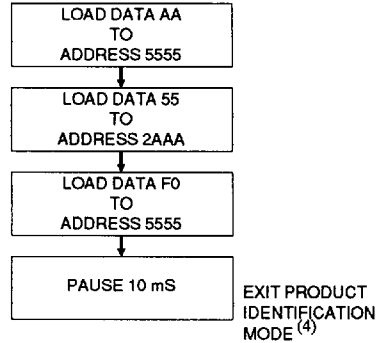
Notes for software product identification:
1. Data Format: $I/O7 - I/O0$ (Hex);
   Address Format: $A14 - A0$ (Hex).
2. $A1 - A14 = V_{IL}$.
   Manufacture Code is read for $A0 = V_{IL}$.
   Device Code is read for $A0 = V_{IH}$.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
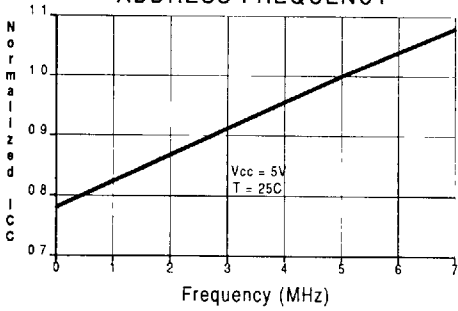5. Manufacturer Code: 1F
   Device Code: DC

NORMALIZED SUPPLY CURRENT vs. TEMPERATURE

Normalized ICC vs Temperature (C)
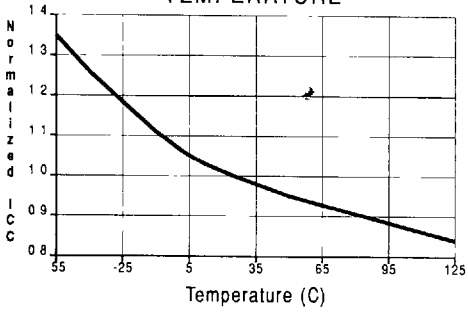
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE

Normalized ICC vs Supply Voltage (V)
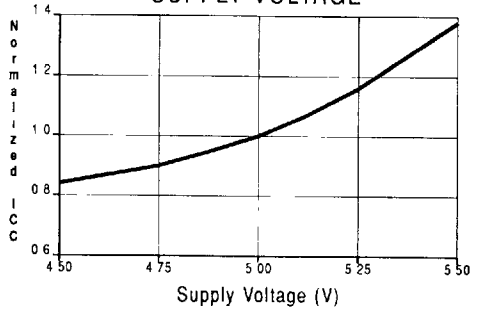
NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY

Vcc = 5V
T = 25C

Normalized ICC vs Frequency (MHz)

Ordering Information

t$_{ACC}$ (ns)	I$_{CC}$ (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	80	0.3	AT29C256-90DC AT29C256-90JC AT29C256-90PC	28D6 32J 28P6	Commercial (0° to 70°C)
90	50	0.3	AT29C256-90TC	28T	Commercial (0° to 70°C)
120	80	0.3	AT29C256-12DC AT29C256-12JC AT29C256-12LC AT29C256-12PC AT29C256-12TC	28D6 32J 32L 28P6 28T	Commercial (0° to 70°C)
			AT29C256-12DI AT29C256-12JI AT29C256-12LI AT29C256-12PI	28D6 32J 32L 28P6	Industrial (-40° to 85°C)
			AT29C256-12DM AT29C256-12LM	28D6 32L	Military (-55°C to 125°C)
			AT29C256-12DM/883 AT29C256-12LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	80	0.3	AT29C256-15DC AT29C256-15JC AT29C256-15LC	28D6 32J 32L	Commercial (0° to 70°C)
			AT29C256-15DI AT29C256-15JI AT29C256-15LI AT29C256-15PI AT29C256-15TI	28D6 32J 32L 28P6 28T	Industrial (-40° to 85°C)
			AT29C256-15DM AT29C256-15LM	28D6 32L	Military (-55°C to 125°C)
			AT29C256-15DM/883 AT29C256-15LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	80	0.3	AT29C256-20DC AT29C256-20JC AT29C256-20LC AT29C256-20PC	28D6 32J 32L 28P6	Commercial (0° to 70°C)
			AT29C256-20DI AT29C256-20JI AT29C256-20LI AT29C256-20PI	28D6 32J 32L 28P6	Industrial (-40° to 85°C)
			AT29C256-20DM AT29C256-20LM	28D6 32L	Military (-55°C to 125°C)
			AT29C256-20DM/883 AT29C256-20LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Ordering Information

| tACC (ns)	ICC (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
250	80	0.3	AT29C256-25DC AT29C256-25JC AT29C256-25LC AT29C256-25PC	28D6 32J 32L 28P6	Commercial (0° to 70°C)
250	80	0 3	AT29C256-25DI AT29C256-25JI AT29C256-25LI AT29C256-25PI	28D6 32J 32L 28P6	Industrial (-40° to 85°C)
			AT29C256-25DM AT29C256-25LM	28D6 32L	Military (-55°C to 125°C)
			AT29C256-25DM/883 AT29C256-25LM/883	28D6 32L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

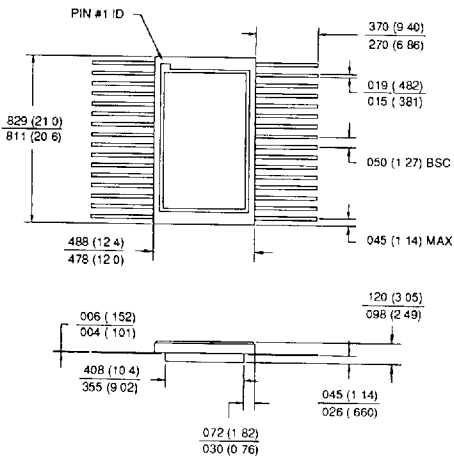| Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
32L	32 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28T	28 Lead, Thin Small Outline Package (TSOP)

1074177 0006908 51T

Packaging Information

28D6, 28 Lead, 0.600" Wide, Non-Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 D-10 CONFIG 1
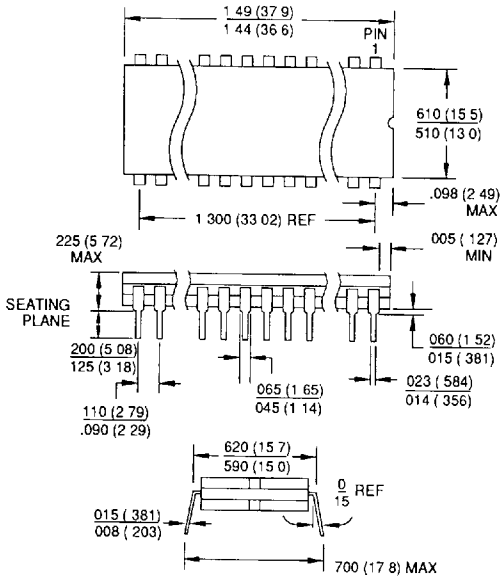
32D6, 32 Lead, 0.600" Wide, Non-Windowed,
Ceramic Dual Inline Package (Cerdip)
Dimensions in Inches and (Millimeters)
MIL-STD-1835 CONFIG A
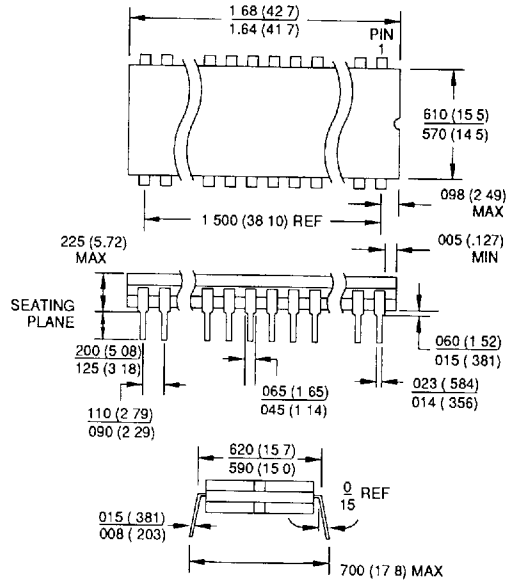
32F, 32 Lead, Non-Windowed,
Ceramic Bottom Brazed Flat Package (Flatpack)
Dimensions in Inches and (Millimeters)
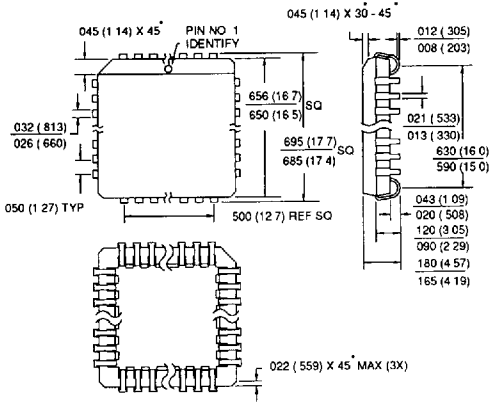MIL-STD-1835 F-18 CONFIG B
JEDEC OUTLINE MO-115

32J, 32 Leadd, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
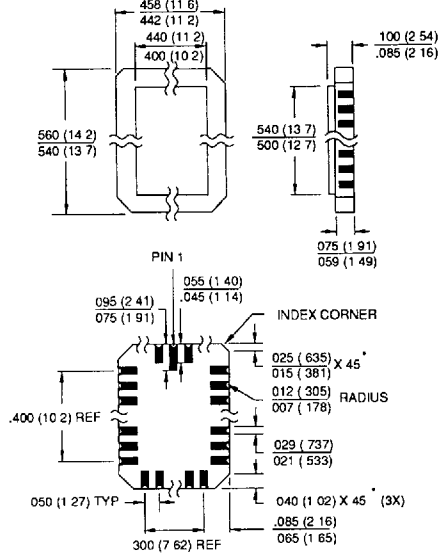JEDEC OUTLINE MO-52 AC
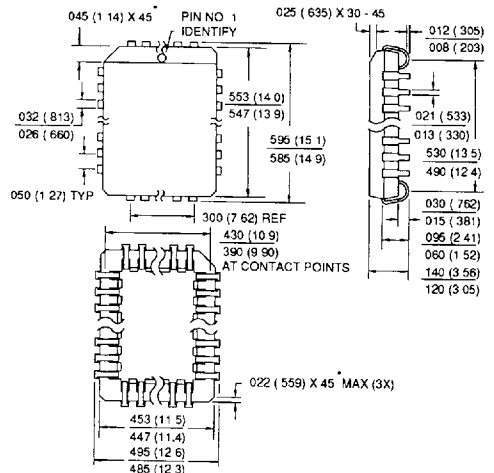
Packaging Information

44J, 44 Leadd, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
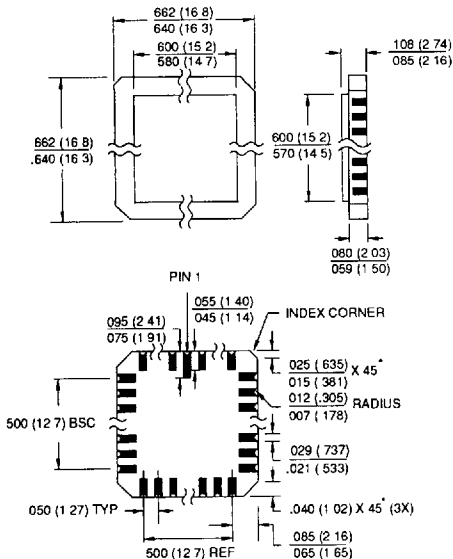JEDEC OUTLINE MO-47 AC

045 (1 14) X 45°
PIN NO 1 IDENTIFY
045 (1 14) X 30 - 45°
012 (305) / 008 (203)
656 (16 7) SQ / 650 (16 5)
032 (813) / 026 (660)
021 (533) / 013 (330)
695 (17 7) SQ / 685 (17 4)
630 (16 0) / 590 (15 0)
050 (1 27) TYP
500 (12 7) REF SQ
043 (1 09) / 020 (508)
120 (3 05) / 090 (2 29)
180 (4 57) / 165 (4 19)
022 (559) X 45° MAX (3X)

32L, 32 Pad, Non-Windowed,
Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)*

458 (11 6) / 442 (11 2) / 440 (11 2) / 400 (10 2)
100 (2 54) / .085 (2 16)
560 (14 2) / 540 (13 7)
540 (13 7) / 500 (12 7)
075 (1 91) / 059 (1 49)
PIN 1
055 (1 40) / .045 (1 14)
095 (2 41) / 075 (1 91)
INDEX CORNER
025 (635) X 45° / 015 (381)
012 (305) RADIUS / 007 (178)
.400 (10 2) REF
029 (737) / 021 (533)
050 (1 27) TYP
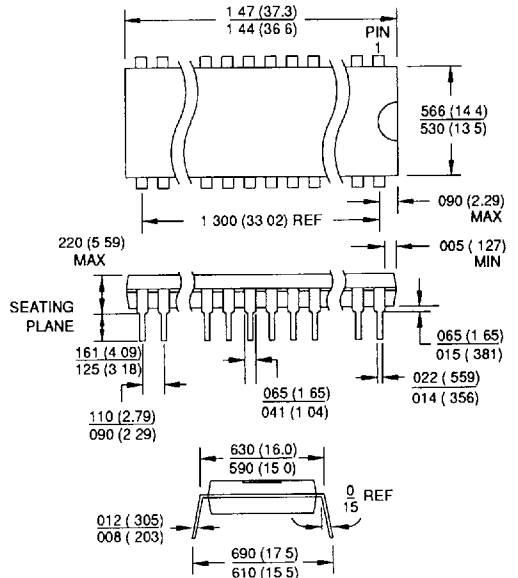040 (1 02) X 45° (3X)
.085 (2 16) / 065 (1 65)
300 (7 62) REF

*Ceramic lid standard unless specified

44L, 44 Pad, Non-Windowed,
Ceramic Leadless Chip Carrier (LCC)
Dimensions in Inches and (Millimeters)*

662 (16 8) / 640 (16 3)
600 (15 2) / 580 (14 7)
108 (2 74) / 085 (2 16)
662 (16 8) / .640 (16 3)
600 (15 2) / 570 (14 5)
080 (2 03) / 059 (1 50)
PIN 1
055 (1 40) / 045 (1 14)
INDEX CORNER
095 (2 41) / 075 (1 91)
025 (635) X 45° / 015 (381)
012 (.305) RADIUS / 007 (178)
500 (12 7) BSC
029 (737) / .021 (533)
050 (1 27) TYP
.040 (1 02) X 45° (3X)
.085 (2 16) / 065 (1 65)
500 (12 7) REF

*Ceramic lid standard unless specified.

28P6, 28 Lead, 0.600" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)

1 47 (37.3) / 1 44 (36 6)
PIN 1
566 (14 4) / 530 (13 5)
1 300 (33 02) REF
090 (2.29) MAX
005 (127) MIN
220 (5 59) MAX
SEATING PLANE
161 (4 09) / 125 (3 18)
065 (1 65) / 015 (381)
022 (559) / 014 (356)
065 (1 65) / 041 (1 04)
110 (2.79) / 090 (2 29)
630 (16.0) / 590 (15 0)
0 / 15 REF
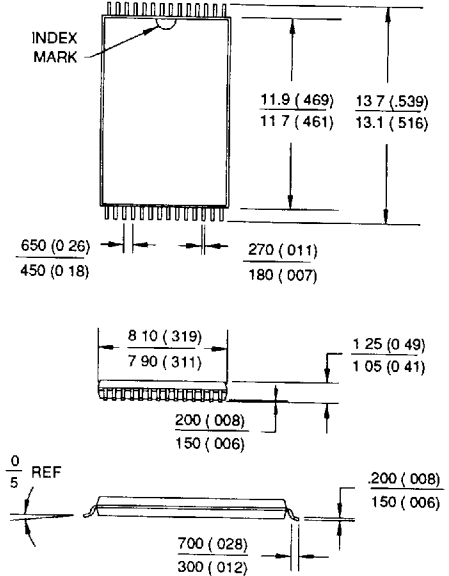012 (305) / 008 (203)
690 (17 5) / 610 (15 5)

Packages

Packaging Information

32P6, 32 Lead, 0.600" Wide,
Plastic Dual Inline Package (PDIP)
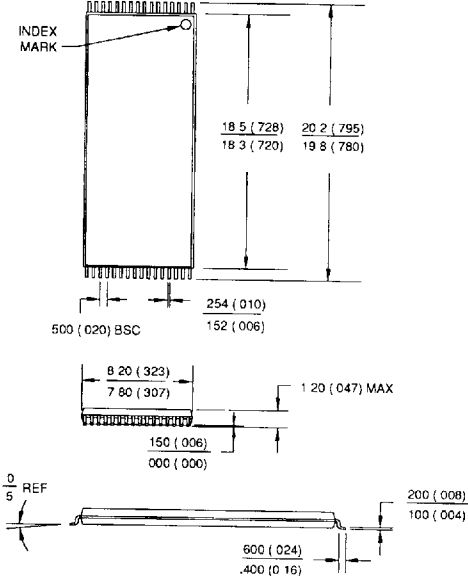Dimensions in Inches and (Millimeters)
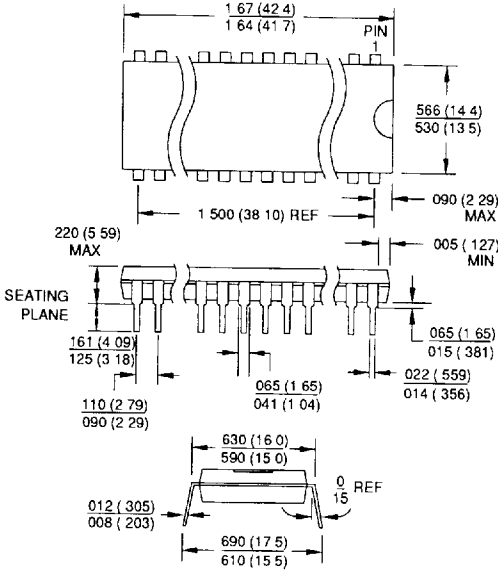
28T, 28 Lead, Plastic Thin Small Outline Package
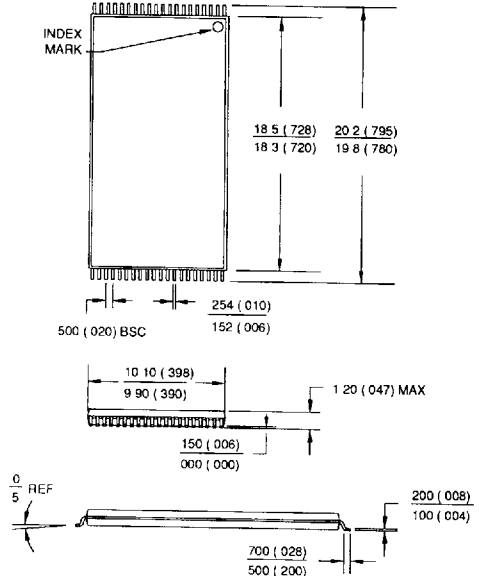(TSOP)
Dimensions in Millimeters and (Inches)*

*Controlling dimension. millimeters

32T, 32 Lead, Plastic Thin Small Outline Package
(TSOP)
Dimensions in Millimeters and (Inches)*

*Controlling dimension. millimeters

40T, 40 Lead, Plastic Thin Small Outline Package
(TSOP)
Dimensions in Millimeters and (Inches)*

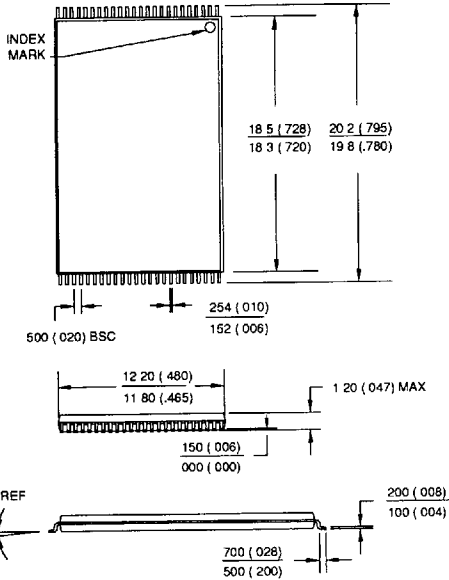

*Controlling dimension. millimeters

Packaging Information

48T, 48 Lead, Plastic Thin Small Outline Package (TSOP)
Dimensions in Millimeters and (Inches)*

INDEX MARK

$\frac{18\ 5\ (.728)}{18\ 3\ (.720)}$ $\frac{20\ 2\ (.795)}{19\ 8\ (.780)}$

$\frac{254\ (.010)}{152\ (.006)}$

500 (020) BSC

$\frac{12\ 20\ (.480)}{11\ 80\ (.465)}$

1 20 (047) MAX

$\frac{150\ (.006)}{000\ (.000)}$

$\frac{0}{5}$ REF

$\frac{200\ (.008)}{100\ (.004)}$

$\frac{700\ (.028)}{500\ (.200)}$

*Controlling dimension: millimeters