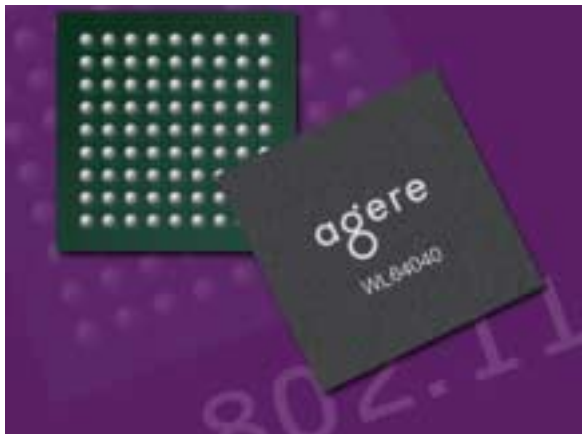
WaveLAN™ WL64040
Multimode Wireless LAN Baseband

1 Features

- Advanced low-power 0.13 µm CMOS technology.
- Interfaces:
  - — Two serial MMI interfaces.
  - — Synchronous MDI interface.
  - — Serial three-wire control interface.
  - — Parallel RF port.
  - — Analog RX/TX IQ interface.
  - — Clock output.
  - — *IEEE* 1149.1 compliant JTAG test access port .
  - — Engineering test interface.
- Analog section:
  - — Clock input (40 MHz) for direct connection.
  - — Integrated A/D and D/A converters .
  - — RSSI ADC 7-bit (10 MHz).
  - — PA ADC 8-bit (1 MHz) measures the actual output power.
  - — PA DAC 7-bit (10 MHz) controls the PA bias.
  - — Integrated PLL circuit.
  - — Low-power, high-precision band gap for generation of reference voltage.
- OFDM features:
  - — Support of OFDM modulation/demodulation for all mandatory and optional data rates (6/9/12/18/ 24/ 36/48/54 Mbits/s) according to the *IEEE* 802.11a and *IEEE* 802.11g standards.
  - — Radar detection.
  - — Interpolation/decimation.
  - — Long and short slot time.
  - — Automatic gain control.
  - — Optimized Viterbi decoder.
  - — Channel tracking.
- DSSS/CCK functions:
  - — Support of DBPSK, DQPSK, and CCK for 1/2/5.5/ 11 Mbits/s according to the *IEEE* 802.11b and *IEEE* 802.11g standards.
  - — Long and short preamble.
  - — Resampling 20 MHz—22 MHz.
  - — Barker and CW detection in parallel to OFDM preamble detection for *IEEE* 802.11g operation.
- P-LFBGA-81-6 (green package).
- Supports OFDM and CCK PHY functions for *IEEE* 802.11a, *IEEE* 802.11b, and *IEEE* 802.11g products.



2 Wireless LAN Applications

- High data-rate multimode applications.
- Client cards for notebooks, desktop PCs, and PDAs.
- Modules with WLAN functionality.
- Enterprise and home infrastructure devices.
- High-speed bridges and point-to-multipoint systems.
- Home entertainment and multimedia systems.

3 Description

The *WaveLAN* WL64040 multimode baseband processor contains the complete signal processing functionality for both OFDM and CCK modulation. It supports Agere's patented antenna diversity implementation, which provides enhanced data throughput and improved signal coverage. The baseband uses a 1.5 V internal power supply to dramatically reduce the power dissipation of high-speed OFDM signal processing, significantly improving battery life. In addition, it uses a novel method of iterative channel estimation to digitally enhance the tolerance of weak radio signals, ensuring reliable connections. It supports a digital interface to the WL60040 MAC, enabling system integration of the MAC with a simple interface to a single-chip radio module. The WL64040 provides an RF interface to connect to the WL54040 dual-mode 2.4 GHz/5 GHz RF transceiver and a digital interface to the WL60040.

3 Description (continued)

The WL64040 is designed to form a complete *IEEE* 802.11a/b/g WLAN chip set in combination with the WL60040 MAC, the WL54040 transceiver, and the WL54240 PA.

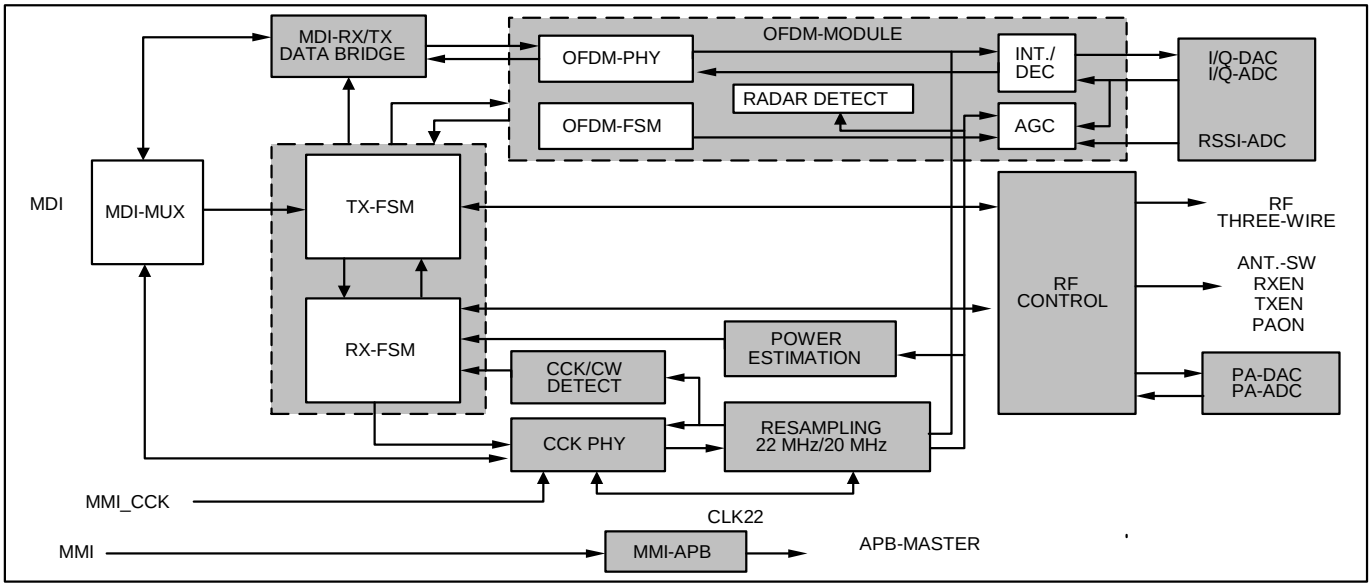


Figure 1. WL64040 Functional Block Diagram

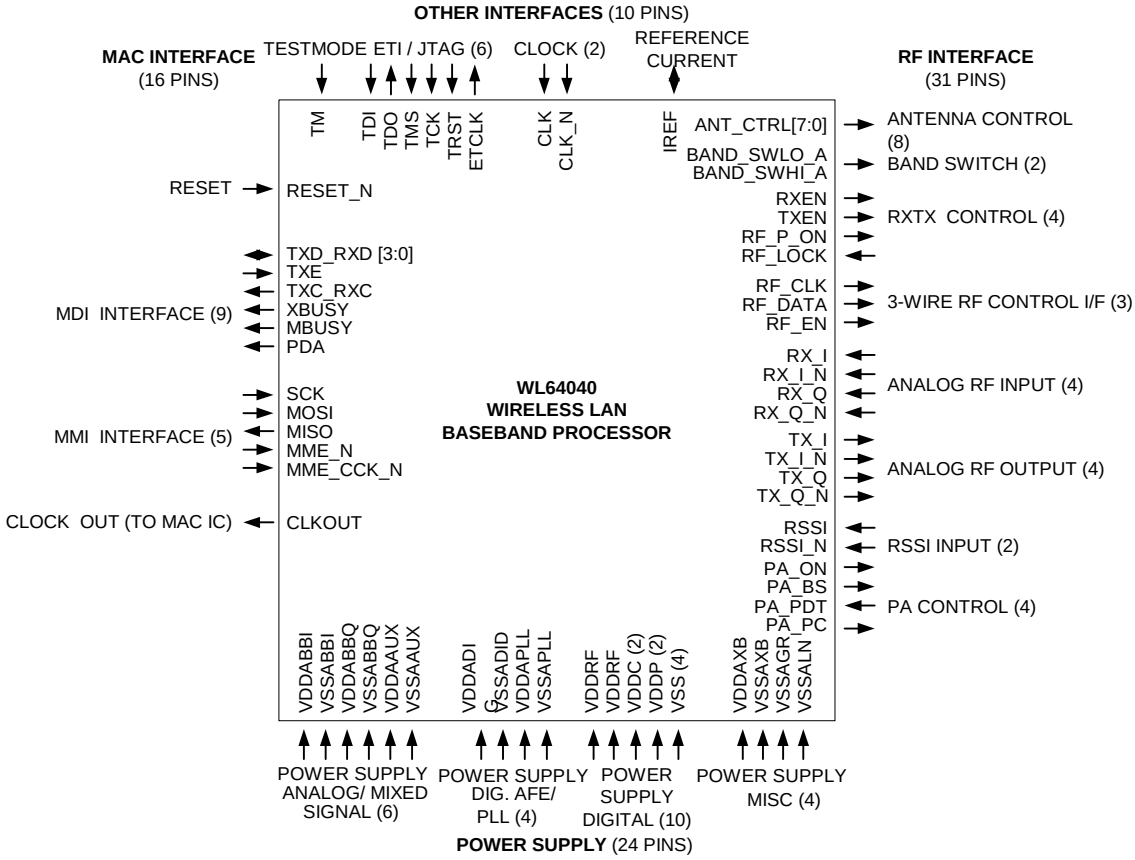


Figure 2. WL64040 Logic Symbol

4 Pin Definition and Functions

Table 1. Pin Descriptions

#	Symbol	I/O/Open Drain	Function	#	Symbol	I/O/Open Drain	Function
H1	TXD_RXD[0]	I/O	MDI RX/TX data(0).	E7	TX_EN	O	Transmitter enable.
G2	TXD_RXD[1]	I/O	MDI RX/TX data(1).	B7	PA_ON	O	Power amplifier enable.
G1	TXD_RXD[2]	I/O	MDI RX/TX data(2).	C7	PA_BS	O	Power amplifier band select
F2	TXD_RXD[3]	I/O	MDI RX/TX data(3).	H6	PA_PDT	AI	PA TX power detect input.
F3	TXE	I	MDI transmit enable.	F6	PA_PC	AO	PA TX power control.
E2	TXC_RXC	O	MDI clock.	A9	ANT_CTRL0	O	Antenna control 0.
E1	XBusy	O	MDI transceiver busy.	B8	ANT_CTRL1	O	Antenna control 1.
D1	MBusy	O	MDI medium busy.	A8	ANT_CTRL2	O	Antenna control 2.
D3	PDA	O	MDI PHY data available.	A7	ANT_CTRL3	O	Antenna control 3.
D2	SCK	I	MMI clock input.	C6	ANT_CTRL4	O	Antenna control 4.
C1	MOSI	I	MMI data input.	B5	ANT_CTRL5	O	Antenna control 5.
C3	MISO	O	MMI data output.	C5	ANT_CTRL6	O	Antenna control 6.
C2	MME_N	I	MMI enable (active-low).	E4	ANT_CTRL7	O	Antenna control 7.
B1	MME_CCK_N	I	MMI enable CCK (active-low).	C8	BAND_SWHI_A	O	5 GHz input filter switch high band.
A1	CLKOUT	O	WL60040 IC clock output (10 MHz/20 MHz).	B9	BAND_SWLO_A	O	5 GHz input filter switch low band.
F4	CLK	AI	Clock input (40 MHz).	G5	IREF	AI	Reference current 50 µA.
J4	CLK_N	AI	Clock input reference.	G6	VDDAAUX	PA	1.5 V analog supply mixed signal.
J1	RESET_N	I	Reset (active-low).	J6	VSSAAUX	GA	1.5 V analog ground mixed signal.
B3	TDI	I/O	JTAG data input/ETD0.	G7	VDDABBI	PA	Supply ADC and DAC I channel.
B4	TDO	O	JTAG data output/ETD1.	F7	VSSABBI	GA	Ground ADC and DAC I channel.
A4	TCK	I/O	JTAG clock/ETD3.	J8	VDDABBQ	PA	Supply ADC and DAC Q-channel.
C4	TMS	I/O	JTAG mode select/ETD2.	H8	VSSABBQ	GA	Ground ADC and DAC Q-channel.
D4	TRST	I/O	JTAG test reset/ETSYNC.	H3	VDDADIG	PA	Supply digital part AFE.
A5	ETCLK	O	Engineering test interface clock.	G3	VSSADIG	GA	Ground digital part AFE.
H2	TM	I	Test mode select (0 = JTAG, 1 = ETI).	G4	VDDAPLL	PA	Supply PLL.
F8	TX_I	AO	RF TX output (I-signal).	J3	VSSAPLL	GA	Ground PLL.
F9	TX_I_N	AO	RF TX output inverted (I-signal).	H5	VDDAXB	PA	Supply mixed signal.
G8	TX_Q	AO	RF TX output (Q-signal)	H4	VSSAXB	GA	Ground mixed signal.
G9	TX_Q_N	AO	RF TX output inverted (Q-signal)	J2	VSSAGR	GA	Ground guard ring.
H9	RX_I	AI	RF RX input (I-signal)	J5	VSSALN	GA	Ground low noise.
J9	RX_I_N	AI	RF RX input Inverted (I-signal)	A6	VDDC	PC	Supply core.
H7	RX_Q	AI	RF RX input (Q-signal).	A3	VDDC	PC	Supply core.
J7	RX_Q_N	AI	RF RX input inverted (Q-signal).	B6	VDDRF	PD	Supply digital RF.
E5	RSSI	AI	RF RSSI input.	D7	VDDRF	PD	Supply digital RF.

4 Pin Definitions and Functions (continued)

Table 1. Pin Descriptions (continued)

#	Symbol	I/O/Open Drain	Function	#	Symbol	I/O/Open Drain	Function
F5	RSSI_N	AI	RF RSSI input inverted.	F1	VDDP	PD	Supply MAC-interface I/O.
D8	RF_CLK	O	3-wire RF interface clock.	B2	VDDP	PD	Supply MAC-interface I/O.
D9	RF_DATA	O	3-wire RF interface data.	A2	VSS	G	Ground digital.
C9	RF_EN	O	3-wire RF interface enable.	E3	VSS	G	Ground digital.
E9	RF_P_ON	O	RF transceiver power-on.	D5	VSS	G	Ground digital.
E6	RF_LOCK	I	PLL lock detection.	D6	VSS	G	Ground digital.
E8	RX_EN	O	Receiver enable.				

5 Electrical Characteristics

Table 2. Absolute Maximum Ratings*

Parameter	Symbol	Min	Max	Unit	Parameter	Symbol	Min	Max	Unit
Supply Core	VDDP	–0.9	4.0	V	Voltage Analog	VDDA	–0.3	1.7	V
Supply Digital RF	VDDRF	–0.9	4.0	V	Supply Core	VDDC	–0.3	1.7	V

* Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 3. Operating Conditions

Parameter	Symbol	Min	Max	Unit	Parameter	Symbol	Min	Max	Unit
Temperature Range	T	–30	85	°C	Voltage Analog	VDDA	1.4	1.6	V
Supply Core	VDDP	3.0	3.6	V	Supply Core	VDDC	1.4	1.6	V
Supply Digital RF	VDDRF	2.6	3.6	V					

6 Ordering Information

Part Number	Temperature Range (°C)	Package	Packing	MOQ	Comcode
WL64040-D	–30 to +85	P-LFBGA-81-6	TBD	TBD	7000550100

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