HM5264165 Series
HM5264805 Series
HM5264405 Series

1,048,576-word × 16-bit × 4-bank Synchronous Dynamic RAM
2,097,152-word × 8-bit × 4-bank Synchronous Dynamic RAM
4,194,304-word × 4-bit × 4-bank Synchronous Dynamic RAM

HITACHI

ADE-203-497(Z)
Preliminary
Rev. 0.2
Dec. 17, 1996

Description

All inputs and outputs are reffered to the rising edge of the clock input. The HM5264165 Series, HM5264805 Series, HM5264405 Series are offered in 4 banks for improved performance.

Features

- 3.3 V power supply
- Clock frequency: 100 MHz/83 MHz/66 MHz
- LVTTL interface
- Single pulsed $\overline{RAS}$
- 4 banks can operate simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length: 1/2/4/8/full page
- Programmable burst sequence
  - — Sequential/interleave
- Full page burst length capability
  - — Sequential burst
  - — Burst stop capability
- Programmable $\overline{CAS}$ latency: 2/3
- 4096 refresh cycles: 64 ms

Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

Hitachi semiconductor

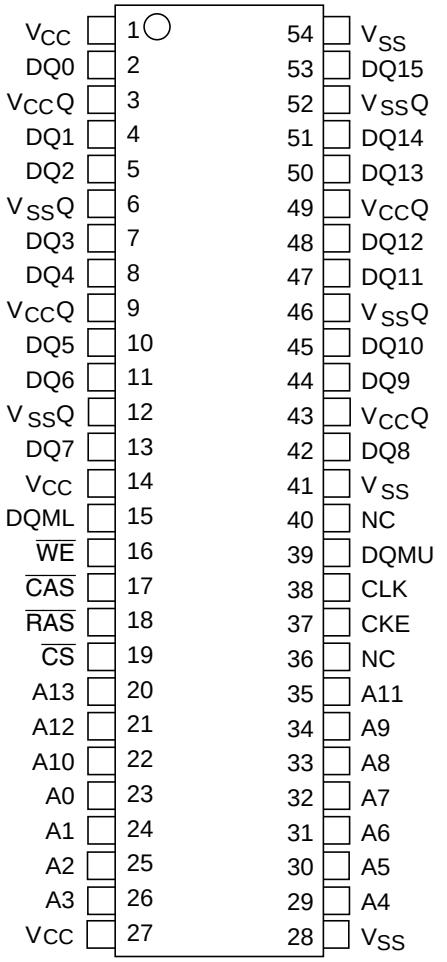
- 2 variations of refresh
  - — Auto refresh
  - — Self refresh

Ordering Information

Type No.	Frequency	Package
HM5264165TT-10	100 MHz	400-mill 54-pin plastic TSOP II (TTP-54D)
HM5264165TT-12	83 MHz	
HM5264165TT-15	66 MHz	
HM5264805TT-10	100 MHz	
HM5264805TT-12	83 MHz	
HM5264805TT-15	66 MHz	
HM5264405TT-10	100 MHz	
HM5264405TT-12	83 MHz	
HM5264405TT-15	66 MHz	

Pin Arrangement

HM5264165TT Series



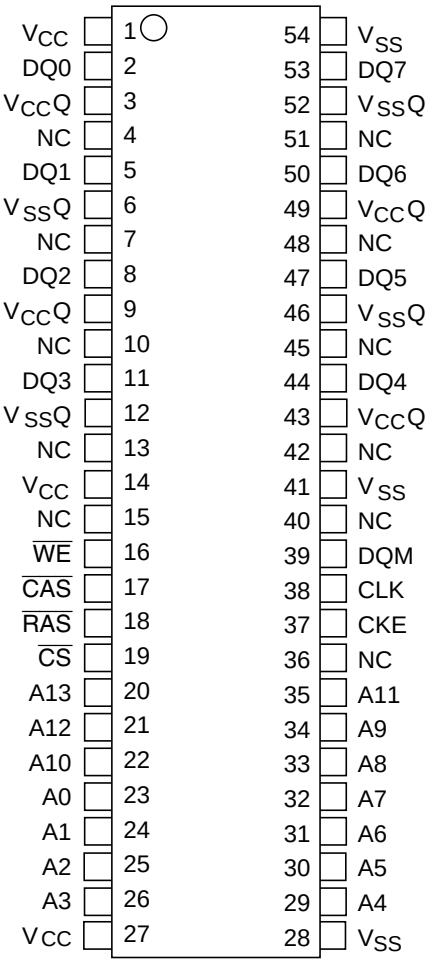
(Top view)

Pin Description

Pin name	Function
A0 to A13	Address input
	— Row address A0 to A11
	— Column address A0 to A7
	— Bank select address A12/A13
DQ0 to DQ15	Data-input/output
$\overline{CS}$	Chip select
$\overline{RAS}$	Row address strobe command
$\overline{CAS}$	Column address strobe command
$\overline{WE}$	Write enable
DQMU/DQML	Input/output mask
CLK	Clock input
CKE	Clock enable
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
$V_{CC}Q$	Power for DQ circuit
$V_{SS}Q$	Ground for DQ circuit
NC	No connection
$\overline{WE}$	Write enable

Pin Arrangement

HM5264805TT Series



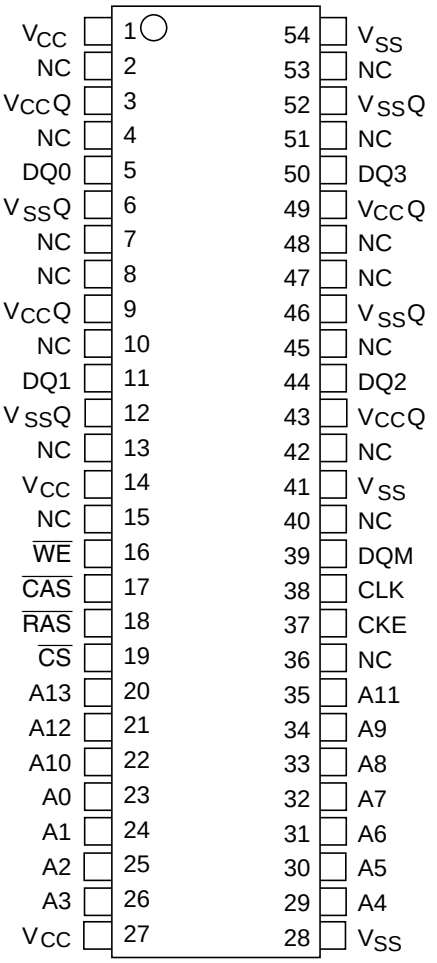
(Top view)

Pin Description

Pin name	Function	
A0 to A13	Address input	
	— Row address	A0 to A11
	— Column address	A0 to A8
	— Bank select address	A12/A13
DQ0 to DQ7	Data-input/output	
$\overline{CS}$	Chip select	
$\overline{RAS}$	Row address strobe command	
$\overline{CAS}$	Column address strobe command	
$\overline{WE}$	Write enable	
DQM	Input/output mask	
CLK	Clock input	
CKE	Clock enable	
V_{CC}	Power for internal circuit	
V_{SS}	Ground for internal circuit	
$V_{CC}Q$	Power for DQ circuit	
$V_{SS}Q$	Ground for DQ circuit	
NC	No connection	

Pin Arrangement

HM5264405TT Series

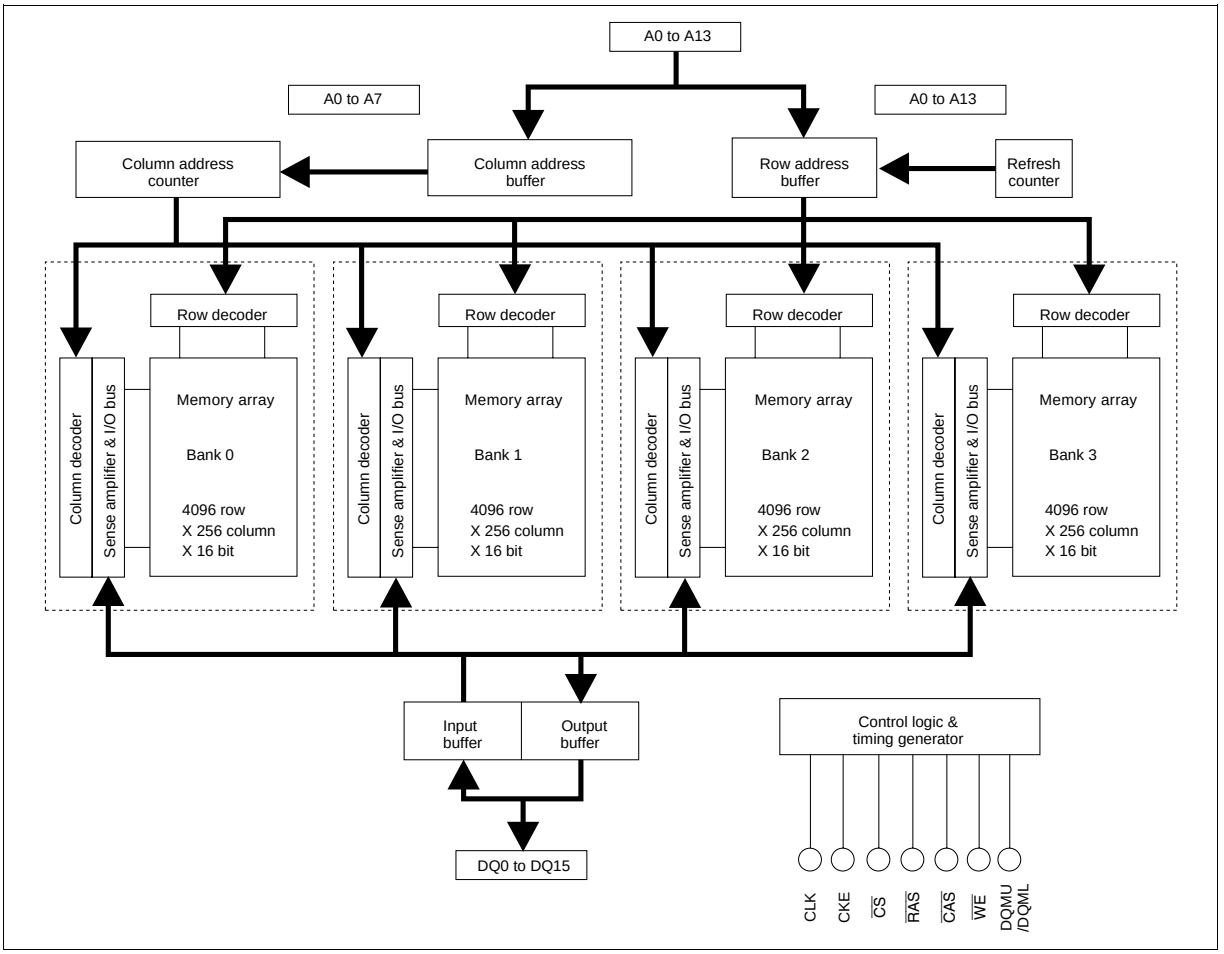


(Top view)

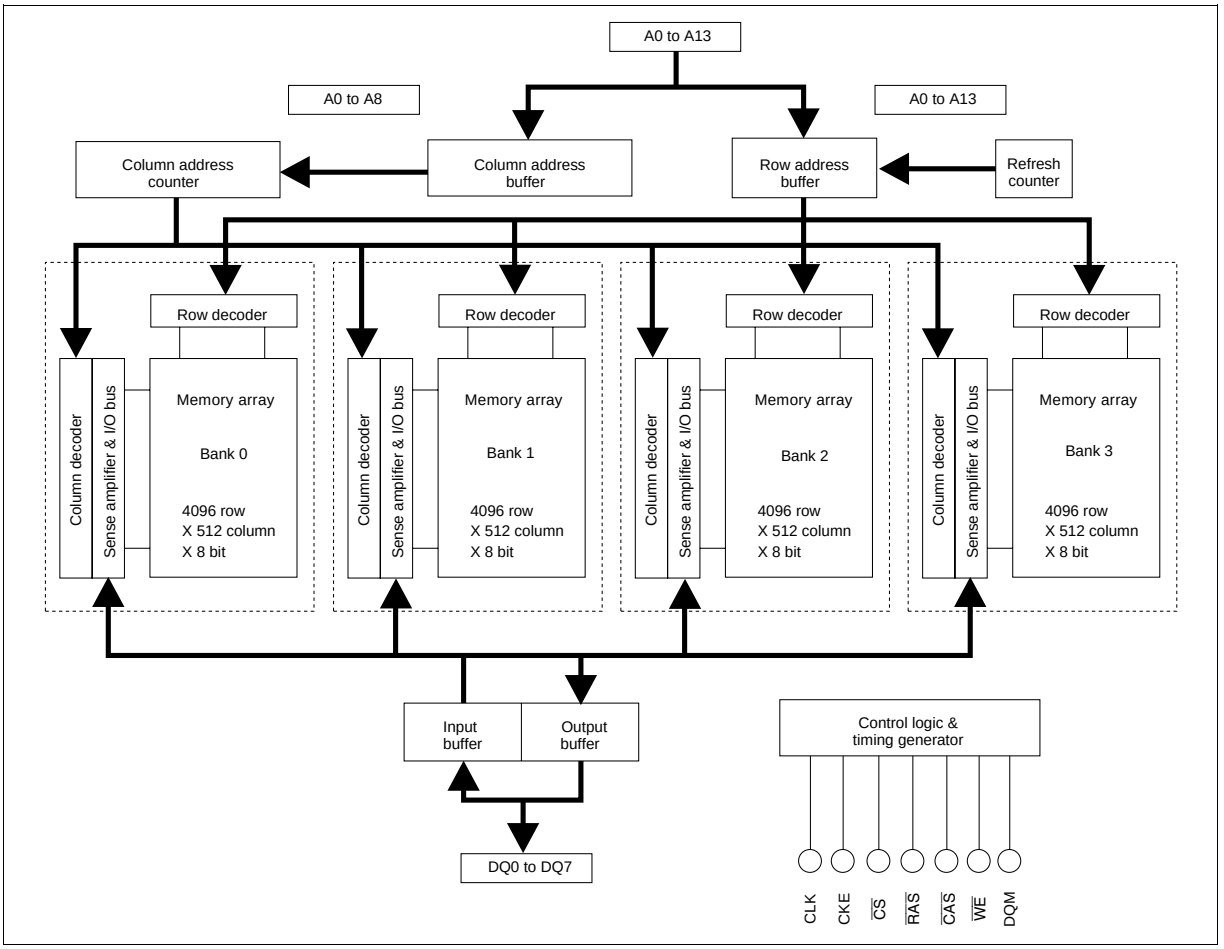
Pin Description

Pin name	Function	
A0 to A13	Address input	
	— Row address	A0 to A11
	— Column address	A0 to A9
	— Bank select address	A12/A13
DQ0 to DQ3	Data-input/output	
$\overline{CS}$	Chip select	
$\overline{RAS}$	Row address strobe command	
$\overline{CAS}$	Column address strobe command	
$\overline{WE}$	Write enable	
DQM	Input/output mask	
CLK	Clock input	
CKE	Clock enable	
V_{CC}	Power for internal circuit	
V_{SS}	Ground for internal circuit	
$V_{CC}Q$	Power for DQ circuit	
$V_{SS}Q$	Ground for DQ circuit	
NC	No connection	

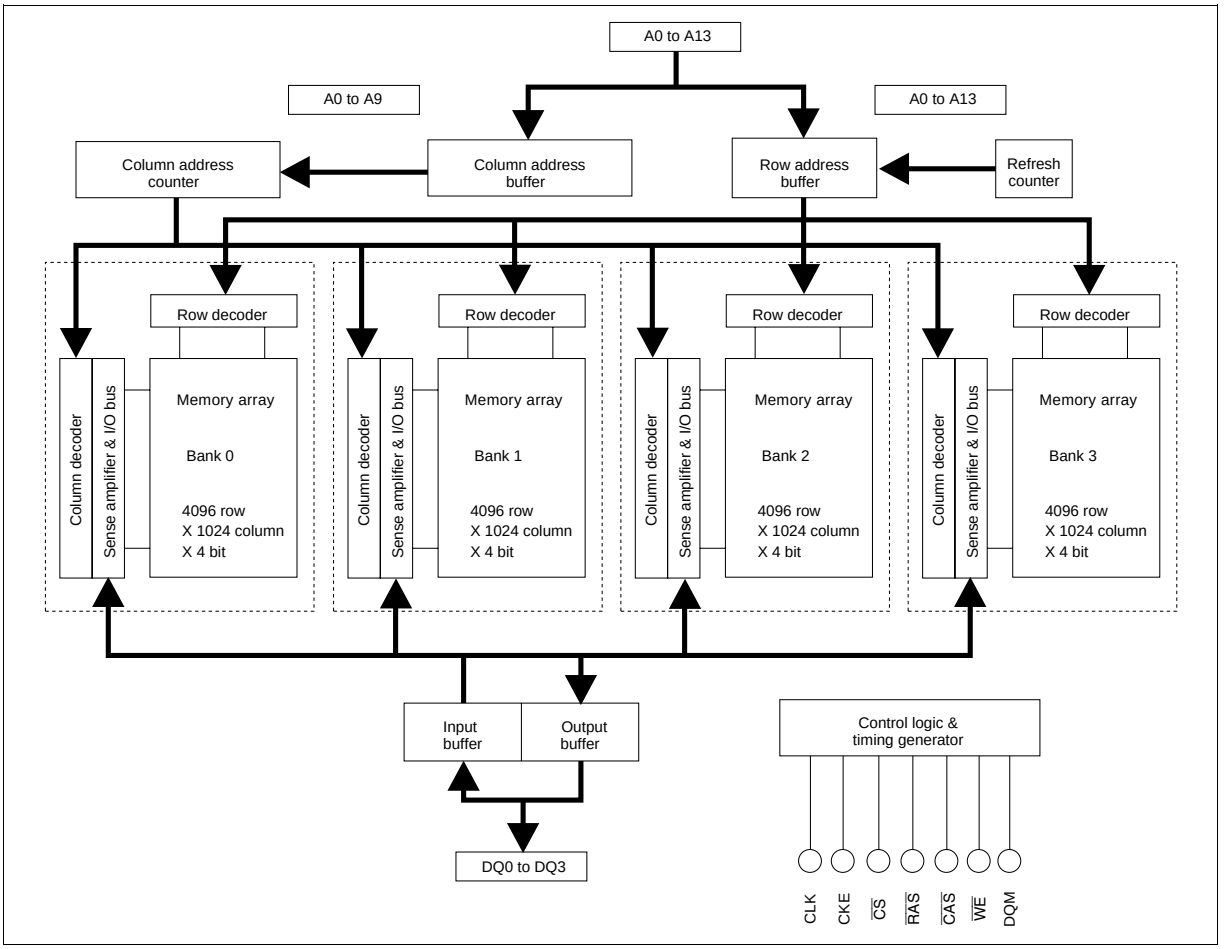
Block Diagram (HM5264165 Series)



Block Diagram (HM5264805 Series)



Block Diagram (HM5264405 Series)



Pin Functions

CLK (input pin): CLK is the master clock input to this pin. The other input signals are referred at CLK rising edge.

$\overline{CS}$ (input pin): When $\overline{CS}$ is Low, the command input cycle becomes valid. When $\overline{CS}$ is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (input pins): Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.

A0 to A11 (input pins): Row address (AX0 to AX11) is determined by A0 to A11 level at the bank active command cycle CLK rising edge. Column address (AY0 to AY7; HM5264165 Series, AY0 to AY8; HM5264805 Series, AY0 to AY9; HM5264405 Series) is determined by A0 to A7, A8 or A9 (A7; HM5264165 Series, A8; HM5264805 Series, A9; HM5264405 Series) level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by A12/A13 (BS) is precharged.

A12/A13 (input pin): A12/A13 are bank select signal (BS). The memory array of the HM5264165 Series, HM5264805 Series, the HM5264405 Series is divided into bank 0, bank 1, bank 2 and bank 3. HM5264165 Series contain 4096-row × 256-column × 16-bit. HM5264805 Series contain 4096-row × 512-column × 8-bit. HM5264405 Series contain 4096-row × 1024-column × 4-bit. If A12 is Low and A13 is Low, bank 0 is selected. If A12 is High and A13 is Low, bank 1 is selected. If A12 is Low and A13 is High, bank 2 is selected. If A12 is High and A13 is High, bank 3 is selected.

CKE (input pin): This pin determines whether or not the next CLK is valid. If CKE is High, the next CLK rising edge is valid. If CKE is Low, the next CLK rising edge is invalid. This pin is used for power-down and clock suspend modes.

DQM, DQMU/DQML (input pins): DQM, DQMU/DQML controls input/output buffers.

Read operation: If DQM, DQMU/DQML is High, the output buffer becomes High-Z. If the DQM, DQMU/DQML is Low, the output buffer becomes Low-Z. (The latency of DQM, DQMU/DQML during reading is 2.)

Write operation: If DQM, DQMU/DQML is High, the previous data is held (the new data is not written). If DQM, DQMU/DQML is Low, the data is written. (The latency of DQM, DQMU/DQML during writing is 0.)

DQ0 to DQ15 (DQ pins): Data is input to and output from these pins (DQ0 to DQ15; HM5264165 Series, DQ0 to DQ7; HM5264805 Series, DQ0 to DQ3; HM5264405 Series). These pins are the same as those of a conventional DRAM.

V_{CC} and $V_{CC}Q$ (power supply pins): 3.3 V is applied. (V_{CC} is for the internal circuit and $V_{CC}Q$ is for the output buffer.)

V_{SS} and $V_{SS}Q$ (power supply pins): Ground is connected. (V_{SS} is for the internal circuit and $V_{SS}Q$ is for the output buffer.)

Command Operation

Command Truth Table

The synchronous DRAM recognizes the following commands specified by the $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and address pins.

Function	Symbol	CKE n - 1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A12/A13	A10	A0 to A11
Ignore command	DESL	H	×	H	×	×	×	×	×	×
No operation	NOP	H	×	L	H	H	H	×	×	×
Burst stop in full page	BST	H	×	L	H	H	L	×	×	×
Column address and read command	READ	H	×	L	H	L	H	V	L	V
Read with auto-precharge	READ A	H	×	L	H	L	H	V	H	V
Column address and write command	WRIT	H	×	L	H	L	L	V	L	V
Write with auto-precharge	WRIT A	H	×	L	H	L	L	V	H	V
Row address strobe and bank active	ACTV	H	×	L	L	H	H	V	V	V
Precharge select bank	PRE	H	×	L	L	H	L	V	L	×
Precharge all bank	PALL	H	×	L	L	H	L	×	H	×
Refresh	REF/SELF	H	V	L	L	L	H	×	×	×
Mode register set	MRS	H	×	L	L	L	L	V	V	V

Note: H: V_{IH}. L: V_{IL}. ×: V_{IH} or V_{IL}. V: Valid address input

Ignore command [DESL]: When this command is set ($\overline{CS}$ is High), the synchronous DRAM ignore command input at the clock. However, the internal status is held.

No operation [NOP]: This command is not an execution command. However, the internal operations continue.

Burst stop in full-page [BST]: This command stops a full-page burst operation (burst length = full-page (256; HM5264165 Series, 512; HM5264805 Series, 1024; HM5264405 Series)), and is illegal otherwise.

Column address strobe and read command [READ]: This command starts a read operation. In addition, the start address of burst read is determined by the column address (AY0 to AY7; HM5264165 Series, AY0 to AY8; HM5264805 Series, AY0 to AY9; HM5264405 Series) and the bank select address (BS). After the read operation, the output buffer becomes High-Z.

Read with auto-precharge [READ A]: This command automatically performs a precharge operation after a burst read with a burst length of 1, 2, 4 or 8. When the burst length is full-page, this command is illegal.

Column address strobe and write command [WRIT]: This command starts a write operation. When the burst write mode is selected, the column address (AY0 to AY7; HM5264165 Series, AY0 to AY8; HM5264805 Series, AY0 to AY9; HM5264405 Series) and the bank select address (A12/A13) become the burst write start address. When the single write mode is selected, data is only written to the location specified by the column address (AY0 to AY7; HM5264165 Series, AY0 to AY8; HM5264805 Series, AY0 to AY9; HM5264405 Series) and the bank select address (A12/A13).

Write with auto-precharge [WRIT A]: This command automatically performs a precharge operation after a burst write with a length of 1, 2, 4 or 8, or after a single write operation. When the burst length is full-page, this command is illegal.

Row address strobe and bank activate [ACTV]: This command activates the bank that is selected by A12/A13 (BS) and determines the row address (AX0 to AX11). When A12 and A13 are Low, bank 0 is activated. When A12 is High and A13 is Low, bank 1 is activated. When A12 is Low and A13 is High, bank 2 is activated. When A12 and A13 are High, bank 3 is activated.

Precharge selected bank [PRE]: This command starts precharge operation for the bank selected by A12/A13. If A12 and A13 are Low, bank 0 is selected. If A12 is High and A13 is Low, bank 1 is selected. If A12 is Low amd A13 is High, bank 2 is selected. If A12 and A13 are High, bank 3 is selected.

Precharge all banks [PALL]: This command starts a precharge operation for all banks.

Refresh [REF/SELF]: This command starts the refresh operation. There are two types of refresh operation, the one is auto-refresh, and the other is self-refresh. For details, refer to the CKE truth table section.

Mode register set [MRS]: Synchronous DRAM has a mode register that defines how it operates. The mode register is specified by the address pins (A0 to A13) at the mode register set cycle. For details, refer to the mode register configuration. After power on, the contents of the mode register are undefined, execute the mode register set command to set up the mode register.

DQM Truth Table (HM5264165 Series)

Function	Symbol	CKE n - 1	n	DQMU	DQML
Upper byte write enable/output enable	ENBU	H	×	L	×
Lower byte write enable/output enable	ENBL	H	×	×	L
Upper byte write inhibit/output disable	MASKU	H	×	H	×
Lower byte write inhibit/output disable	MASKL	H	×	×	H

Note: H: V_{IH}. L: V_{IL}. ×: V_{IH} or V_{IL}.
Write: I_{DID} is needed.
Read: I_{DOD} is needed.

The HM5264165 series can mask input/output data by means of DQMU/DQML. DQMU masks the upper byte and DQML masks the lower byte.

During reading, the output buffer is set to Low-Z by setting DQMU/DQML to Low, enabling data output. On the other hand, when DQMU/DQML is set to High, the output buffer becomes High-Z, disabling data output.

During writing, data is written by setting DQMU/DQML to Low. When DQMU/DQML is set to High, the previous data is held (the new data is not written). Desired data can be masked during burst read or burst write by setting DQMU/DQML. For details, refer to the DQMU/DQML control section of the HM5264165 Series operating instructions.

DQM Truth Table (HM5264805 Series, HM5264405 Series)

Function	Symbol	n - 1	n	DQM
Write enable/output enable	ENB	H	×	L
Write inhibit/output disable	MASK	H	×	H

Note: H: V_{IH}. L: V_{IL}. ×: V_{IH} or V_{IL}.
Write: I_{DID} is needed.
Read: I_{DOD} is needed.

The HM5264805 series, HM5264405 Series can mask input/output data by means of DQM.

During reading, the output buffer is set to Low-Z by setting DQM to Low, enabling data output. On the other hand, when DQM is set to High, the output buffer becomes High-Z, disabling data output.

During writing, data is written by setting DQM to Low. When DQM is set to High, the previous data is held (the new data is not written). Desired data can be masked during burst read or burst write by setting DQM. For details, refer to the DQM control section of the HM5264805 Series, HM5264405 Series operating instructions.

CKE Truth Table

Current state	Function	CKE n - 1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
Active	Clock suspend mode entry	H	L	H	×	×	×	×
Any	Clock suspend	L	L	×	×	×	×	×
Clock suspend	Clock suspend mode exit	L	H	×	×	×	×	×
Idle	Auto-refresh command (REF)	H	H	L	L	L	H	×
Idle	Self-refresh entry (SELF)	H	L	L	L	L	H	×
Idle	Power down entry	H	L	L	H	H	H	×
		H	L	H	×	×	×	×
Self refresh	Self refresh exit (SELFX)	L	H	L	H	H	H	×
		L	H	H	×	×	×	×
Power down	Power down exit	L	H	L	H	H	H	×
		L	H	H	×	×	×	×

Note: H: V_{IH}. L: V_{IL}. ×: V_{IH} or V_{IL}.

Clock suspend mode entry: The synchronous DRAM enters clock suspend mode from active mode by setting CKE to Low. The clock suspend mode changes depending on the current status (1 clock before) as shown below.

ACTIVE clock suspend: This suspend mode ignores inputs after the next clock by internally maintaining the bank active status.

READ suspend and READ A suspend: The data being output is held (and continues to be output).

WRITE suspend and WRIT A suspend: In this mode, external signals are not accepted. However, the internal state is held.

Clock suspend: During clock suspend mode, keep the CKE to Low.

Clock suspend mode exit: The synchronous DRAM exits from clock suspend mode by setting CKE to High during the clock suspend state.

IDLE: In this state, all banks are not selected, and completed precharge operation.

Auto-refresh command [REF]: When this command is input from the IDLE state, the synchronous DRAM starts auto-refresh operation. (The auto-refresh is the same as the CBR refresh of conventional DRAMs.) During the auto-refresh operation, refresh address and bank select address are generated inside the synchronous DRAM. For every auto-refresh cycle, the internal address counter is updated. Accordingly, 4096 times are required to refresh the entire memory. Before executing the auto-refresh command, all the banks must be in the IDLE state. In addition, since the precharge for all banks is automatically performed after auto-refresh, no precharge command is required after auto-refresh.

Self-refresh entry [SELF]: When this command is input during the IDLE state, the synchronous DRAM starts self-refresh operation. After the execution of this command, self-refresh continues while CKE is Low. Since self-refresh is performed internally and automatically, external refresh operations are unnecessary.

Power down mode entry: When this command is executed during the IDLE state, the synchronous DRAM enters power down mode. In power down mode, power consumption is suppressed by cutting off the initial input circuit.

Self-refresh exit: When this command is executed during self-refresh mode, the synchronous DRAM can exit from self-refresh mode. After exiting from self-refresh mode, the synchronous DRAM enters the IDLE state.

Power down exit: When this command is executed at the power down mode, the synchronous DRAM can exit from power down mode. After exiting from power down mode, the synchronous DRAM enters the IDLE state.

Function Truth Table

The following table shows the operations that are performed when each command is issued in each mode of the synchronous DRAM.

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Precharge	H	×	×	×	×	DESL	Enter IDLE after t_{RP}
	L	H	H	H	×	NOP	Enter IDLE after t_{RP}
	L	H	H	L	×	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A10	PRE, PALL	NOP
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Idle	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Bank and row active
	L	L	H	L	BA, A10	PRE, PALL	NOP
	L	L	L	H	×	REF, SELF	Refresh
	L	L	L	L	MODE	MRS	Mode register set

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Row active	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	Begin read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Begin write
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank*3
	L	L	H	L	BA, A10	PRE, PALL	Precharge
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Read	H	×	×	×	×	DESL	Continue burst to end
	L	H	H	H	×	NOP	Continue burst to end
	L	H	H	L	×	BST	Burst stop to full page
	L	H	L	H	BA, CA, A10	READ/READ A	Continue burst read to $\overline{CAS}$ latency and New read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst read/start write
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank*3
	L	L	H	L	BA, A10	PRE, PALL	Term burst read and Precharge
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Read with	H	×	×	×	×	DESL	Continue burst to end and precharge
auto-precharge	L	H	H	H	×	NOP	Continue burst to end and precharge
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank*3
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Write	H	×	×	×	×	DESL	Continue burst to end
	L	H	H	H	×	NOP	Continue burst to end
	L	H	H	L	×	BST	Burst stop on full page
	L	H	L	H	BA, CA, A10	READ/READ A	Term burst and New read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst and New write
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank*[3]
	L	L	H	L	BA, A10	PRE, PALL	Term burst write and Precharge*[2]
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Write with	H	×	×	×	×	DESL	Continue burst to end and precharge
auto-precharge	L	H	H	H	×	NOP	Continue burst to end and precharge
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank*[3]
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Refresh	H	×	×	×	×	DESL	Enter IDLE after t_{RC}
(auto-refresh)	L	H	H	H	×	NOP	Enter IDLE after t_{RC}
	L	H	H	L	×	BST	Enter IDLE after t_{RC}
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Notes: 1. H: V_{IH}. L: V_{IL}. ×: V_{IH} or V_{IL}.
The other combinations are inhibit.
2. An interval of t_{DPL} is required between the final valid data input and the precharge command.
3. If t_{RRD} is not satisfied, this operation is illegal.

From [PRECHARGE]

To [DESL], [NOP] or [BST]: When these commands are executed, the synchronous DRAM enters the IDLE state after t_{RP} has elapsed from the completion of precharge.

From [IDLE]

To [DESL], [NOP], [BST], [PRE] or [PALL]: These commands result in no operation.

To [ACTV]: The bank specified by the address pins and the ROW address is activated.

To [REF], [SELF]: The synchronous DRAM enters refresh mode (auto-refresh or self-refresh).

To [MRS]: The synchronous DRAM enters the mode register set cycle.

From [ROW ACTIVE]

To [DESL], [NOP] or [BST]: These commands result in no operation.

To [READ], [READ A]: A read operation starts. (However, an interval of t_{RCD} is required.)

To [WRIT], [WRIT A]: A write operation starts. (However, an interval of t_{RCD} is required.)

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands set the synchronous DRAM to precharge mode. (However, an interval of t_{RAS} is required.)

From [READ]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: Data output by the previous read command continues to be output. After $\overline{CAS}$ latency, the data output resulting from the next command will start.

To [WRIT], [WRIT A]: These commands stop a burst read, and start a write cycle.

To [ACTV]: This command makes other banks bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop a burst read, and the synchronous DRAM enters precharge mode.

From [READ with AUTO-PRECHARGE]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed, and the synchronous DRAM then enters precharge mode.

To [ACTV]: This command makes other banks bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

From [WRITE]

To [DESL], [NOP]: These commands continue write operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: These commands stop a burst and start a read cycle.

To [WRIT], [WRIT A]: These commands stop a burst and start the next write cycle.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop burst write and the synchronous DRAM then enters precharge mode.

From [WRITE with AUTO-PRECHARGE]

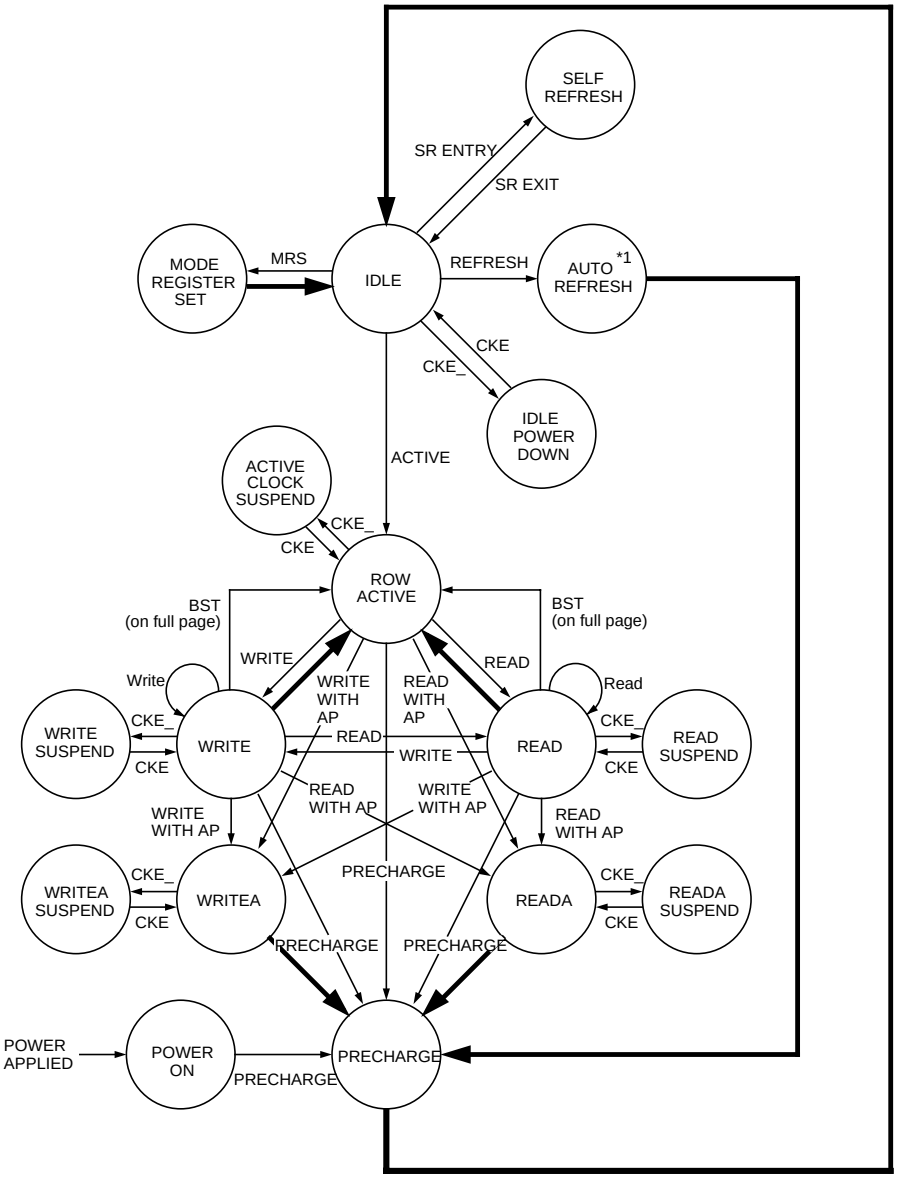
To [DESL], [NOP]: These commands continue write operations until the burst is completed, and the synchronous DRAM enters precharge mode.

To [ACTV]: This command makes the other bank activ. (However, an interval of t_{RC} is required.) Attempting to make the currently active bank active results in an illegal command.

From [REFRESH]

To [DESL], [NOP], [BST]: After an auto-refresh cycle (after t_{RC}), the synchronous DRAM automatically enters the IDLE state.

Simplified State Diagram



Automatic transition after completion of command.
Transition resulting from command input.

Note: 1. After the auto-refresh operation, precharge operation is performed automatically and enter the IDLE state.

Mode Register Configuration

The mode register is set by the input to the address pins (A0 to A11) during mode register set cycles. The mode register consists of five sections, each of which is assigned to address pins.

A13, A12, A11, A10, A9 A8: (OPCODE): The synchronous DRAM has two types of write modes. One is the burst write mode, and the other is the single write mode. These bits specify write mode.

Burst read and BURST WRITE: Burst write is performed for the specified burst length starting from the column address specified in the write cycle.

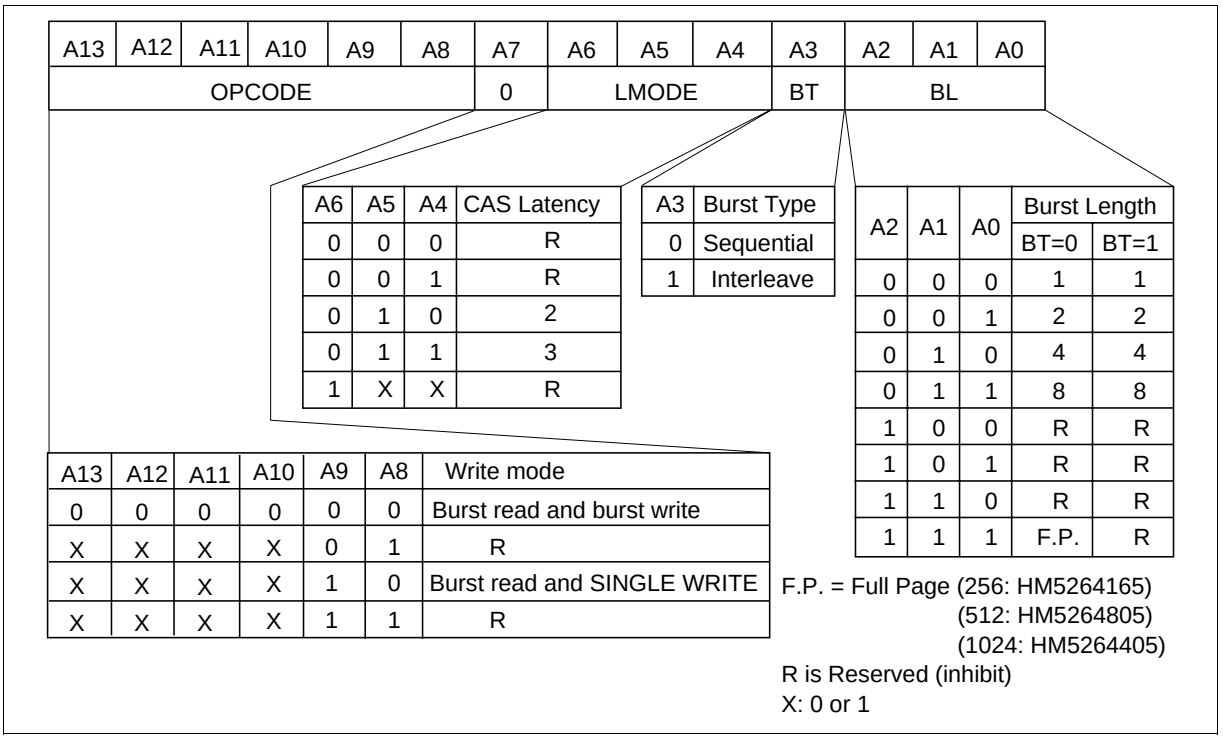
Burst read and SINGLE WRITE: Data is only written to the column address specified during the write cycle, regardless of the burst length.

A7: Keep this bit Low at the mode register set cycle.

A6, A5, A4: (LMODE): These pins specify the $\overline{\text{CAS}}$ latency.

A3: (BT): A burst type is specified. When full-page burst is performed, only "sequential" can be selected.

A2, A1, A0: (BL): These pins specify the burst length.



A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
OPCODE						0	LMODE			BT	BL		

A6	A5	A4	CAS Latency
0	0	0	R
0	0	1	R
0	1	0	2
0	1	1	3
1	X	X	R

A3	Burst Type
0	Sequential
1	Interleave

A2	A1	A0	Burst Length	
			BT=0	BT=1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	R	R
1	0	1	R	R
1	1	0	R	R
1	1	1	F.P.	R

A13	A12	A11	A10	A9	A8	Write mode
0	0	0	0	0	0	Burst read and burst write
X	X	X	X	0	1	R
X	X	X	X	1	0	Burst read and SINGLE WRITE
X	X	X	X	1	1	R

F.P. = Full Page (256: HM5264165)
(512: HM5264805)
(1024: HM5264405)
R is Reserved (inhibit)
X: 0 or 1

Burst Sequence

Burst length = 2

Starting Ad.	Addressing(decimal)	
A0	Sequence	Interleave
0	0, 1,	0, 1,
1	1, 0,	1, 0,

Burst length = 4

Starting Ad.		Addressing(decimal)	
A1	A0	Sequence	Interleave
0	0	0, 1, 2, 3,	0, 1, 2, 3,
0	1	1, 2, 3, 0,	1, 0, 3, 2,
1	0	2, 3, 0, 1,	2, 3, 0, 1,
1	1	3, 0, 1, 2,	3, 2, 1, 0,

Burst length = 8

Starting Ad.			Addressing(decimal)	
A2	A1	A0	Sequence	Interleave
0	0	0	0, 1, 2, 3, 4, 5, 6, 7,	0, 1, 2, 3, 4, 5, 6, 7,
0	0	1	1, 2, 3, 4, 5, 6, 7, 0,	1, 0, 3, 2, 5, 4, 7, 6,
0	1	0	2, 3, 4, 5, 6, 7, 0, 1,	2, 3, 0, 1, 6, 7, 4, 5,
0	1	1	3, 4, 5, 6, 7, 0, 1, 2,	3, 2, 1, 0, 7, 6, 5, 4,
1	0	0	4, 5, 6, 7, 0, 1, 2, 3,	4, 5, 6, 7, 0, 1, 2, 3,
1	0	1	5, 6, 7, 0, 1, 2, 3, 4,	5, 4, 7, 6, 1, 0, 3, 2,
1	1	0	6, 7, 0, 1, 2, 3, 4, 5,	6, 7, 4, 5, 2, 3, 0, 1,
1	1	1	7, 0, 1, 2, 3, 4, 5, 6,	7, 6, 5, 4, 3, 2, 1, 0,

Operation of HM5264165 Series, HM5264805 Series, HM5264405 Series

Read/Write Operations

Bank active: Before executing a read or write operation, the corresponding bank and the row address must be activated by the bank active (ACTV) command. Bank 0, bank 1, bank 2 or bank 3 is activated according to the status of the A12/A13 pin, and the row address (AX0 to AX11) is activated by the A0 to A11 pins at the bank active command cycle. An interval of t_{RCD} is required between the bank active command input and the following read/write command input.

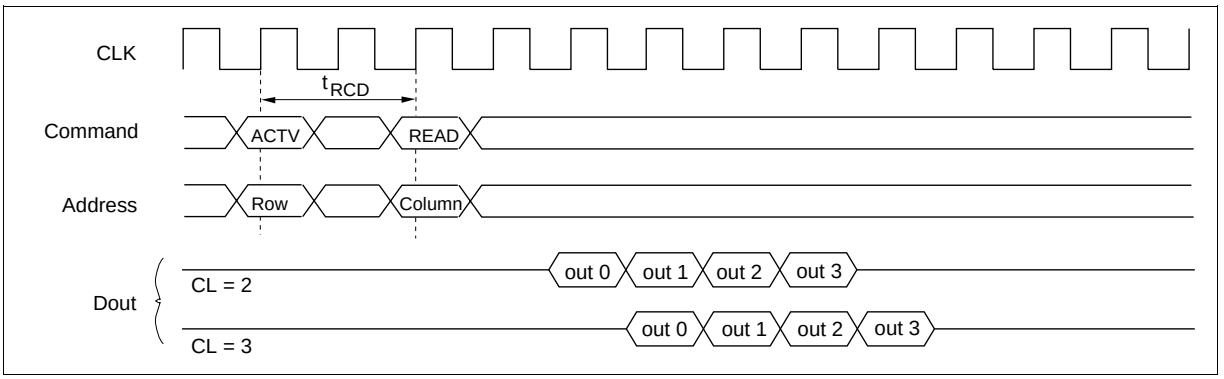
Read operation: A read operation starts when a read command is input. Output buffer becomes Low-Z in the ($\overline{CAS}$ Latency - 1) cycle after read command set. HM5264165 Series, HM5264805 series, HM5264405 Series can perform a burst read operation.

The burst length can be set to 1, 2, 4, 8 or full-page(256; HM5264165 Series, 512; HM5264805 Series, 1024; HM5264405 Series). The start address for a burst read is specified by the column address (AY0 to AY7; HM5264165 Series, AY0 to AY8; HM5264805 Series, AY0 to AY9; HM5264405 Series) and the bank select address (A12/A13) at the read command set cycle. In a read operation, data output starts after the number of cycles specified by the $\overline{CAS}$ Latency. The $\overline{CAS}$ Latency can be set to 2 or 3.

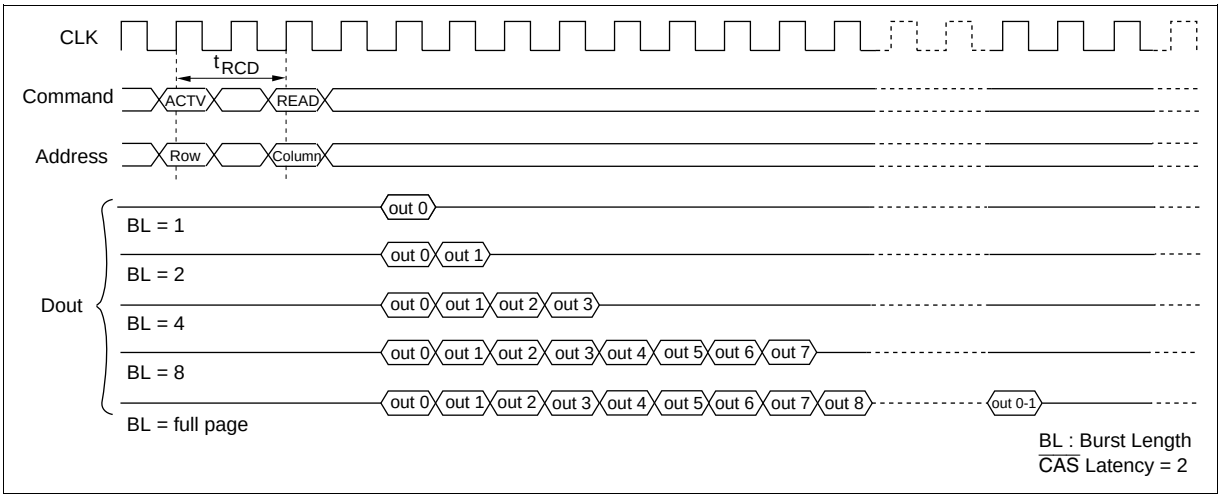
When the burst length is 1, 2, 4, 8, or full-page (256; HM5264165 Series, 512; HM5264805 Series, 1024; HM5264405 Series), the Dout buffer automatically becomes High-Z at the next cycle after the successive burst-length data has been output.

The $\overline{CAS}$ latency and burst length must be specified at the mode register.

$\overline{CAS}$ Latency

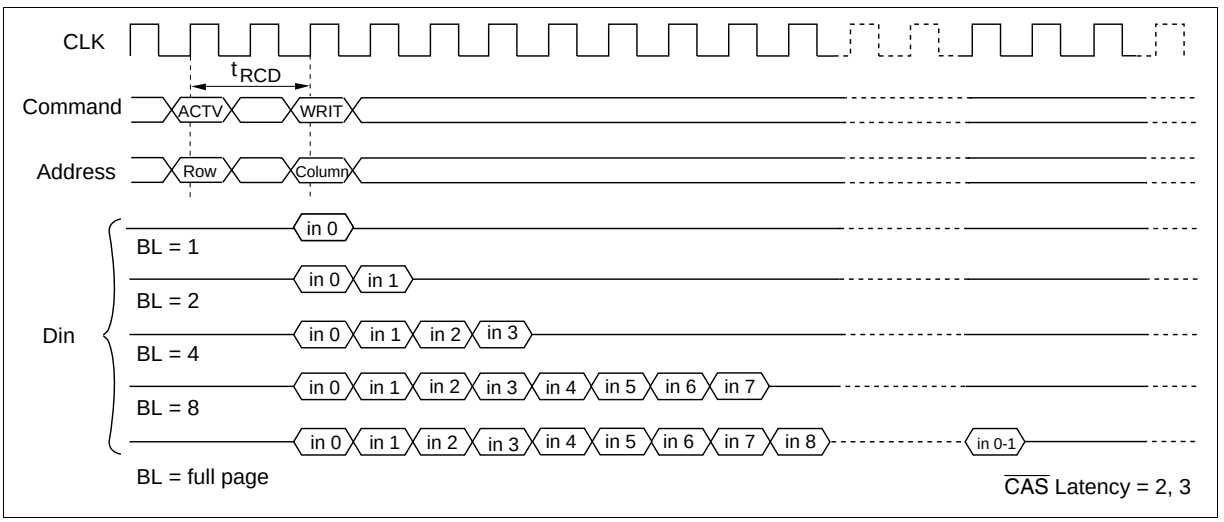


Burst Length

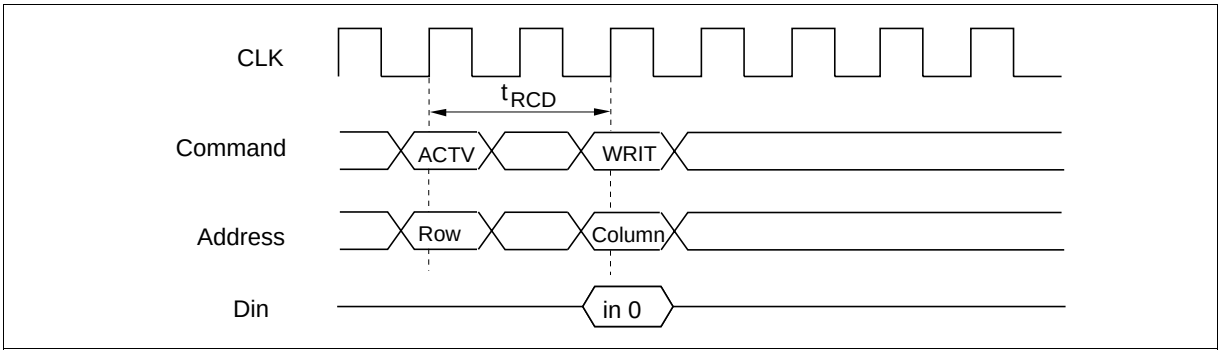


Write operation: Burst write or single write mode is selected by the OPCODE (A13, A12, A11, A10, A9, A8) of the mode register.

1. Burst write: A burst write operation is enabled by setting OPCODE (A9, A8) to (0, 0). A burst write starts in the same cycle as a write command set. (The latency of data input is 0.) The burst length can be set to 1, 2, 4, 8, and full-page, like burst read operations. The write start address is specified by the column address (AY0 to AY7; HM5264165 Series, AY0 to AY8; HM5264805 Series, AY0 to AY9; HM5264405 Series) and the bank select address (A12/A13) at the write command set cycle.

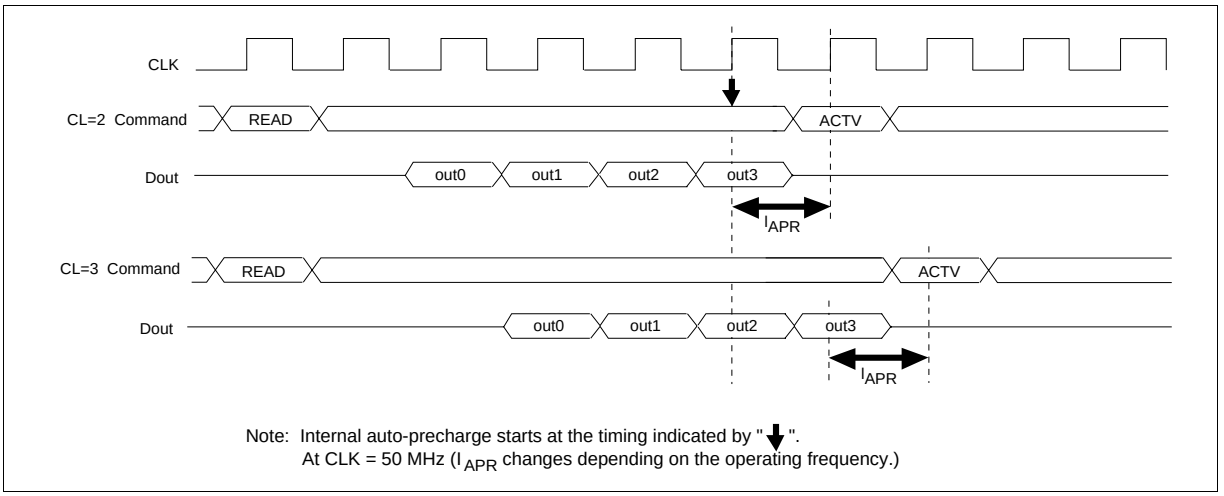


2. Single write: A single write operation is enabled by setting OPCODE (A9, A8) to (1, 0). In a single write operation, data is only written to the column address (AY0 to AY7; HM5264165 Series, AY0 to AY8; HM5264805 Series, AY0 to AY9; HM5264405 Series) and the bank select address (A12/A13) specified by the write command set cycle without regard to the burst length setting. (The latency of data input is 0).



Read with auto-precharge: In this operation, since precharge is automatically performed after completing a read operation, a precharge command need not be executed after each read operation. The command executed for the same bank after the execution of this command must be the bank active (ACTV) command. In addition, an interval defined by l_{APR} is required before execution of the next command.

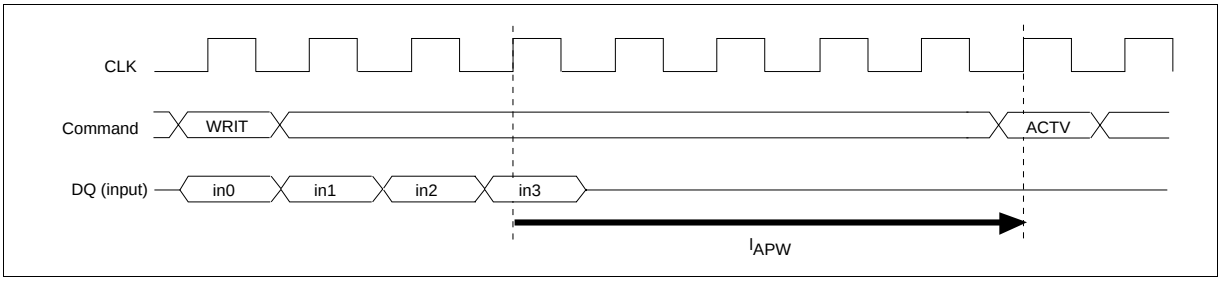
$\overline{\text{CAS}}$ latency	**Precharge start cycle**
3	2 cycle before the final data is output
2	1 cycle before the final data is output



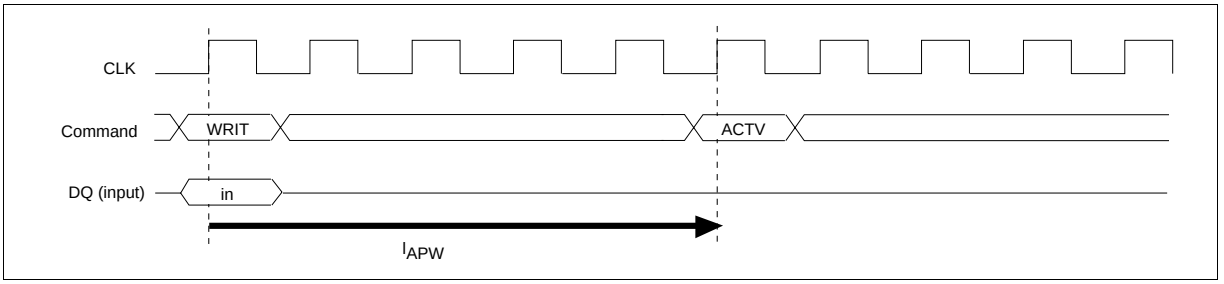
Note: Internal auto-precharge starts at the timing indicated by "↓".
At CLK = 50 MHz (l_{APR} changes depending on the operating frequency.)

Write with auto-precharge: In this operation, since precharge is automatically performed after completing a burst write or single write operation, a precharge command need not be executed after each write operation. The command executed for the same bank after active (ACTV) command. In addition, an interval of l_{APW} is required between the final valid data input and input of next command.

Burst Write (Burst Length = 4)



Single Write

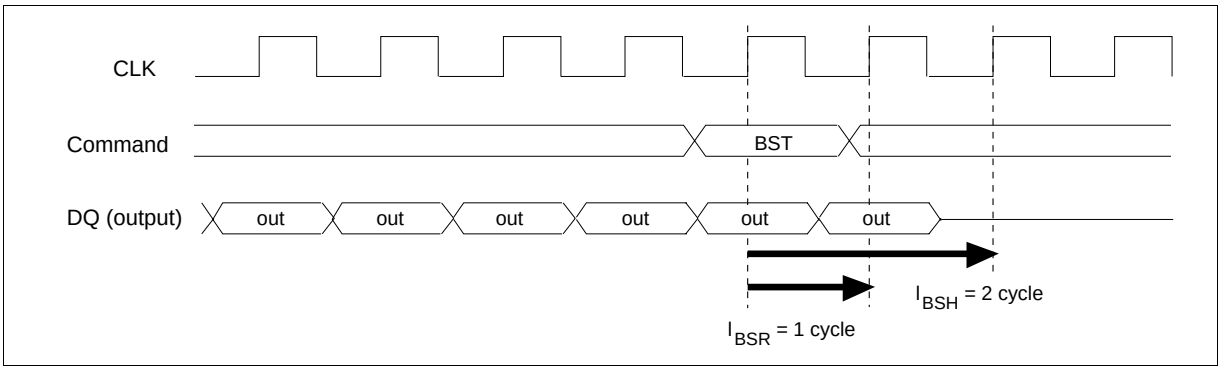


Full-page Burst Stop

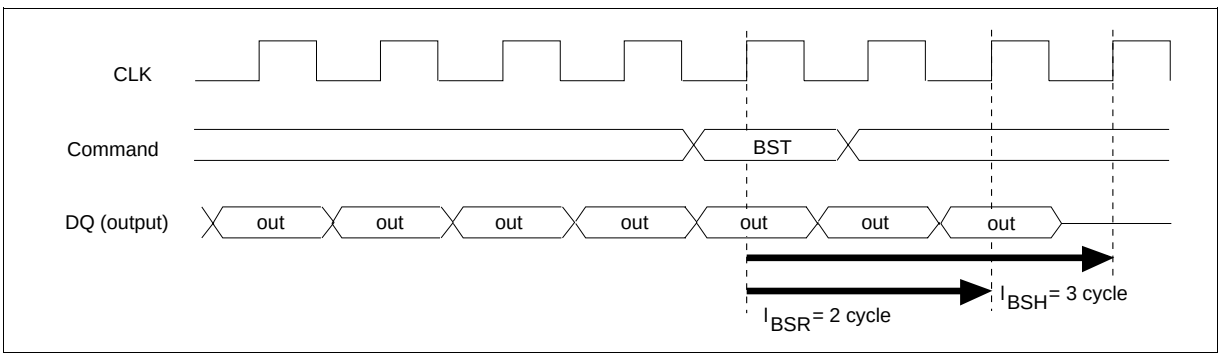
Burst stop command during burst read: The burst stop (BST) command is used to stop data output during a full-page burst. The BST command sets the output buffer to High-Z and stops the full-page burst read. The timing from command input to the last data changes depending on the $\overline{\text{CAS}}$ latency setting. In addition, the BST command is valid only during full-page burst mode, and is illegal with burst lengths 1, 2, 4 and 8.

$\overline{\text{CAS}}$ latency	BST to valid data	BST to high impedance
2	1	2
3	2	3

$\overline{\text{CAS}}$ Latency = 2, Burst Length = full page

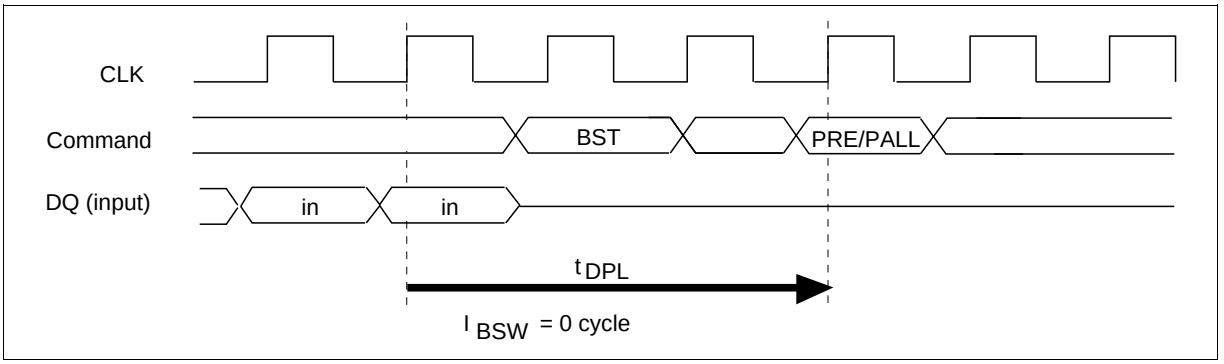


$\overline{\text{CAS}}$ Latency = 3, Burst Length = full page



Burst stop command at burst write: The burst stop command (BST command) is used to stop data input during a full-page burst write. No data is written in the same cycle as the BST command, and in subsequent cycles. In addition, the BST command is only valid during full-page burst mode, and is illegal with burst lengths of 1, 2, 4 and 8. And an interval of t_{DPL} is required between last data-in and the next precharge command.

Burst Length = full page

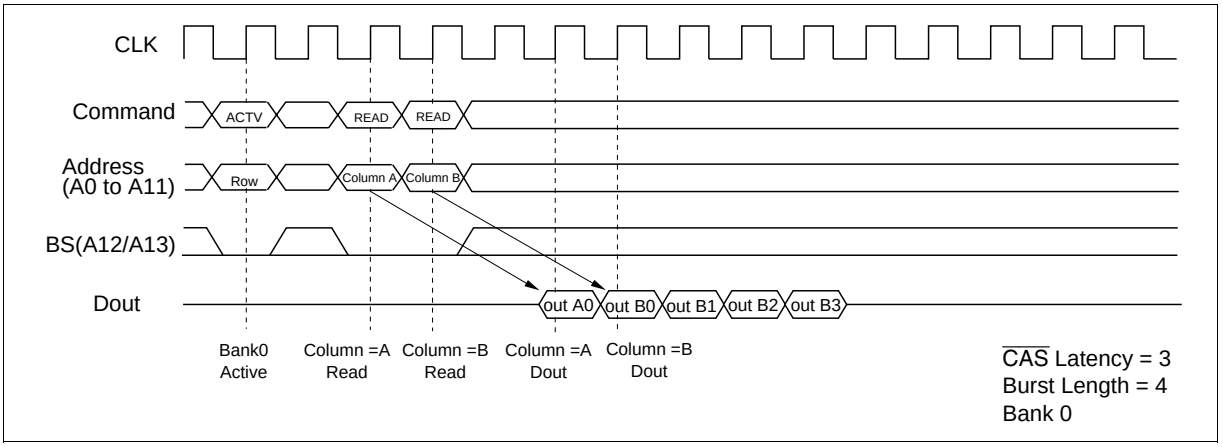


Command Intervals

Read command to Read command interval:

1. Same bank, same ROW address: When another read command is executed at the same ROW address of the same bank as the preceding read command execution, the second read can be performed after an interval of no less than 1 cycle. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.

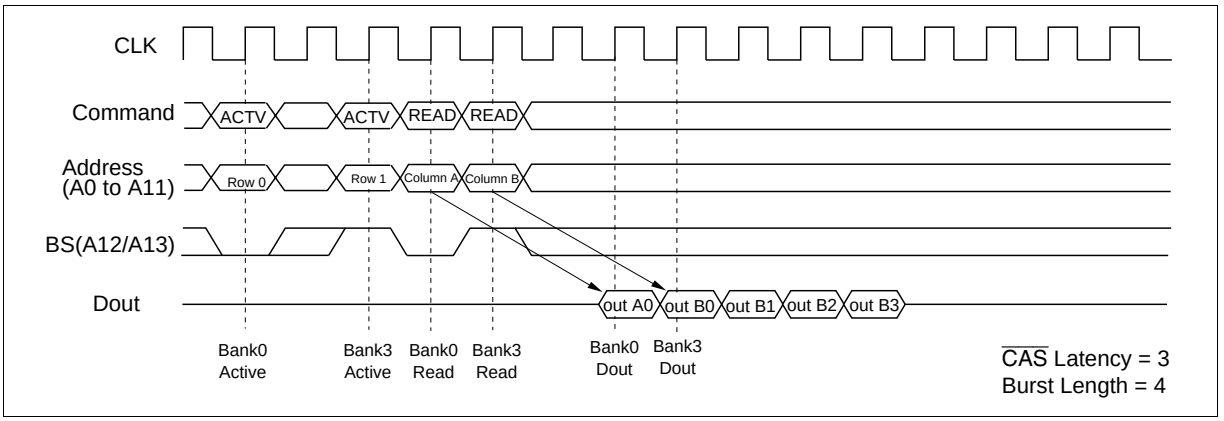
READ to READ Command Interval (same ROW address in same bank)



2. Same bank, different ROW address: When the ROW address changes on same bank, consecutive read commands cannot be executed; it is necessary to separate the two read commands with a precharge command and a bank-active command.

3. Different bank: When the bank changes, the second read can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.

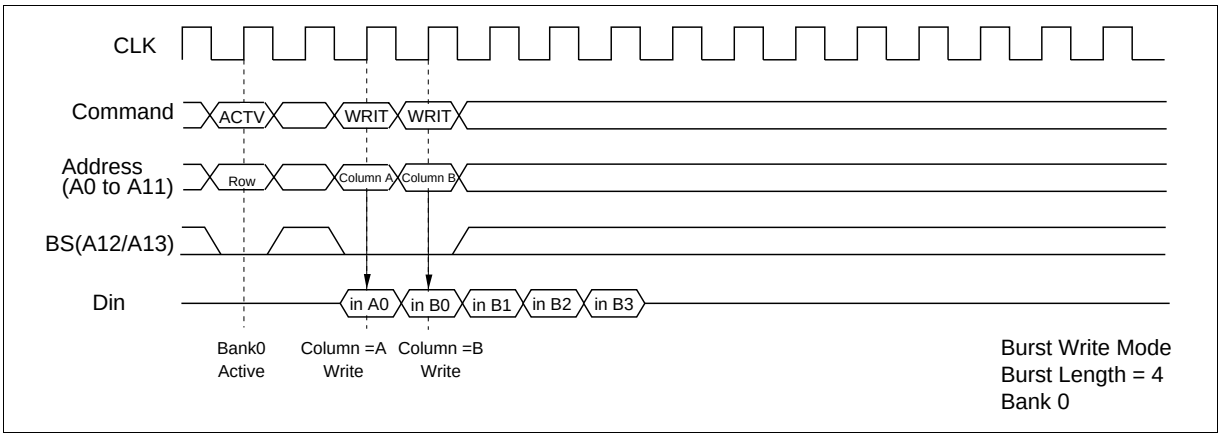
READ to READ Command Interval (different bank)



Write command to Write command interval:

1. Same bank, same ROW address: When another write command is executed at the same ROW address of the same bank as the preceding write command, the second write can be performed after an interval of no less than 1 cycle. In the case of burst writes, the second write command has priority.

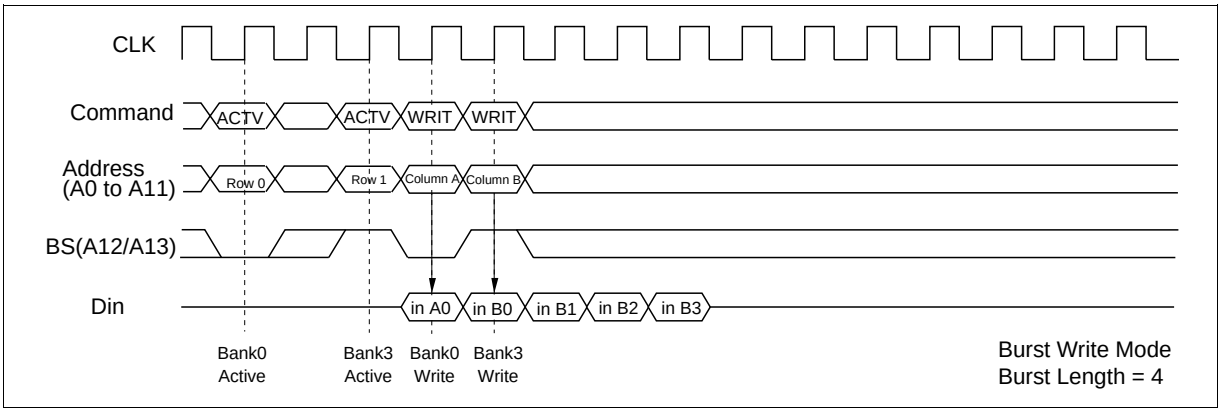
WRITE to WRITE Command Interval (same ROW address in same bank)



2. Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two write commands with a precharge command and a bank-active command.

3. Different bank: When the bank changes, the second write can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. In the case of burst write, the second write command has priority.

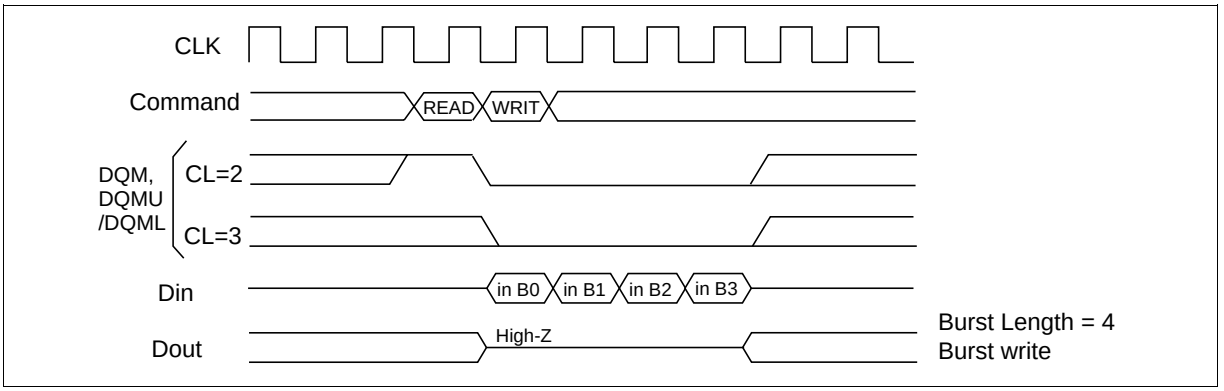
WRITE to WRITE Command Interval (different bank)



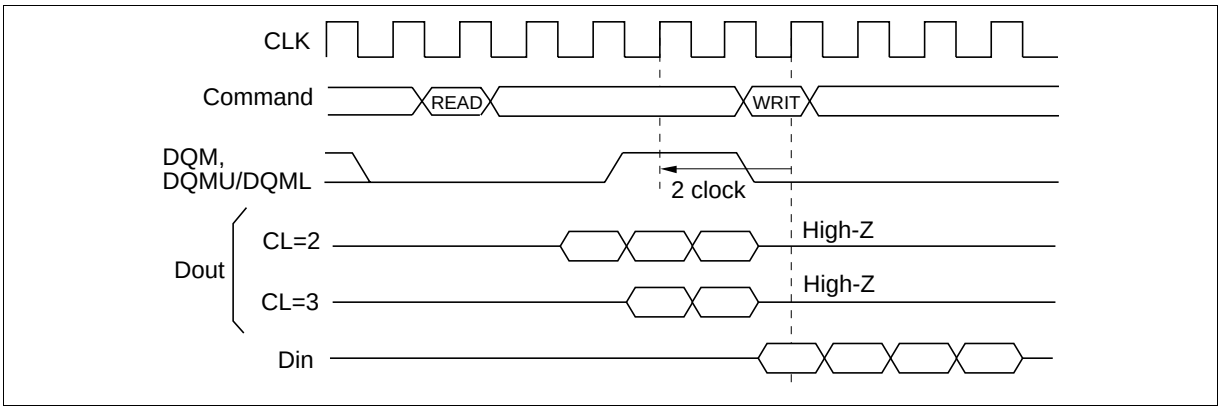
Read command to Write command interval:

1. Same bank, same ROW address: When the write command is executed at the same ROW address of the same bank as the preceding read command, the write command can be performed after an interval of no less than 1 cycle. However, DQM, DQMU/DQML must be set High so that the output buffer becomes High-Z before data input.

READ to WRITE Command Interval (1)



READ to WRITE Command Interval (2)



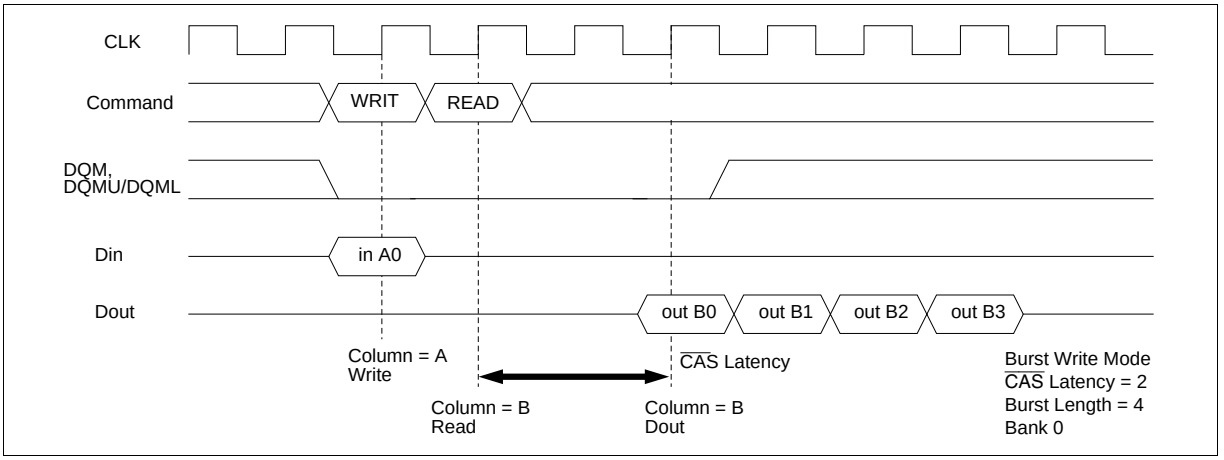
2. Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two commands with a precharge command and a bank-active command.

3. Different bank: When the bank changes, the write command can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. However, DQM, DQMU/DQML must be set High so that the output buffer becomes High-Z before data input.

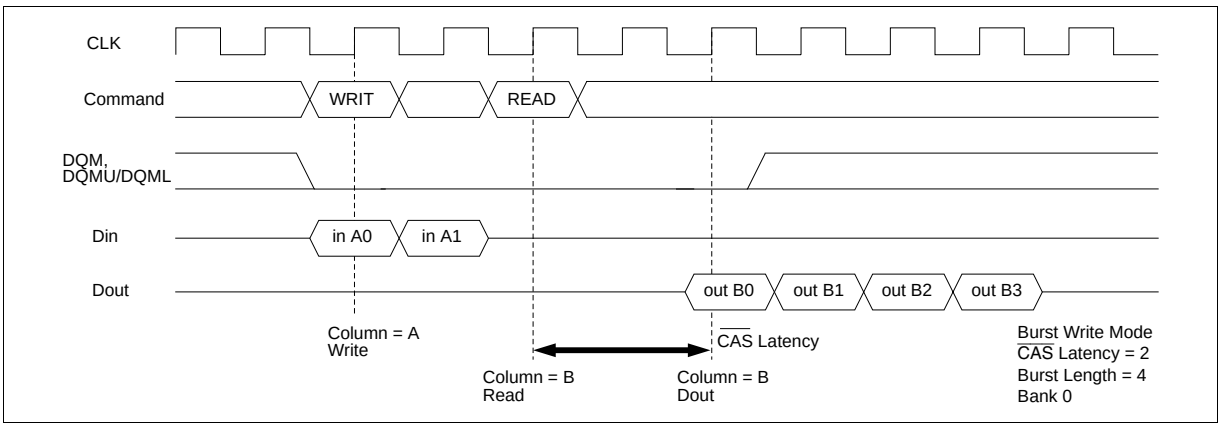
Write command to Read command interval:

1. Same bank, same ROW address: When the read command is executed at the same ROW address of the same bank as the preceding write command, the write command can be performed after an interval of no less than 1 cycle. However, in the case of a burst write, data will continue to be written until one cycle before the read command is executed.

WRITE to READ Command Interval (1)



WRITE to READ Command Interval (2)



2. Same bank, different ROW address: When the ROW address changes, consecutive read commands cannot be executed; it is necessary to separate the two commands with a precharge command and a bank-active command.

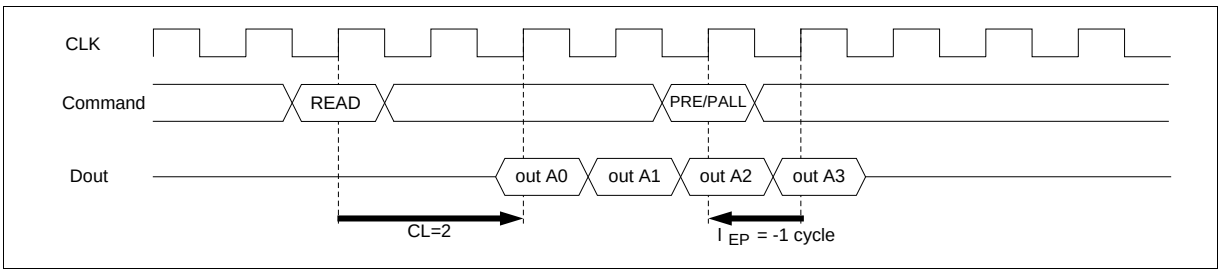
3. Different bank: When the bank changes, the read command can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. However, in the case of a burst write, data will continue to be written until one cycle before the read command is executed (as in the case of the same bank and the same address).

Read command to Precharge command interval (same bank):

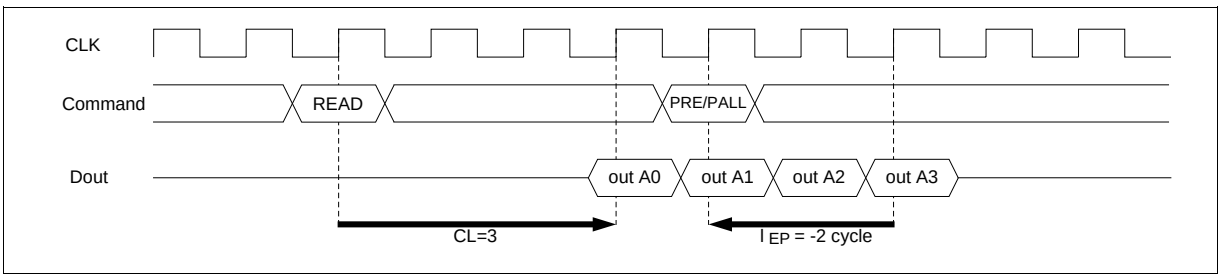
When the precharge command is executed for the same bank as the read command that preceded it, the minimum interval between the two commands is one cycle. However, since the output buffer then becomes High-Z after the cycles defined by l_{HZP}, there is a possibility that burst read data output will be interrupted, if the precharge command is input during burst read. To read all data by burst read, the cycles defined by l_{EP} must be assured as an interval from the final data output to precharge command execution.

READ to PRECHARGE Command Interval (same bank): To output all data

$\overline{\text{CAS}}$ Latency = 2, Burst Length = 4

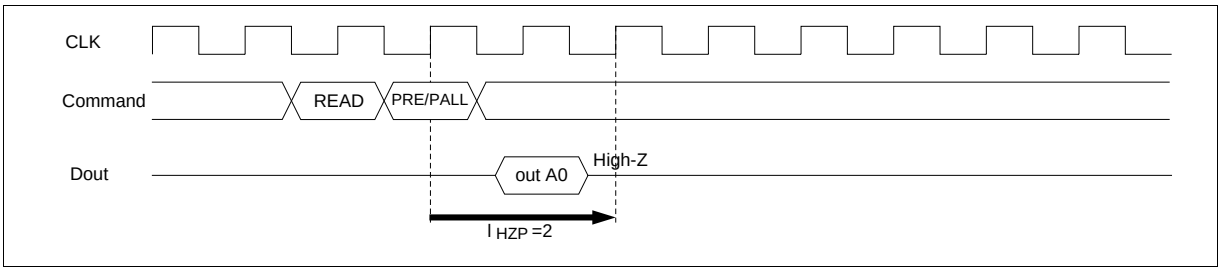


$\overline{\text{CAS}}$ Latency = 3, Burst Length = 4

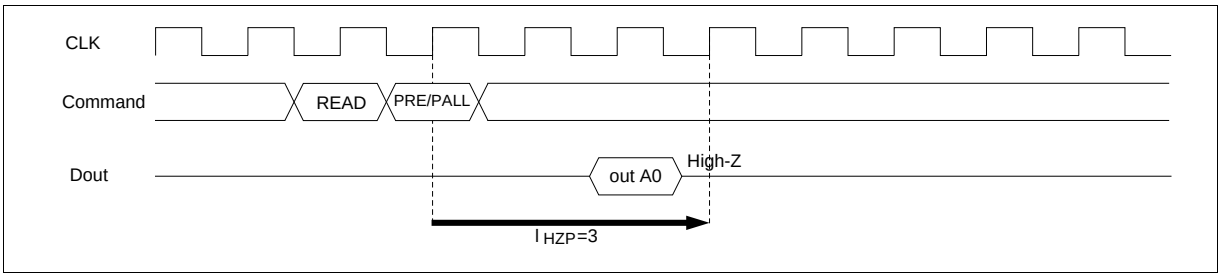


READ to PRECHARGE Command Interval (same bank): To stop output data

$\overline{\text{CAS}}$ Latency = 2, Burst Length = 1, 2, 4, 8



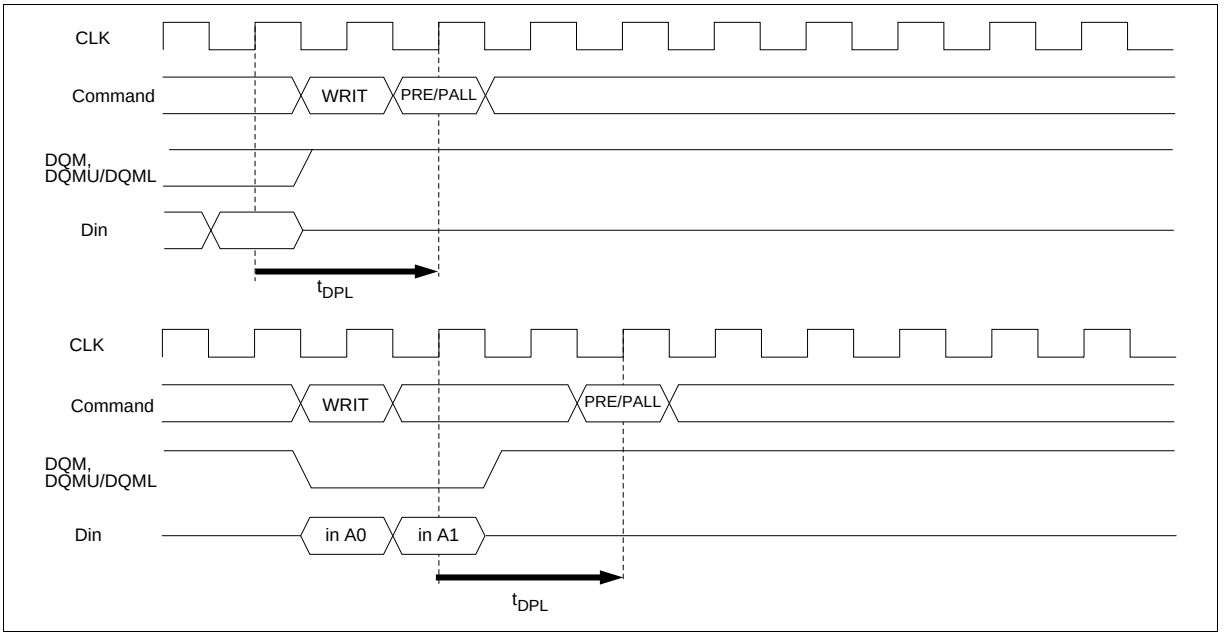
$\overline{\text{CAS}}$ Latency = 3, Burst Length = 1, 2, 4, 8



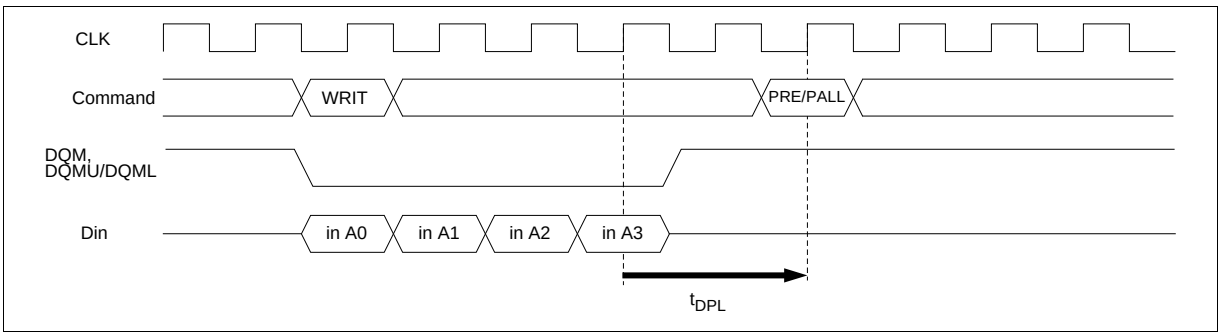
Write command to Precharge command interval (same bank): When the precharge command is executed for the same bank as the write command that preceded it, the minimum interval between the two commands is 1 cycle. However, if the burst write operation is unfinished, the input data must be masked by means of DQM, DQMU/DQML for assurance of the cycle defined by t_{DPL}.

WRITE to PRECHARGE Command Interval (same bank)

Burst Length = 4 (To stop write operation)



Burst Length = 4 (To write all data)

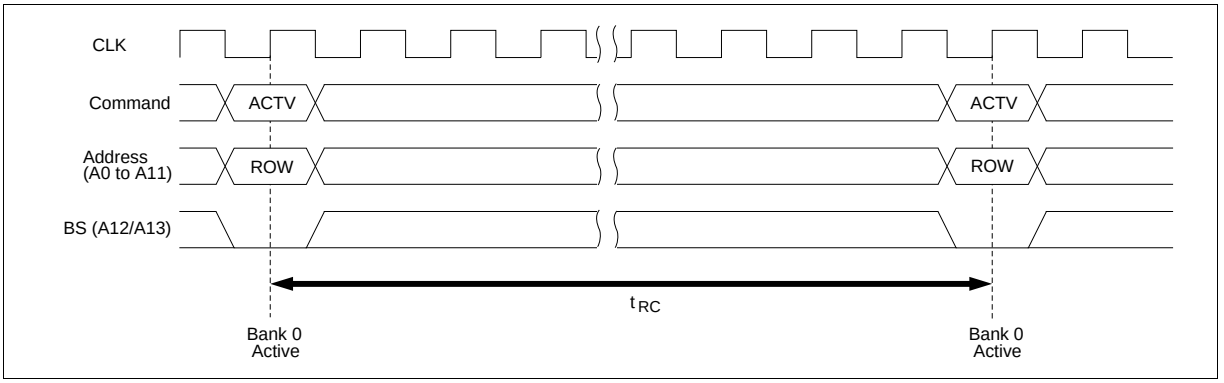


Bank active command interval:

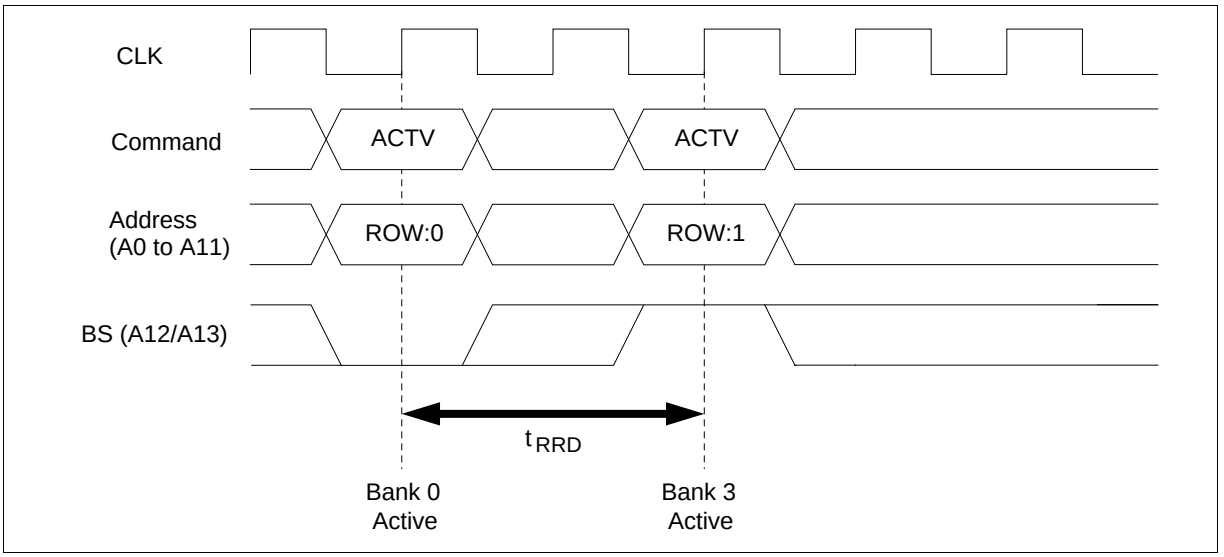
1. Same bank: The interval between the two bank-active commands must be no less than t_{RC}.

2. In the case of different bank-active commands: The interval between the two bank-active commands must be no less than t_{RRD}.

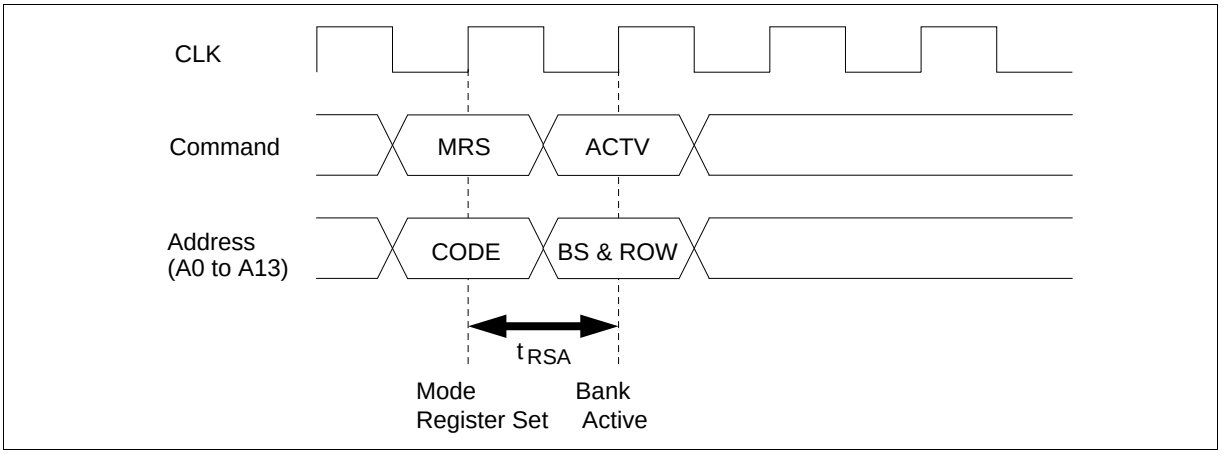
Bank Active to Bank Active for Same Bank



Bank Active to Bank Active for Different Bank



Mode register set to Bank-active command interval: The interval between setting the mode register and executing a bank-active command must be no less than t_{RSA}.



DQM Control (HM5264165 Series)

The DQMU and DQML mask the lower and upper bytes of the DQ data, respectively. The timing of DQMU/DQML is different during reading and writing.

Reading: When data is read, the output buffer can be controlled by DQMU/DQML. By setting DQMU/DQML to Low, the output buffer becomes Low-Z, enabling data output. By setting DQMU/DQML to High, the output buffer becomes High-Z, and the corresponding data is not output. However, internal reading operations continue. The latency of DQMU/DQML during reading is 2.

Writing: Input data can be masked by DQMU/DQML. By setting DQMU/DQML to Low, data can be written. In addition, when DQMU/DQML is set to High, the corresponding data is not written, and the previous data is held. The latency of DQMU/DQML during writing is 0.

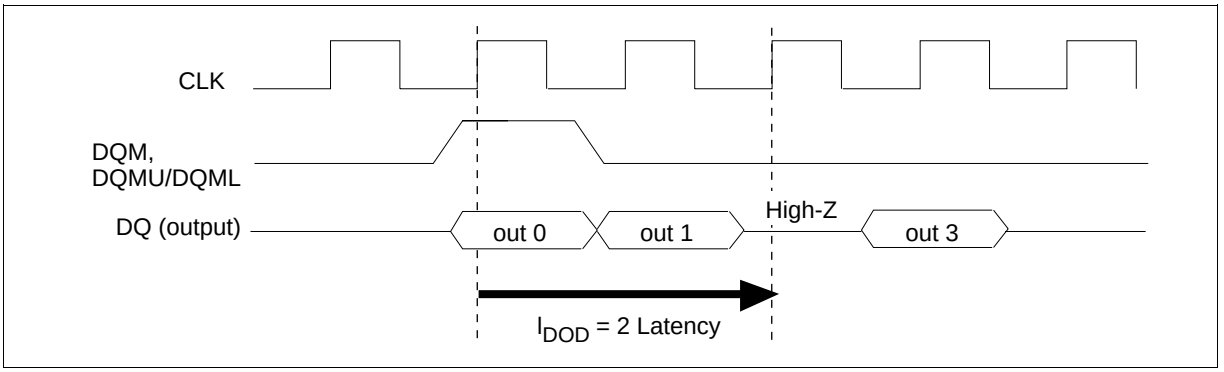
DQM Control (HM5264805 Series, HM5264405 Series)

The DQM mask the lower and upper bytes of the DQ data, respectively. The timing of DQM is different during reading and writing.

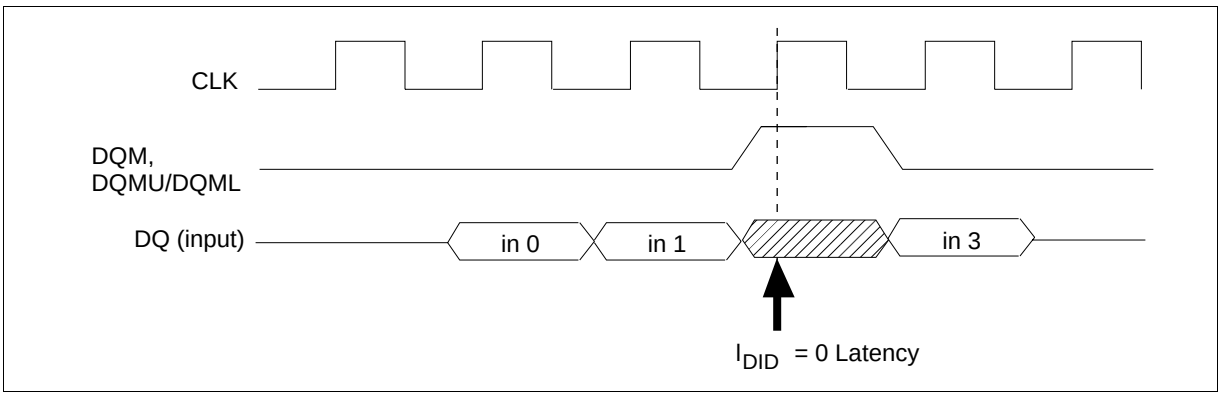
Reading: When data is read, the output buffer can be controlled by DQM. By setting DQM to Low, the output buffer becomes Low-Z, enabling data output. By setting DQM to High, the output buffer becomes High-Z, and the corresponding data is not output. However, internal reading operations continue. The latency of DQM during reading is 2.

Writing: Input data can be masked by DQM. By setting DQM to Low, data can be written. In addition, when DQM is set to High, the corresponding data is not written, and the previous data is held. The latency of DQM during writing is 0.

Reading



Writing



Refresh

Auto-refresh: All the banks must be precharged before executing an auto-refresh command. Since the auto-refresh command updates the internal counter every time it is executed and determines the banks and the ROW addresses to be refreshed, external address specification is not required. The refresh cycle is 4096 cycles/64 ms. (4096 cycles are required to refresh all the ROW addresses.) The output buffer becomes High-Z after auto-refresh start. In addition, since a precharge has been completed by an internal operation after the auto-refresh, an additional precharge operation by the precharge command is not required.

Self-refresh: After executing a self-refresh command, the self-refresh operation continues while CKE is held Low. During self-refresh operation, all ROW addresses are refreshed by the internal refresh timer. A self-refresh is terminated by a self-refresh exit command. If you use distributed auto-refresh mode with 15.6 µs interval in normal read/write cycle, auto-refresh should be executed within 15.6 µs immediately after exiting from and before entering into self refresh mode. If you use address refresh or burst auto-refresh mode in normal read/write cycle, 4096 cycles of distributed auto-refresh with 15.6 µs interval should be executed within 64 ms immediately after exiting from and before entering into self refresh mode.

Others

Power-down mode: The synchronous DRAM enters power-down mode when CKE goes Low in the IDLE state. In power down mode, power consumption is suppressed by deactivating the input initial circuit. Power down mode continues while CKE is held Low. In addition, by setting CKE to High, the synchronous DRAM exits from the power down mode, and command input is enabled from the next cycle. In this mode, internal refresh is not performed.

Clock suspend mode: By driving CKE to Low during a bank-active or read/write operation, the synchronous DRAM enters clock suspend mode. During clock suspend mode, external input signals are ignored and the internal state is maintained. When CKE is driven High, the synchronous DRAM terminates clock suspend mode, and command input is enabled from the next cycle. For details, refer to the "CKE Truth Table".

Power-up sequence: During power-up sequence, the DQM and the CKE must be set to High. When 200 µs has past after power on, all banks must be precharged using the precharge command. After t_{RP} delay, set 8 or more auto refresh commands. And set the mode register set command to initialize the mode register.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{SS}	V_T	–1.0 to +4.6	V	1
Supply voltage relative to V_{SS}	V_{CC}	–1.0 to +4.6	V	1
Short circuit output current	Iout	50	mA	
Power dissipation	P_T	1.0	W	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	–55 to +125	°C	

Note: 1. Respect to V_{SS}

Recommended DC Operating Conditions (Ta = 0 to +70˚C)

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage	V_{CC}, $V_{CC}Q$	3.0	3.6	V	1
	V_{SS}, $V_{SS}Q$	0	0	V	
Input high voltage	V_{IH}	2.0	V_{CC} + 0.3	V	1, 2, 3
Input low voltage	V_{IL}	–0.3	0.8	V	1, 4

Notes: 1. All voltage referred to V_{SS}
2. V_{IH} (max) = V_{CC} + 0.5 V for pulse width ≤ 5 ns at V_{CC}. (DQ pins).
3. V_{IH} (max) = 4.6 V for pulse width ≤ 5 ns at V_{CC}. (Others).
4. V_{IL} (min) = –1.0 V for pulse width ≤ 5 ns at V_{SS}.

DC Characteristics (Ta = 0 to 70°C, V_{CC}, $V_{CC}Q$ = 3.3 V ± 0.3 V, V_{SS}, $V_{SS}Q$ = 0 V)

		HM5264165/HM5264805								
		-10		-12		-15				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
Operating current	I_{CC1}	—	130	—	105	—	85	mA	Burst length = 1 t_{RC} = min	1, 2, 4
Standby current	I_{CC2}	—	3	—	3	—	3	mA	CKE = V_{IL}, t_{CK} = min	5
(Bank Disable)		—	2	—	2	—	2	mA	CLK = V_{IL} or V_{IH} Fixed	6
		—	50	—	45	—	35	mA	CKE = V_{IH}, NOP command t_{CK} = min	3
Active standby current (Bank active)	I_{CC3}	—	12	—	12	—	12	mA	CKE = V_{IL}, t_{CK} = min DQ = High-Z	1, 2
		—	55	—	50	—	40	mA	CKE = V_{IH}, NOP command t_{CK} = min, DQ = High-Z	1, 2, 9
Burst operating current										
($\overline{CAS}$ Latency = 2)	I_{CC4}	—	150	—	130	—	100	mA	t_{CK} = min, BL = 8	1, 2, 8
($\overline{CAS}$ Latency = 3)	I_{CC4}	—	200	—	180	—	140	mA		
Refresh current	I_{CC5}	—	150	—	125	—	100	mA	t_{RC} = min, Address = V_{IL} or V_{IH} Fixed	
Self refresh current	I_{CC6}	—	3	—	3	—	3	mA	$V_{IH} \geq V_{CC} - 0.2$ $V_{IL} \leq 0.2$ V	7
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	$0 \leq Vin \leq V_{CC}$	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	$0 \leq Vout \leq V_{CC}$ DQ = disable	
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	V	I_{OH} = –2 mA	
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	V	I_{OL} = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CLK cycles.
4. Input signal transition is once per one CLK cycle.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.
8. Input signal transition is once per CLK eight cycles.
9. Input signal transition is once per CLK four cycles.

DC Characteristics (Ta = 0 to 70˚C, V_{CC}, $V_{CC}Q$ = 3.3 V ± 0.3 V, V_{SS}, $V_{SS}Q$ = 0 V)

		HM5264405								
		-10		-12		-15				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	110	—	95	—	75	mA	Burst length = 1 t_{RC} = min	1, 2, 4
Standby current	I_{CC2}	—	3	—	3	—	3	mA	CKE = V_{IL}, t_{CK} = min	5
(Bank Disable)		—	2	—	2	—	2	mA	CLK = V_{IL} or V_{IH} Fixed	6
		—	40	—	35	—	30	mA	CKE = V_{IH}, NOP command t_{CK} = min	3
Active standby current (Bank active)	I_{CC3}	—	12	—	12	—	12	mA	CKE = V_{IL}, t_{CK} = min DQ = High-Z	1, 2
		—	45	—	40	—	35	mA	CKE = V_{IH}, NOP command t_{CK} = min, DQ = High-Z	1, 2, 9
Burst operating current										
($\overline{CAS}$ Latency = 2)	I_{CC4}	—	140	—	120	—	95	mA	t_{CK} = min, BL = 8	1, 2, 8
($\overline{CAS}$ Latency = 3)	I_{CC4}	—	190	—	170	—	135	mA		
Refresh current	I_{CC5}	—	150	—	125	—	100	mA	t_{RC} = min, Address = V_{IL} or V_{IH} Fixed	
Self refresh current	I_{CC6}	—	3	—	3	—	3	mA	$V_{IH} \geq V_{CC} - 0.2$ $V_{IL} \leq 0.2$ V	7
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	$0 \leq Vin \leq V_{CC}$	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	$0 \leq Vout \leq V_{CC}$ DQ = disable	
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	V	I_{OH} = –2 mA	
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	V	I_{OL} = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CLK cycles.
4. Input signal transition is once per one CLK cycle.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.
8. Input signal transition is once per eight CLK cycles.
9. Input signal transition is once per four CLK cycles.

Capacitance (Ta = 25°C, V_{CC}, $V_{CC}Q$ = 3.3 V ± 0.3 V)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1, 3
Input capacitance (Signals)	C_{I2}	—	5	pF	1, 3
Output capacitance (DQ)	C_O	—	7	pF	1, 2, 3

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQM, DQMU/DQML = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70°C, V_{CC}, $V_{CC}Q$ = 3.3 V ± 0.3 V, V_{SS}, $V_{SS}Q$ = 0 V)

		HM5264165/HM5264805/HM5264405							
		-10		-12		-15			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
System clock cycle time									
($\overline{CAS}$ Latency = 2)	t_{CK}	15	—	18	—	22.5	—	ns	1
($\overline{CAS}$ Latency = 3)	t_{CK}	10	—	12	—	15	—	ns	
CLK high pulse width	t_{CKH}	3	—	4	—	5	—	ns	1
CLK low pulse width	t_{CKL}	3	—	4	—	5	—	ns	1
Access time from CLK									
($\overline{CAS}$ Latency = 2)	t_{AC}	—	9	—	13	—	15	ns	1, 2
($\overline{CAS}$ Latency = 3)	t_{AC}	—	8	—	10	—	12	ns	
Data-out hold time	t_{OH}	3	—	3	—	3	—	ns	1, 2
CLK to Data-out low impedance	t_{LZ}	2	—	2	—	2	—	ns	1, 2, 3
CLK to Data-out high impedance									
($\overline{CAS}$ Latency = 2, 3)	t_{HZ}	—	7	—	9	—	11	ns	1, 4
Data-in setup time	t_{DS}	2	—	3	—	3	—	ns	1
Data in hold time	t_{DH}	1	—	1	—	1	—	ns	1
Address setup time	t_{AS}	2	—	3	—	3	—	ns	1
Address hold time	t_{AH}	1	—	1	—	1	—	ns	1
CKE setup time	t_{CES}	2	—	3	—	3	—	ns	1, 5

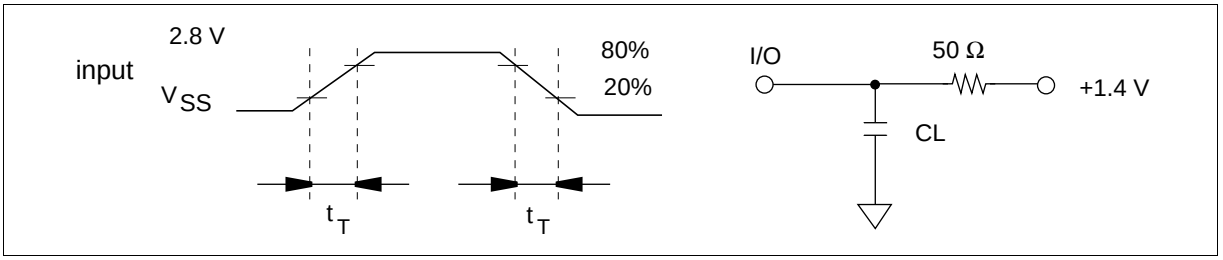
AC Characteristics (Ta = 0 to 70°C, V_{CC}, $V_{CC}Q$ = 3.3 V ± 0.3 V, V_{SS}, $V_{SS}Q$ = 0 V)

		HM5264165/HM5264805/HM5264405							
		-10		-12		-15			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
CKE setup time for power down exit	t_{CESP}	2	—	3	—	3	—	ns	1
CKE hold time	t_{CEH}	1	—	1	—	1	—	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time	t_{CS}	2	—	3	—	3	—	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time	t_{CH}	1	—	1	—	1	—	ns	1
Ref/Active to Ref/Active command period	t_{RC}	90	—	108	—	135	—	ns	1
Active to Precharge command period	t_{RAS}	60	120000	72	120000	90	120000	ns	1
Active command to column command (same bank)	t_{RCD}	30	—	36	—	45	—	ns	1
Precharge to active command period	t_{RP}	30	—	36	—	45	—	ns	1
Write recovery or data-in to precharge lead time	t_{DPL}	15	—	18	—	22.5	—	ns	1
Active (a) to Active (b) command period	t_{RRD}	20	—	24	—	30	—	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	1	5	ns	
Refresh period	t_{REF}	—	64	—	64	—	64	ms	

Notes: 1. AC measurement assumes t_T = 1 ns. Reference level for timing of input signals is 1.40 V.
2. Access time is measured at 1.40 V. Load condition is CL = 50 pF with current source.
3. t_{LZ} (max) defines the time at which the outputs achieves the low impedance state.
4. t_{HZ} (max) defines the time at which the outputs achieves the high impedance state.
5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

Test Conditions

- Input and output timing reference levels: 1.4 V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency

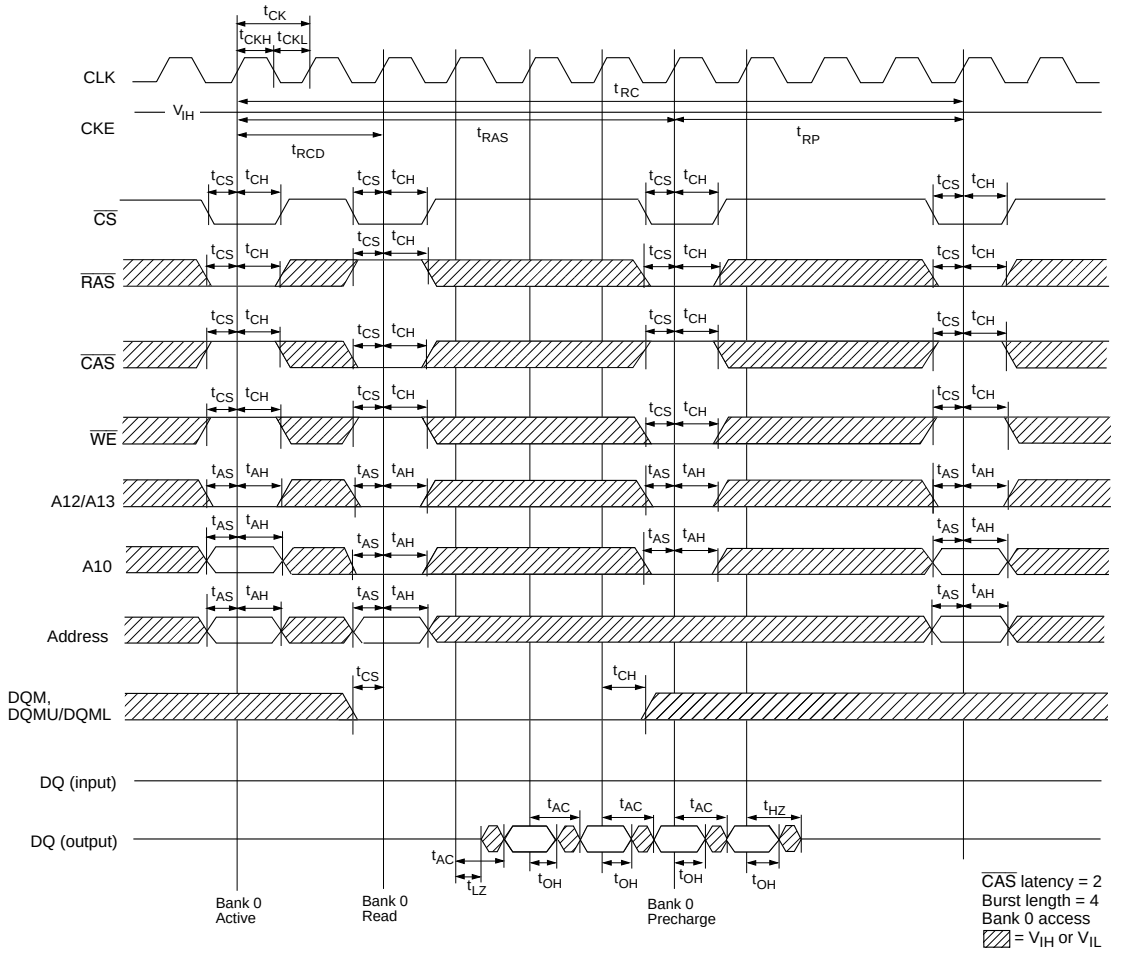
Parameter		HM5264165/HM5264805/HM5264405									
		-10			-12			-15			
Frequency (MHz)		100	66	33	83	55	28	66	44	22	
t_{CK} (ns)	Symbol	10	15	30	12	18	36	15	22.5	45	Notes
Active command to column command (same bank)	I_{RCD}	3	2	1	3	2	1	3	2	1	1
Active command to active command (same bank)	I_{RC}	9	6	3	9	6	3	9	6	3	= [I_{RAS}+ I_{RP}] 1
Active command to precharge command (same bank)	I_{RAS}	6	4	2	6	4	2	6	4	2	1
Precharge command to active command (same bank)	I_{RP}	3	2	1	3	2	1	3	2	1	1
Write recovery or data-in to precharge command (same bank)	I_{DPL}	2	1	1	2	1	1	2	1	1	1
Active command to active command (different bank)	I_{RRD}	2	2	1	2	2	1	2	2	1	1
Self refresh exit time	I_{SREX}	2	2	2	2	2	2	2	2	2	2
Last data in to active command (Auto precharge, same bank)	I_{APW}	5	3	2	5	3	2	5	3	2	= [I_{DPL} + I_{RP}]
Self refresh exit to command input	I_{SEC}	9	6	3	9	6	3	9	6	3	= [I_{RC}]

Parameter		HM5264165/HM5264805/HM5264405									
		-10			-12			-15			
Frequency (MHz)		100	66	33	83	55	28	66	44	22	
t_{CK} (ns)	Symbol	10	15	30	12	18	36	15	22.5	45	Notes
Precharge command to high impedance											
($\overline{CAS}$ latency = 2)	I_{HZP}	—	2	2	—	2	2	—	2	2	
($\overline{CAS}$ latency = 3)	I_{HZP}	3	3	3	3	3	3	3	3	3	
Last data out to active command (auto precharge) (same bank)	I_{APR}	1	1	1	1	1	1	1	1	1	
Last data out to precharge (early precharge)											
($\overline{CAS}$ latency = 2)	I_{EP}	—	–1	–1	—	–1	–1	—	–1	–1	
($\overline{CAS}$ latency = 3)	I_{EP}	–2	–2	–2	–2	–2	–2	–2	–2	–2	
Column command to column command	I_{CCD}	1	1	1	1	1	1	1	1	1	
Write command to data in latency	I_{WCD}	0	0	0	0	0	0	0	0	0	
DQM to data in	I_{DID}	0	0	0	0	0	0	0	0	0	
DQM to data out	I_{DOD}	2	2	2	2	2	2	2	2	2	
CKE to CLK disable	I_{CLE}	1	1	1	1	1	1	1	1	1	
Register set to active command	I_{RSA}	1	1	1	1	1	1	1	1	1	
$\overline{CS}$ to command disable	I_{CDD}	0	0	0	0	0	0	0	0	0	
Power down exit to command input	I_{PEC}	1	1	1	1	1	1	1	1	1	
Burst stop to output valid data hold											
($\overline{CAS}$ latency = 2)	I_{BSR}	—	1	1	—	1	1	—	1	1	
($\overline{CAS}$ latency = 3)	I_{BSR}	2	2	2	2	2	2	2	2	2	
Burst stop to output high impedance											
($\overline{CAS}$ latency = 2)	I_{BSH}	—	2	2	—	2	2	—	2	2	
($\overline{CAS}$ latency = 3)	I_{BSH}	3	3	3	3	3	3	3	3	3	
Burst stop to write data ignore	I_{BSW}	0	0	0	0	0	0	0	0	0	

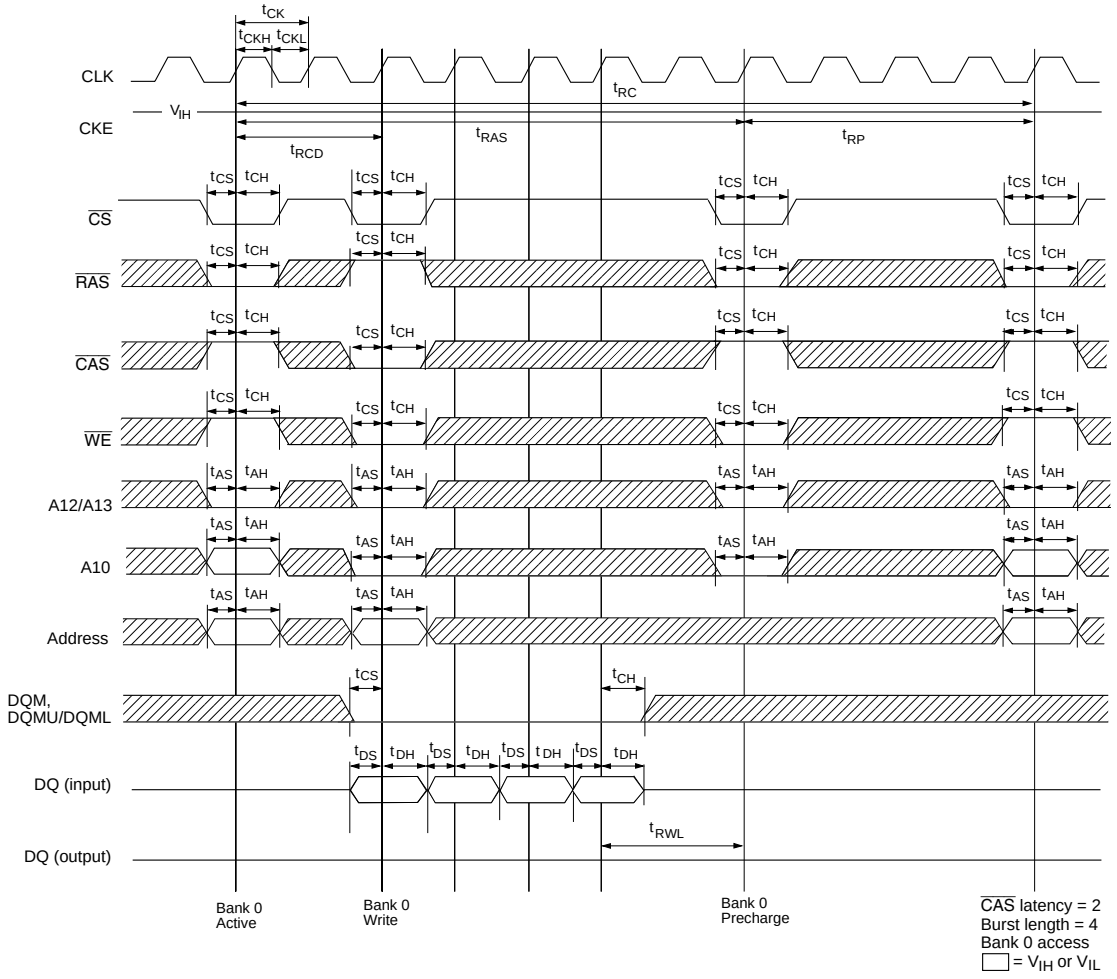
Notes: 1. I_{RCD} to I_{RRD} are recommended value.
2. 2 clock is required between self refresh exit time and next refresh or active command.

Timing Waveforms

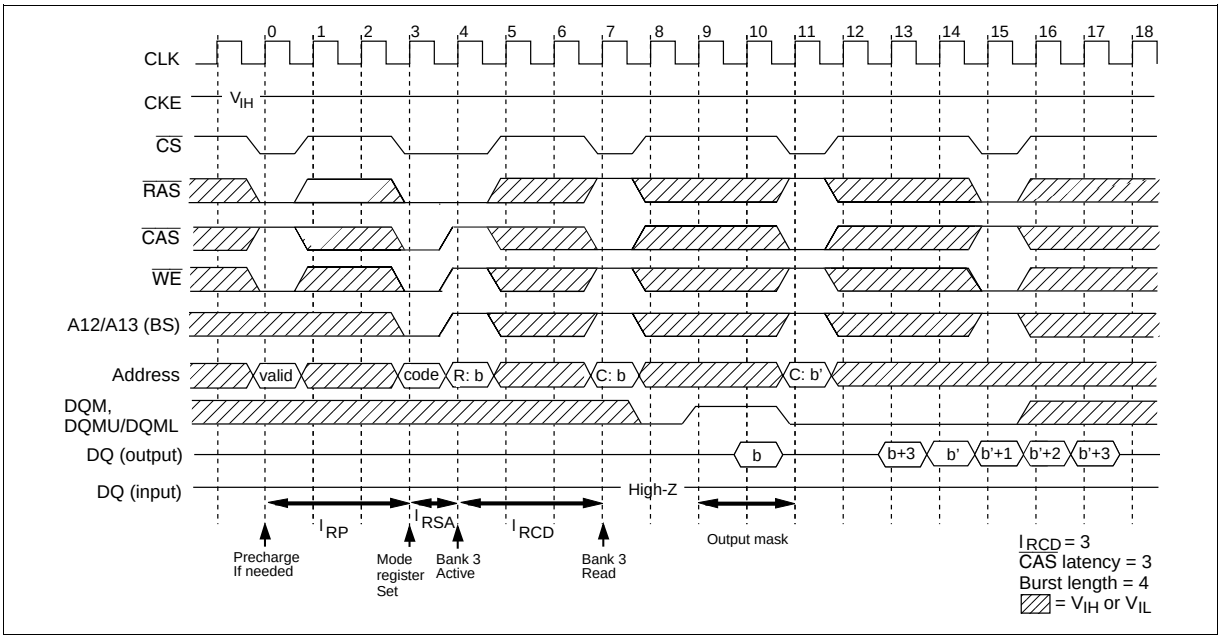
Read Cycle



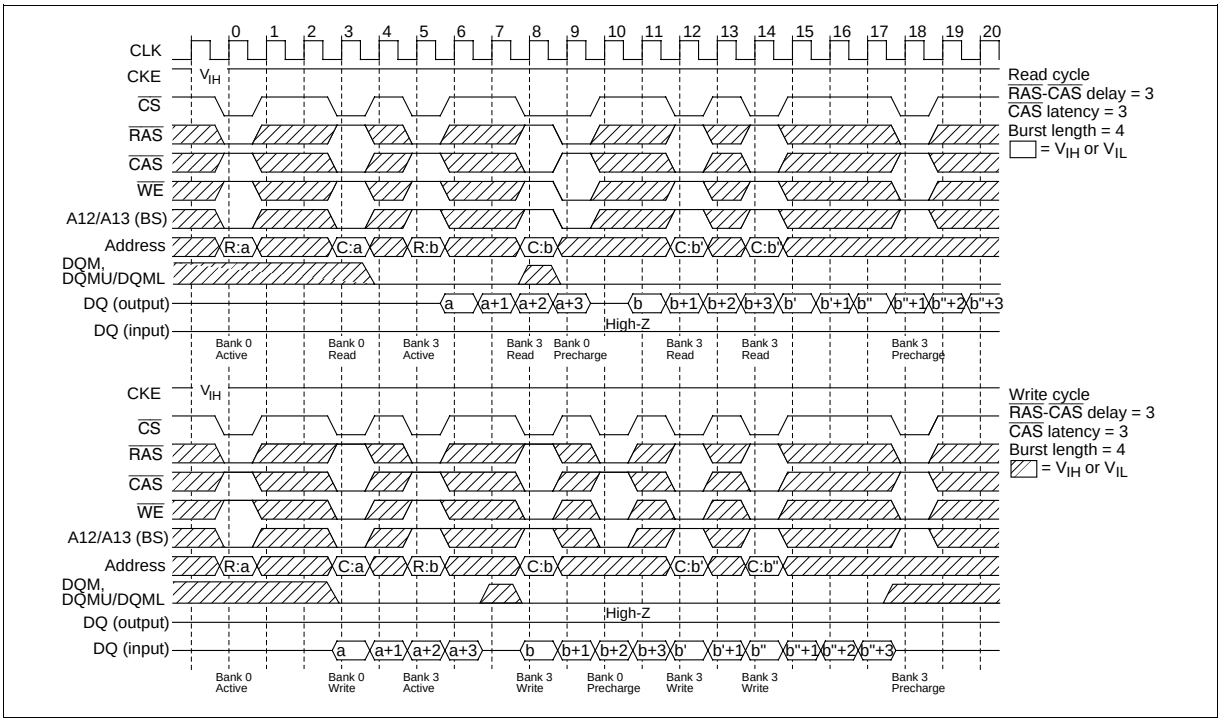
Write Cycle


tCK
tCKH tCKL
CLK
tRC
VIH
CKE
tRAS
tRP
tRCD
tCS tCH
CS
RAS
CAS
WE
tAS tAH
A12/A13
A10
Address
DQM,
DQMU/DQML
tDS tDH
DQ (input)
tRWL
DQ (output)
Bank 0
Active
Bank 0
Write
Bank 0
Precharge
CAS latency = 2
Burst length = 4
Bank 0 access
= VIH or VIL

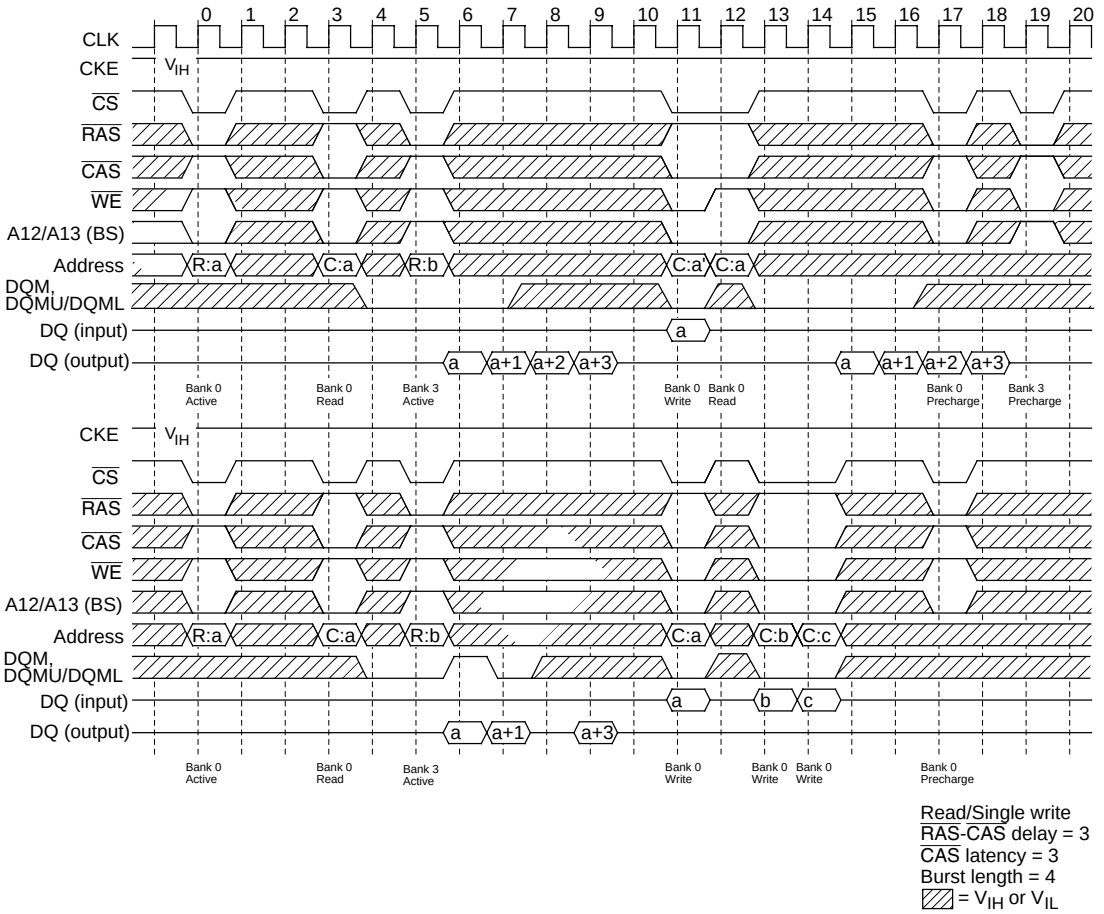
Mode Register Set Cycle



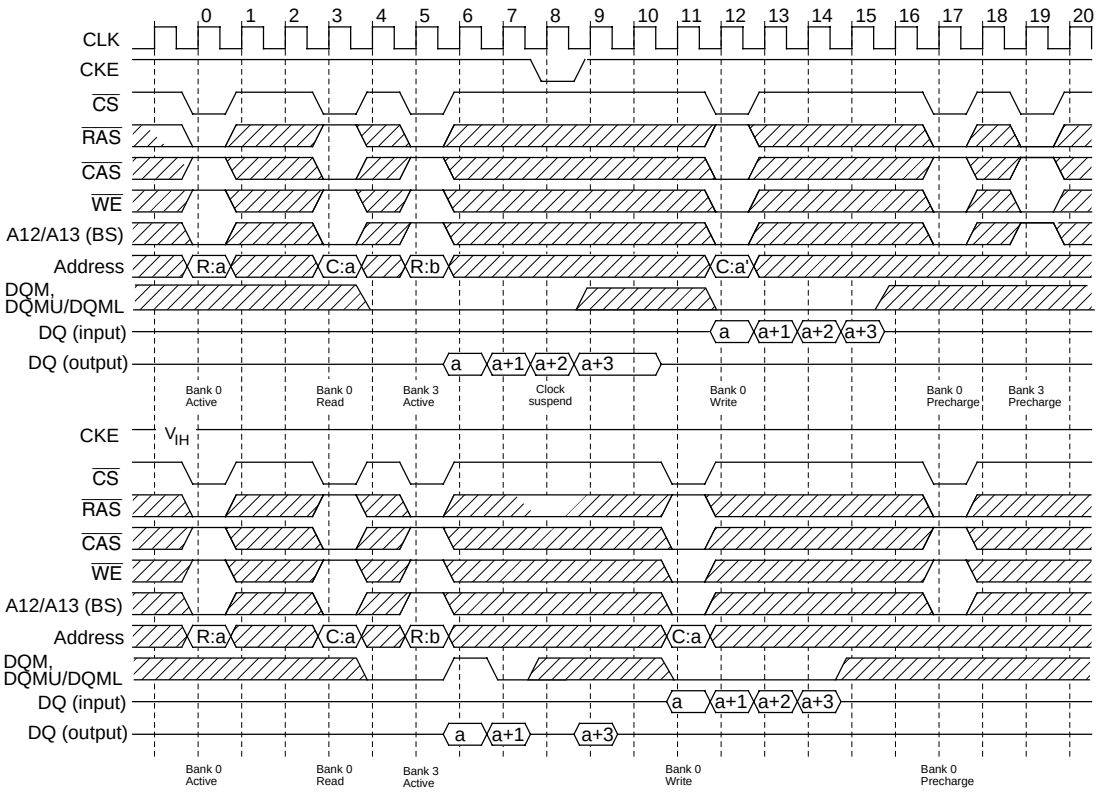
Read Cycle/Write Cycle



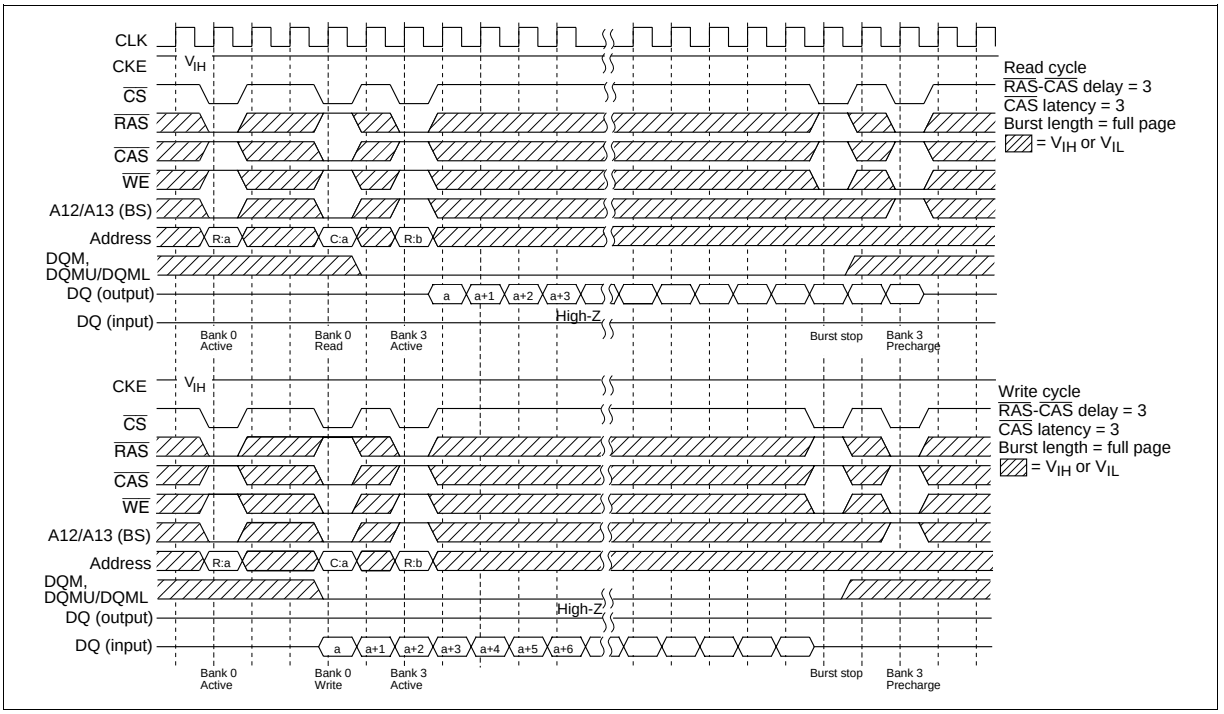
Read/Single Write Cycle



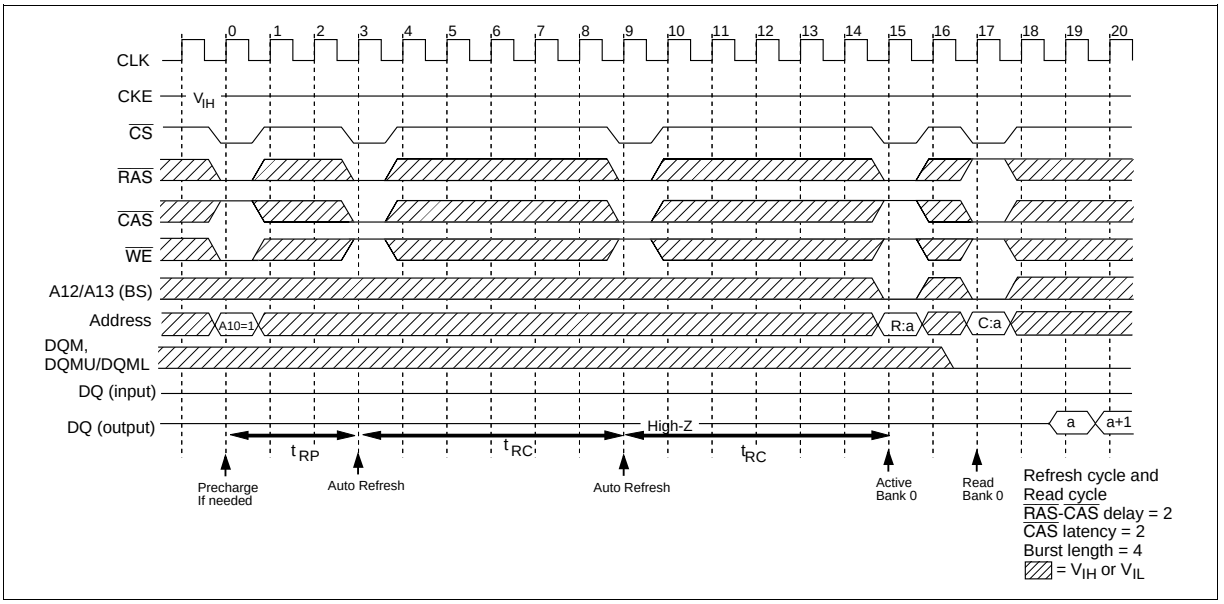
Read/Burst Write Cycle



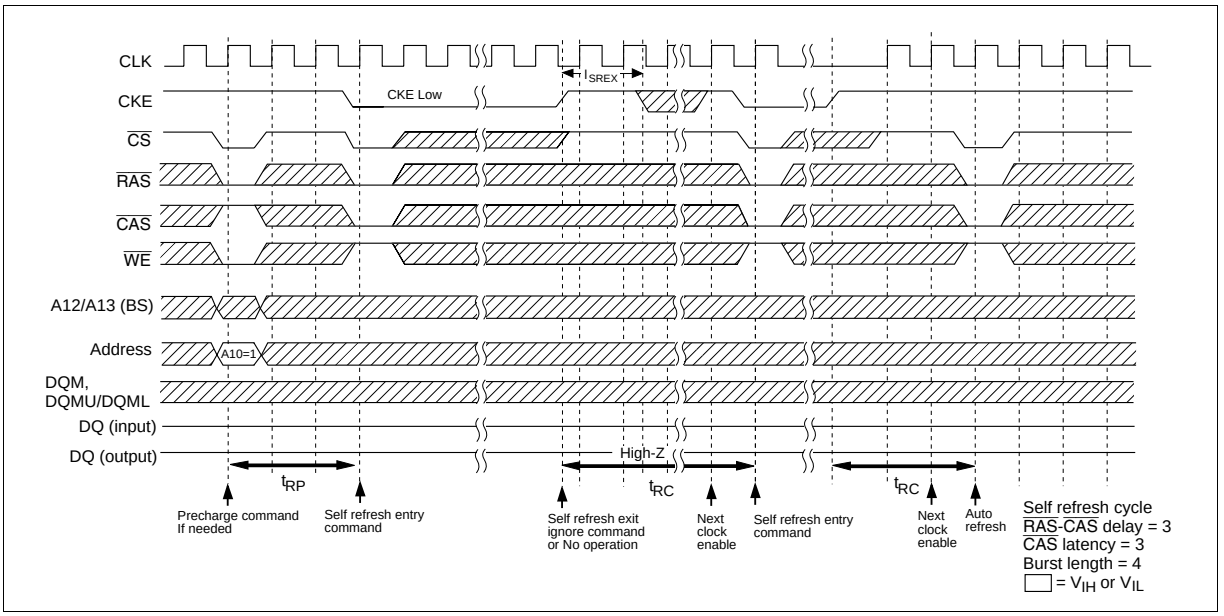
Full Page Read/Write Cycle



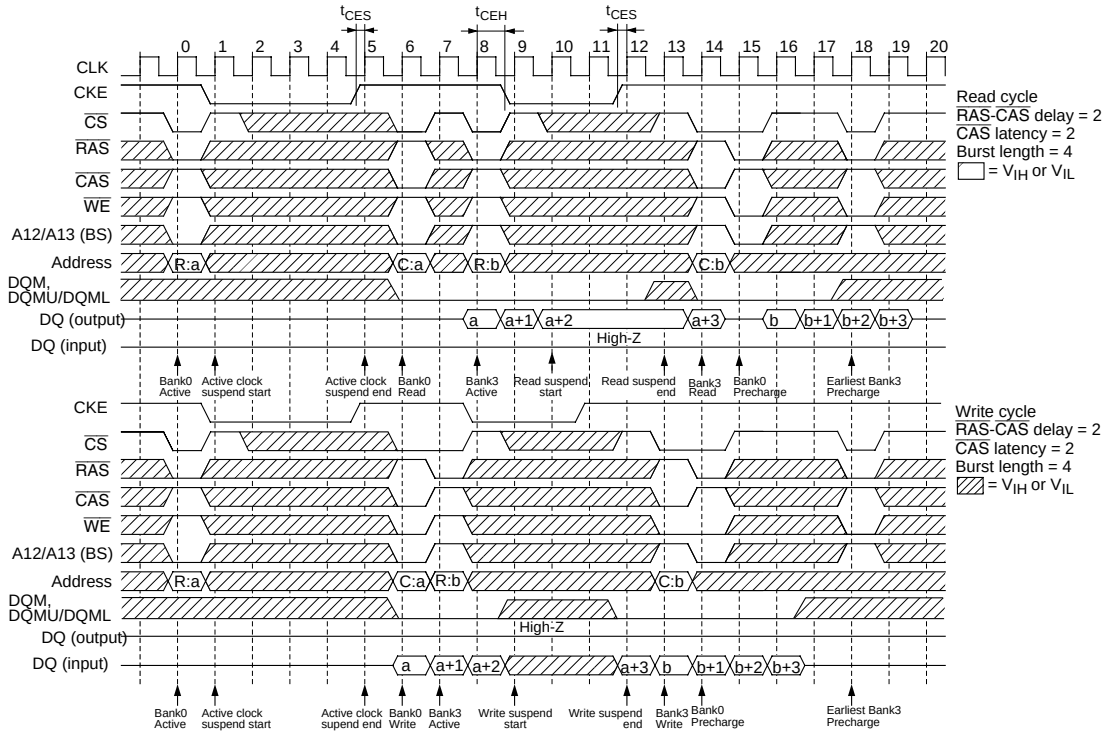
Auto Refresh Cycle



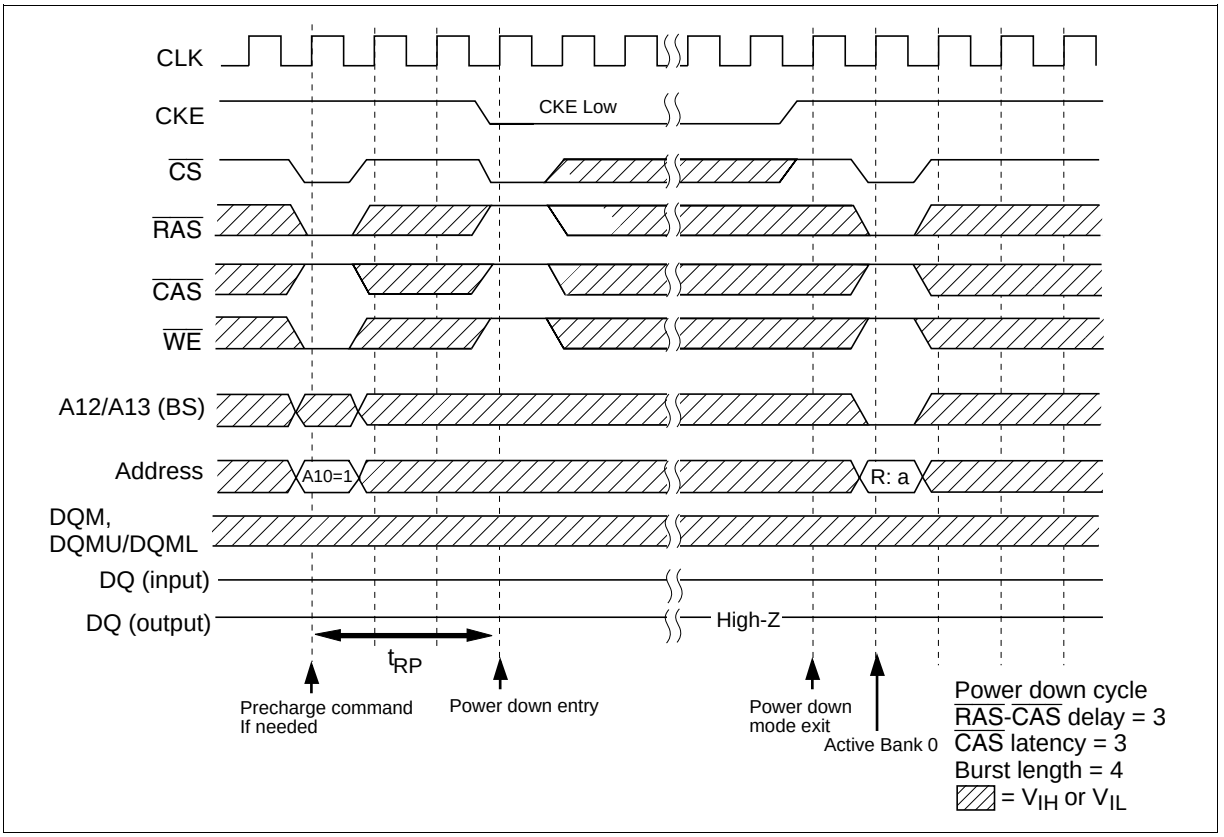
Self Refresh Cycle



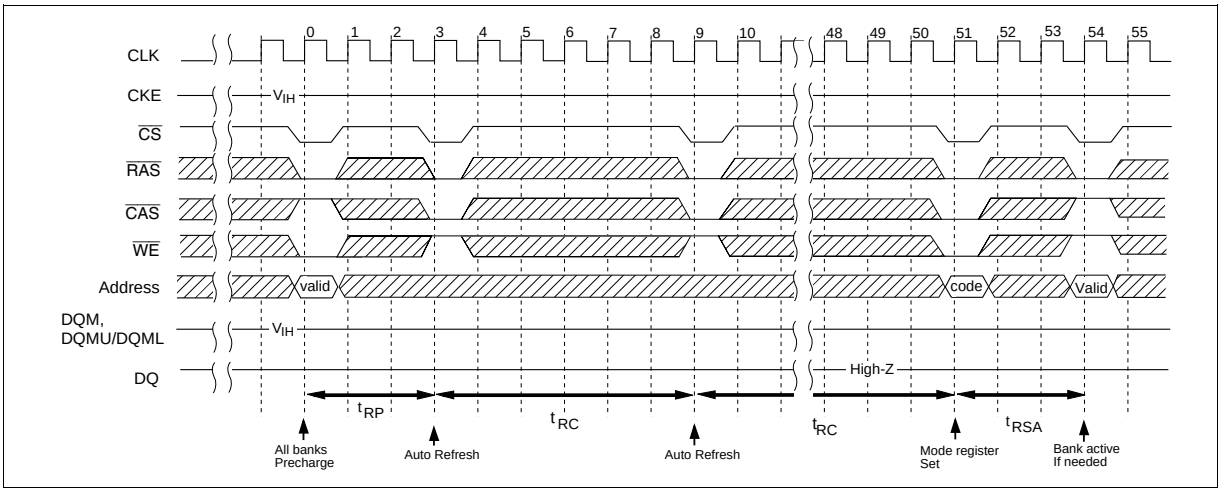
Clock Suspend Mode



Power Down Mode



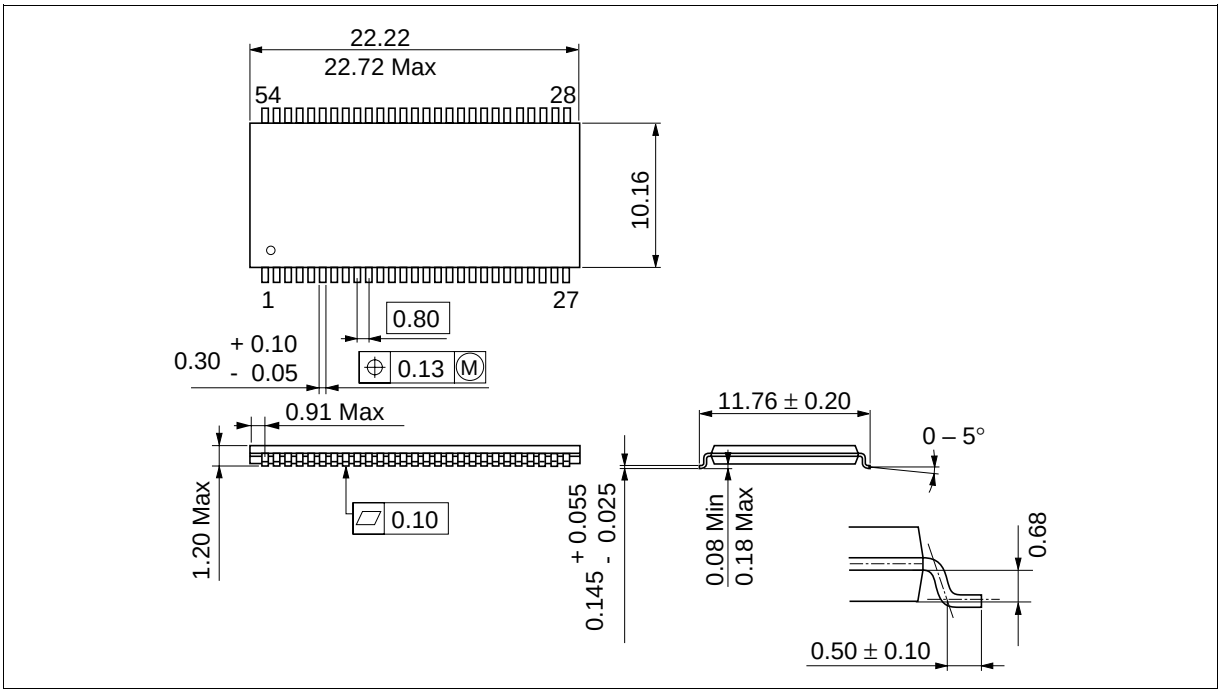
Power Up Sequence



Package Dimensions

HM5264165TT/HM5264805TT/HM5264405TT Series (TTP-54D)

Unit: mm



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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	May. 30, 1996	Initial issue	H. Miyashita	K. Sato
0.1	Nov. 29, 1996	Correct errors Operation of HM5264165/5264805/5264405 Series Change of description for Read/Write operaion and Full-page burst stop DC Characteristics (HM5264165) I_{CC3} max: 7/7/7 mA to 12/12/12 mA I_{CC4} (CL = 2) max: 100/85/65 mA to 150/130/100 mA I_{CC4} (CL = 3) max: 150/125/100 mA to 200/180/140 mA I_{CC4} test conditions: BL = 4 to BL = 8 I_{CC6} max: 2/2/2 mA to 3/3/3 mA Addition of I_{CC5} test conditions: Address = V_{IL} or V_{IH} Fixed Addition of notes8 and 9 DC Characteristics (HM5264805) I_{CC2} max: 40/35/30 mA to 50/45/35 mA I_{CC3} max: 7/7/7 mA to 12/12/12 mA I_{CC3} max: 45/40/35 mA to 55/50/40 mA I_{CC4} (CL = 2) max: 100/85/65 mA to 150/130/100 mA I_{CC4} (CL = 3) max: 150/125/100 mA to 200/180/140 mA I_{CC4} test conditions: BL = 4 to BL = 8 I_{CC6} max: 2/2/2 mA to 3/3/3 mA Addition of I_{CC5} test conditions: Address = V_{IL} or V_{IH} Fixed Addition of notes8 and 9 DC Characteristics (HM5264405) I_{CC3} max: 7/7/7 mA to 12/12/12 mA I_{CC4} (CL = 2) max: 100/85/65 mA to 140/120/95 mA I_{CC4} (CL = 3) max: 150/125/100 mA to 190/170/135 mA I_{CC4} test conditions: BL = 4 to BL = 8 I_{CC5} max: 130/110/85 mA to 150/125/100 mA I_{CC6} max: 2/2/2 mA to 3/3/3 mA Addition of I_{CC5} test conditions: Address = V_{IL} or V_{IH} Fixed Addition of notes8 and 9 AC Characteristics t_{AC} (CL = 2) max: 12/15/17 ns 9/13/15 ns	A. Kumata	K. Sato
0.2	Dec. 17, 1996	Correct errors Change of description for Command Truth Table Change of figures for Operation of HM5264165, HM5264805, HM5264405 Series Change of description for Self-refresh Recommended DC Operating Conditions Change of notes2 AC Characteristics Change of symbol: t_{DPL} to t_{DPL} Timing Waveforms Change of Full Page Read/Write cycle		