TTChip austriamicrosystems

AS8202NF

TTP-C2NF Communication Controller

Data Sheet
Rev.1.4, July 2005

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1. General Description

The AS8202NF communication controller is an integrated device supporting serial communication according to the TTP® specification version 1.1. It performs all communication tasks such as reception and transmission of messages in a TTP cluster without interaction of the host CPU. TTP provides mechanisms that allow the deployment in high-dependability distributed real-time systems. It provides the following services:

- Predictable transmission of messages with minimal jitter
- Fault-tolerant distributed clock synchronization
- Consistent membership service with small delay
- Masking of single faults

The CNI (communication network interface) forms a temporal firewall. It decouples the controller network from the host subsystem by use of a dual ported RAM (CNI). This prevents the propagation of control errors. The interface to the host CPU is implemented as a 16-bit wide non-multiplexed asynchronous bus interface.

TTP follows a conflict-free media access strategy called time division multiple access (TDMA). This means, TTP deploys a time slot technique based on a global time that is permanently synchronized. Each node is assigned a time slot in which it is allowed to perform transmit operation. The sequence of time slots is called TDMA round, a set of TDMA rounds forms a cluster cycle. The operation of the network is repeated after one cluster cycle. The sequence of interactions forming the cluster cycle is defined in a static time schedule, called message descriptor list (MEDL). The definition of the MEDL in conjunction with the global time determines the response time for a service request.

The membership of all nodes in the network is evaluated by the communications controller. This information is presented to all correct cluster members in a consistent fashion. During operation, the status of all other nodes is propagated within one TDMA round. Please read more about TTP and request the TTP specification at www.tttech.com.

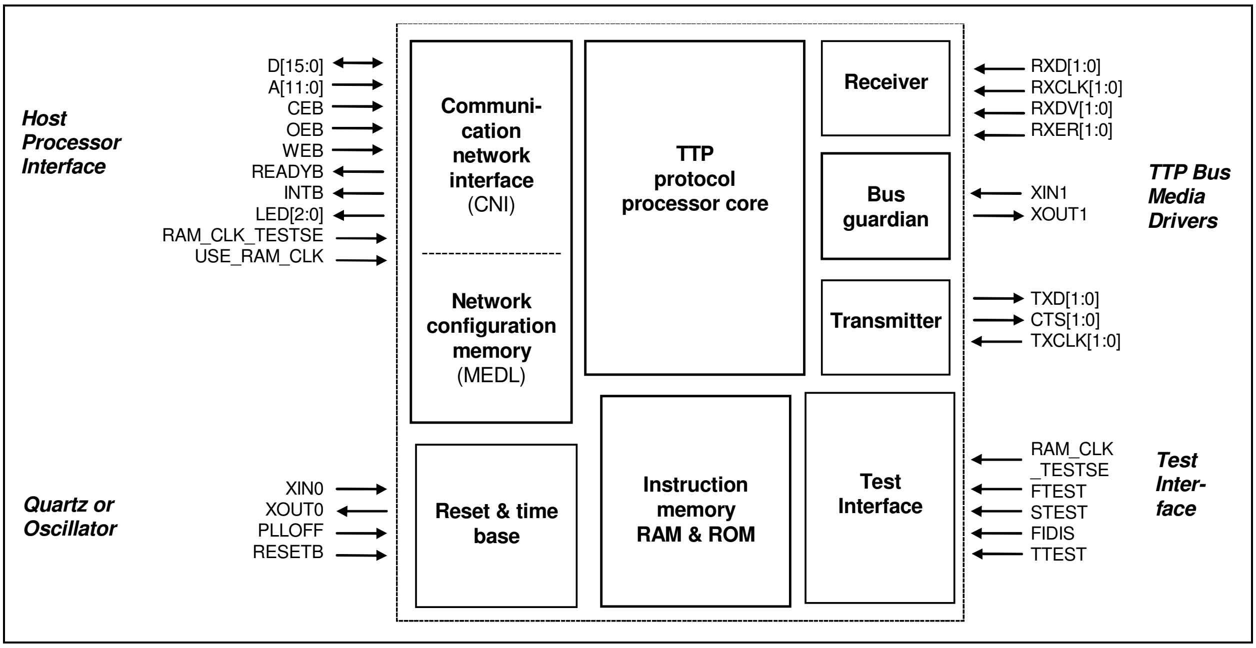


Figure 1. AS8202NF Block Diagram

2. Benefits

The AS8202NF provides support for fault-tolerant, high-speed bus systems in a single device. The communication controller is qualified for the full temperature range required for automotive applications and is certifiable according to RTCA standards. It offers superior reliability and supports data transfer rates of 25 Mbit/s with MII and up to 5 Mbit/s with MFM/Manchester. The AS8202NF is the first TTP controller to support both MFM and Manchester coding. Manchester coding is important for DC-free data transmission, which allows the use of transformers in the data stream. The AS8202NF is pin-compatible with its predecessor, the AS8202.

3. Key Features

- Dedicated controller supporting TTP (time-triggered protocol class C)
- Suited for dependable distributed real-time systems with guaranteed response time
- Application fields: automotive (by-wire braking, steering, vehicle dynamics control, drive train control), aerospace (aircraft electronic systems), industrial systems, railway systems
- Asynchronous data rate up to 5 Mbit/s (MFM / Manchester)
- Synchronous data rate 5 to 25 Mbit/s
- Bus interface (speed, encoding) for each channel selectable independently
- 40 MHz main clock with support for 10 MHz crystal, 10 MHz oscillator or 40 MHz oscillator
- 16 MHz bus guardian clock with support for 16 MHz crystal or 16 MHz oscillator
- Single power supply 3.3V, 0.35µm CMOS process
- Full automotive temperature range (-40°C to 125°C)
- 16k x 16 SRAM for message, status, control area (communication network interface) and for scheduling information (MEDL)
- 4k x 16 (plus parity) instruction code RAM for protocol execution code
- Data sheet conforms to protocol revision 2.03
- 16k x 16 instruction code ROM containing startup execution code and deprecated protocol code revision 1.00
- 16 Bit non-multiplexed asynchronous host CPU interface
- 16 Bit RISC architecture
- Software tools, design support, development boards available (www.tttech.com)
- 80 pin LQFP80 Package

4. Pin Assignment

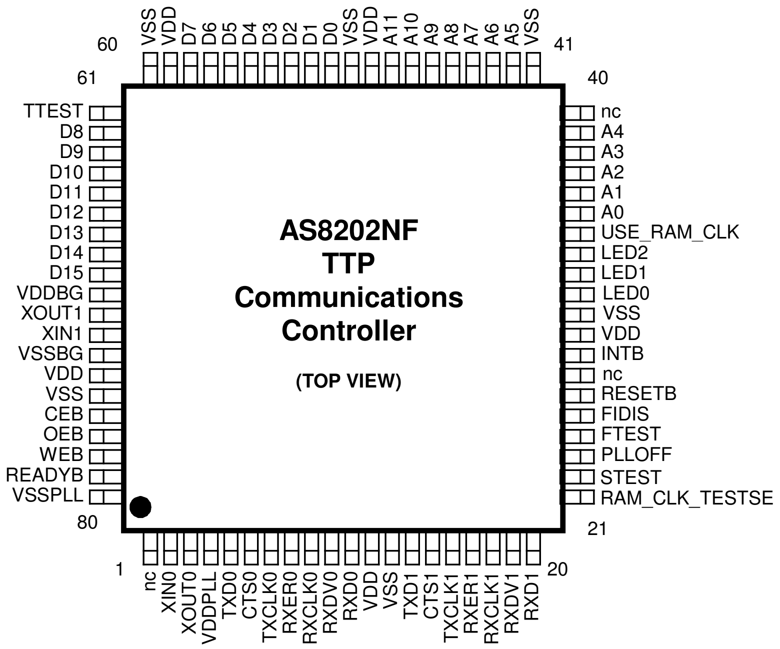


Figure 2. LQFP 80 Pin Package and Pin Assignment

5. Pin Description

Pin	Name	Dir	Function
12,29,49,59,74	VDD	P	Positive Power Supply
13,30,41,50,60,75	VSS	P	Negative Power Supply
70	VDDBG	P	Positive Power Supply for Bus Guardian (connect to VDD)
73	VSSBG	P	Negative Power Supply for Bus Guardian (connect to VSS)
4	VDDPLL	P	Positive Power Supply for Main Clock PLL (connect to VDD)
80	VSSPLL	P	Negative Power Supply for Main Clock PLL (connect to VSS)
21	RAM_CLK_TESTSE	I_{PD}	RAM_CLK when STEST='0' and USE_RAM_CLK='1', else Test Input, connect to VSS if not used
22	STEST	I_{PD}	Test Input, connect to VSS
24	FTEST	I_{PD}	Test Input, connect to VSS
25	FIDIS	I_{PD}	Test Input, connect to VSS
61	TTEST	I_{PU}	Test Input, connect to VDD
34	USE_RAM_CLK	I_{PD}	RAM_CLK Pin Enable, connect to VSS if not used
2	XIN0	A	Main Clock: Analog CMOS Oscillator Input, use as input when providing external clock
3	XOUT0	A	Main Clock: Analog CMOS Oscillator Ouptut, leave open when providing external clock
23	PLLOFF	I_{PD}	Main Clock PLL Disable Pin, connect to VSS when providing 10 MHz crystal for enabling the internal PLL
72	XIN1	A	Bus Guardian Clock: Analog CMOS Oscillator Input, use as input when providing external clock
71	XOUT1	A	Bus Guardian Clock: Analog CMOS Oscillator Output, leave open when providing external clock
26	RESETB	I_{PU}	Main Reset Input, active low
5	TXD0	O_{PU}	TTP Bus Channel 0: Transmit Data
6	CTS0	O_{PD}	TTP Bus Channel 0: Transmit Enable
11	RXD0	I_{PU}	TTP Bus Channel 0: Receive Data
7	TXCLK0	I_{PD}	TTP Bus Channel 0: Transmit Clock (MII mode)
8	RXER0	I_{PU}	TTP Bus Channel 0: Receive Error (MII mode)

Pin	Name	Dir	Function
9	RXCLK0	I_{PD}	TTP Bus Channel 0: Receive Clock (MII mode)
10	RXDV0	I_{PU}	TTP Bus Channel 0: Receive Data Valid (MII mode)
14	TXD1	O_{PU}	TTP Bus Channel 1: Transmit Data
15	CTS1	O_{PD}	TTP Bus Channel 1: Transmit Enable
20	RXD1	I_{PU}	TTP Bus Channel 1: Receive Data
16	TXCLK1	I_{PD}	TTP Bus Channel 1: Transmit Clock (MII mode)
17	RXER1	I_{PU}	TTP Bus Channel 1: Receive Error (MII mode)
18	RXCLK1	I_{PD}	TTP Bus Channel 1: Receive Clock (MII mode)
19	RXDV1	I_{PU}	TTP Bus Channel 1: Receive Data Valid (MII mode)
35-39, 42-48	A[11:0]	I	Host Interface (CNI) Address Bus
51-58, 62-69	D[15:0]	I/O	Host Interface (CNI) Data Bus, tristate
76	CEB	I_{PU}	Host Interface (CNI) Chip Enable, active low
77	OEB	I_{PU}	Host interface (CNI) output enable, active low
78	WEB	I_{PU}	Host interface (CNI) write enable, active low
79	READYB	O_{PU}	Host interface (CNI) transfer finish signal, active low, open drain[1]
28	INTB	O_{PU}	Host interface (CNI) time signal (interrupt), active low, open drain
31-33	LED[2:0]	O_{PD}	Configurable generic output port
1, 27, 40	nc		Not connected, leave open

Note 1: At de-assertion READYB is driven to the inactive value (high) for a configurable time.

5.1. Pin Directions

Dir	Function
I	TTL Input
I_{PU}	TTL Input with Internal Weak Pull-Up
I_{PD}	TTL Input with Internal Weak Pull-Down
I/O	TTL Input/Output with Tristate
O_{PU}	TTL Output with Internal Weak Pull-Up at Tristate
O_{PD}	TTL Output with Internal Weak Pull-Down at Tristate
A	Analog CMOS Pin
P	Power Pin

6. Electrical Specifications

6.1. Absolute Maximum Ratings (Non Operating)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC Supply Voltage	VDD		-0.3		5.0	V
Input Voltage	Vin	any pin	-0.3		VDD+0.3	V
Input Current	Iin	any pin, TA=25°C	-100		100	mA
Storage Temperature	Tstrg		-55		150	°C
Soldering Temperature	Tsold	t=10 sec, Reflow and Wave			235	°C
Humidity	H		5		85	%
Electrostatic Discharge	ESD	HBM: 1KV Mil.std.883, Method 3015.7	1000			V

Note: Stresses higher than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device under these or any other conditions higher than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability (e.g. hot carrier degradation).

6.2. Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC Supply Voltage[1]	VDD	VSS=0V	3.0	3.3	3.6	V
Ambient Temperature[1]	TA		-40		125	°C
Static Supply Current	IDDs	all inputs tied to VDD/VSS, clocks stopped, exclusive of I/O drive requirements, VDD=3.6V	5		900	µA

Operating Supply Current[2]	IDD	VDD=3.3V, PLL active, exclusive of I/O drive requirements			100[4]	mA
Clock Period of Main Clock (external) [2]	CLK0_ext_PLL	PLL active[3]		100		ns
	CLK0_ext	PLL inactive		25		ns
Clock Period of Bus Guardian Clock[2]	CLK1			62.5		ns

Note 1: The input and output parameter values in this table are directly related to ambient temperature and DC supply voltage. A temperature range other than Ta_{min} to Ta_{max} or a supply voltage range other than VDD_{min} to VDD_{max} will affect these values and must be evaluated on its own.

Note 2: Typical values: CLK0=40 MHz, CLK1=16 MHz

Note 3: Using the internal PLL multiplies the main clock frequency by 4.

Note 4: To be defined

6.3. DC Electrical Characteristics

TTL Input Pins and TTL Bidirectional Pins in Input/Tristate Mode

Parameter	Symbol	Conditions		Min[1]	Typ	Max[1]	Unit
Input Low Voltage	Vil					0.8	V
Input High Voltage	Vih			2.0			V
Input Leakage Current	Iin	Pins without pad resistors, VDD=3.6V				±1	µA
Input Low Current	Iil	Pins with pull-down resistors VDD=3.0V	Vin=0.4V	4.9[3]			µA
			Vin=0.8V	8.8[3]			
		Pins with pull-up resistors	VDD=3.6V Vin=0V	-15		-75	
Input High Current	Iih	Pins with pull-down resistors	VDD=3.6V Vin=3.6V	15		75	µA
		Pins with pull-up resistors VDD=3.0V	Vin=2.0V	-10.7[3]			
			Vin=2.5V	-6[3]			
Input Capacitance	Cin				4.5[2]		pF

CMOS Inputs (XIN), drive from external clock generator

Drive at XIN (XOUT = open)

Parameter	Symbol	Conditions	Min[1]	Typ	Max[1]	Unit
Input Capacitance	C_xin	Input slope 2ns, Vil=0V, Vih=3.3V, VDD=3.3V		1.9	2.5	pF
Input Current	Iin_xin				±1[2]	µA
Input Low Voltage	Vil_xin		0		0.3*VDD	V
Input High Voltage	Vih_xin		0.7*VDD		VDD	V

Outputs and TTL Bidirectional Pins in Output Mode

Parameter	Symbol	Conditions		Min[1]	Typ	Max[1]	Unit
Output Low Current	Iol	VDD=3.0V, Vo = 0.4V				-4	mA
Output High Current	Ioh	VDD=3.0V, Vo = 2.5V				4	mA
Output Tristate Current	Ioz	VDD=3.6V				±10[2]	µA
Transition Time – Rise	Tr T(Vout=0.1*VDD) to T(Vout=0.9*VDD)	T = 125 °C, Slow Process, VDD=3.0V, Cload=35pF	TXD[1,0], CTS[1,0], LED[2:0], INTB			8.1[3]	ns
			D[15:0], READYB			8.9[3]	
Transition Time – Fall	Tf T(Vout=0.9*VDD) to T(Vout=0.1*VDD)	T = 125 °C, Slow Process, VDD=3.0V, Cload=35pF	TXD[1,0], CTS[1,0], LED[2:0], INTB			6[3]	ns
			D[15:0], READYB			7[3]	

Note 1: If Min/Max values are both negative, they are ordered according to their absolute value.

Note 2: Typical value, not tested during production.
Note 3: Implicitly tested.

8. Application Information

8.1. Host CPU Interface

The host CPU interface, also referred to as CNI (Communication Network Interface), connects the application circuitry to the AS8202NF TTP controller. All related signal pins provide an asynchronous read/write access to a dual ported RAM located in the AS8202NF. There are no setup/hold constraints referring to the microtick (main clock "CLK0").

The host interface features an interrupt or time signal INTB to notify the application circuitry of programmed and protocol-specific, synchronous and asynchronous events.

The host CPU interface allows access to the internal instruction code memory. This is required for proper loading of the protocol execution code into the internal instruction code RAM, for extensive testing of the instruction code RAM and for verifying the instruction code ROM contents.

INTB is an open-drain output, i.e. the output is only driven to '0' and is weak-pull-up at any other time, so external pull-up resistors or transistors may be necessary depending on the application.

READYB is also an open-drain output, but with a possibility to be driven to '1' for a defined time (selectable by register) before weak-pull-up at any other time.

The **LED** port is software-configurable to automatically show some protocol-related states and events, see below for the LED port configuration.

Host Interface Ports

Pin Name	Mode	Width	Comment
A[11:0]	in	12	CNI address bus, 12 bit (A0 is LSB)
D[15:0]	inout (tri)	16	CNI data bus, 16 bit (D0 is LSB)
CEB	in	1	CNI chip enable, active low
WEB	in	1	CNI write enable, active low
OEB	In	1	CNI output enable, active low
READYB	out (open drain)	1	CNI ready, active low
INTB	out (open drain)	1	CNI interrupt, time signal, active low
RAM_CLK_TESTSE	in	1	HOST clock
USE_RAM_CLK	in	1	HOST clock pin enable

Asynchronous READYB permits the shortest possible bus cycle but eventually requires signal synchronization in the application. Connect USE_RAM_CLK to VSS to enable this mode of operation.

Synchronous READYB uses an external clock (usually the host processor's bus clock) for synchronization of the signal eliminating external synchronization logic. Connect USE_RAM_CLK to VDD and RAM_CLK_TESTSE to the host processor's bus clock to enable this mode of operation.

Asynchronous DPRAM interface

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Controller Cycle Time	Tc			25		ns
Input Valid to CEB, WEB (Setup Time)	1a	A[11:0]	5			ns
	2a	D[15:0]				
CEB, WEB to Input Invalid (Hold Time)	1b	A[11:0]	3			ns
	2b	D[15:0]	4			
Input Rising to CEB, WEB Falling	3	CEB, WEB, OEB	5[1,2]			ns
CEB, WEB Rising to Input Falling	4	CEB, WEB, OEB	5[1,2]			ns
Write Access Time (CEB, WEB to READYB)	5	min = 1 Tc, max = 4 Tc	25		100	ns
CEB, WEB de-asserted to READYB de-asserted	6				9.4	ns
Input Valid to CEB, OEB (Setup Time)	7a	A[11:0]	5			ns
CEB, OEB to Input Invalid (Hold Time)	7b	A[11:0]	2			ns
Input Rising to CEB, OEB Falling	8	CEB, WEB, OEB	5[1]			ns
CEB, OEB Rising to Input Falling	9	CEB, WEB, OEB	5[1]			ns
Read Access Time (CEB, OEB to READYB)	10	min = 1.5 Tc, max = 6 Tc	37.5		150	ns
CEB, OEB asserted to signal asserted	11a	D[15:0]	4.0		8.4	ns
CEB, OEB de-asserted to signal de-asserted	11b	D[15:0]	3.8		8	ns
	11c	READYB			8.8	
READYB, D skew	12				±2	ns
RAM_CLK_TESTSE Rising to READYB Falling	13	USE_RAM_CLK='1'	3.7		13.5	ns
RAM_CLK_TESTSE Rising to READYB Rising	14	USE_RAM_CLK='1'	3		9.7	ns
RAM_CLK_TESTSE Rising to READYB Deactivated 1->Z	15	USE_RAM_CLK ='1' Ready delay='00'	3.6		12.9	ns
		Ready delay='01'	4.5		15.4	
		Ready delay='10'	5.4		18.8	
		Ready delay='11'	6.4		22.2	
Read to Read Access Inactivity Time (CEB, OEB low to CEB, OEB low)	16	min = 1.5 Tc	37.5[1]			ns
Read to Write Access Inactivity Time (CEB, OEB low to CEB, WEB low)	17		5[1]			ns
Write to Write Access Inactivity Time (CEB, WEB low to CEB, WEB low)	18		5[1,2]			ns
Write to Read Access Inactivity Time (CEB, WEB low to CEB, OEB low)	19	min = 2.5 Tc	62.5[1,2]			ns

Note 1: Prior to starting a read or write access, CEB, WEB and OEB have to be stable for at least 5 ns (see symbol 3, 4, 8, 9). In addition the designer has to consider the minimum inactivity time according to symbols 16, 17, 18, 19. See Figure 3 for more information on the inactivity times.

Note 2: To allow proper internal initialization, after finishing any write access (CEB or WEB is high) to the internal CONTROLLER_ON register, CEB OEB and WEB have to be stable high within 200 ns (min = 8 Tc).

Note: All values not tested during production, guaranteed by design.

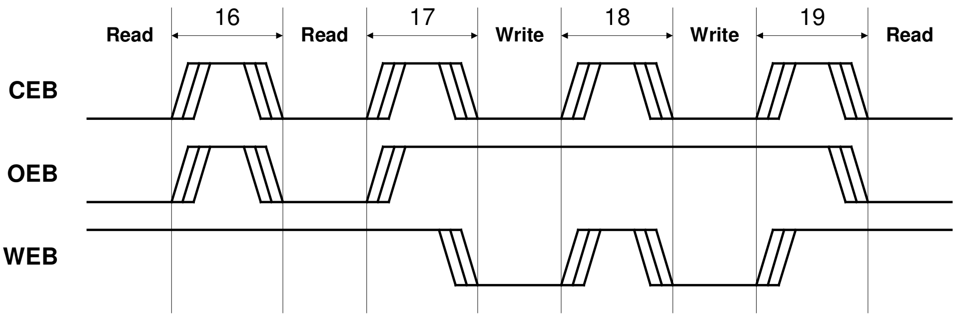


Figure 3. Read/Write Access Inactivity Time

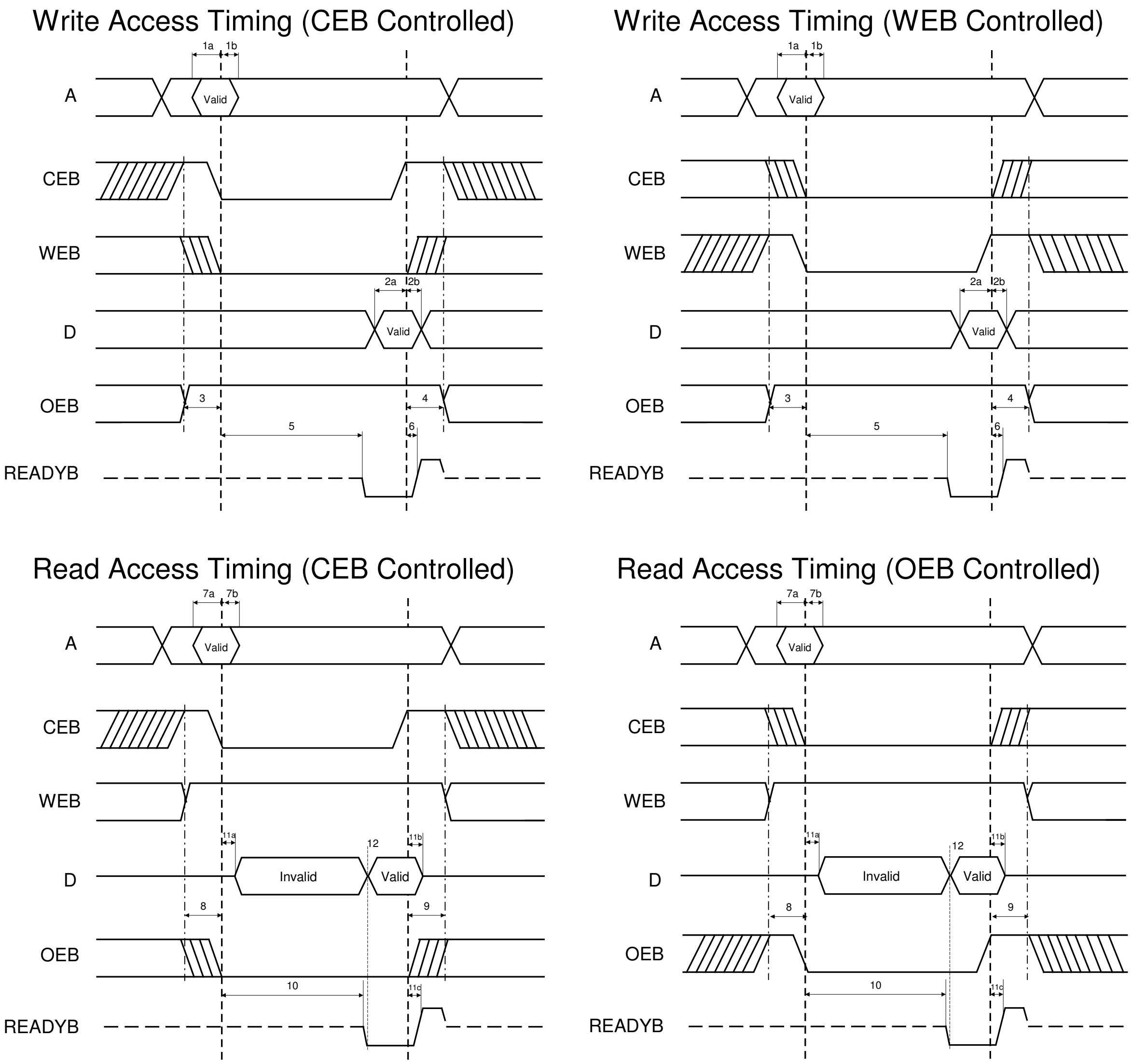


Figure 4. Host Read/Write Access Timing

Synchronous READYB Generation

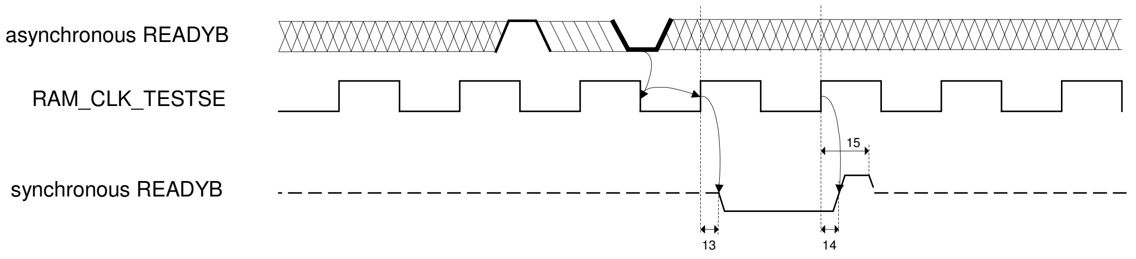


Figure 5. Synchronous READYB Timing

Synchronous READYB is aligned to host clock (with pulse duration of one host clock cycle) to fulfill the required host timing constraints for input setup and input hold time to/after host clock rising edge.

Note: Connect USE_RAM_CLK to VDD and RAM_CLK_TESTSE to the host processor's bus clock to enable this mode of operation.

8.2. Reset and Oscillator

Pin Name	Mode	Comment
XIN0	analog	main oscillator input (external clock input)
XOUT0	analog	main oscillator output
XIN1	analog	bus guardian oscillator input (external clock input)
XOUT1	analog	bus guardian oscillator output
PLLOFF	in	PLL disable
RESETB	in	external reset

External Reset Signal

To issue a reset of the chip the RESETB port has to be driven low for at least 1 us. Pulses under 50 ns duration are discarded. At power-up the reset must overlap the build-up time of the power supply.

Integrated Power-On Reset

The Device has an internal Power-On Reset generator. When supply voltage ramps up, the internal reset signal is kept active (low) for 33 µs typical.

Parameter	Symbol	Min	Typ	Max	Unit
supply voltage slope	dV/dt	551	-	-	V/ms
power on reset active time after VDD > 1,0V	tpores	25	33	49	µs

Note 1: In case of non-compliance keep the external reset (RESETB) active for min. 5 ms after supply voltage is valid and oscillator inputs active.

Oscillator Circuitry

The internal oscillators for main and bus guardian clock require external quartzes or external oscillators. The main clock features a PLL multiplying a 10 MHz XIN0/XOUT0 oscillation to an internal frequency of 40 MHz when enabled.

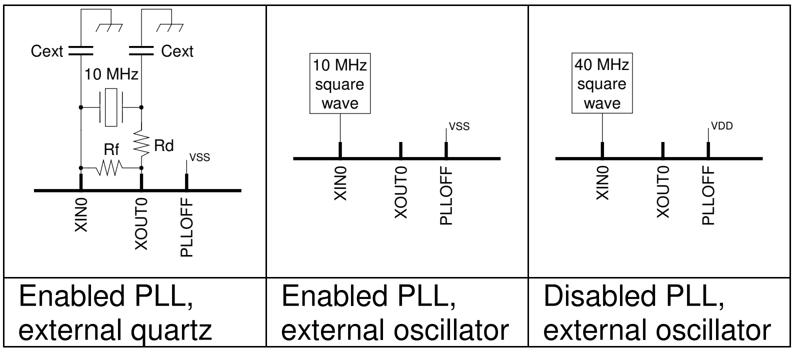


Figure 6. Main clock setup

Rf will normally not be soldered, it is only provided to get maximum flexibility. Cext, typ = 15/18 pF. Rd has to be calculated, if the measured drive level will be too high; if drive level is ok, Rd = 0.

If using an external oscillator at 10 MHz with enabled internal PLL, the oscillator must have a period of 100 ns with low jitter. Note that a crystal-based clock is recommended over a derived clock (i.e., PLL-based) to allow best internal PLL performance.

Parameter	Conditions	Min	Typ	Max	Unit
R_osc10	Oscillation margin @ 10 MHz, Cload = 18 pF	0.95[1]	1.62[1]		kOhm
R_osc16	Oscillation margin @ 16 MHz, Cload = 18 pF	0.37[1]	0.64[1]		kOhm
R_osc20	Oscillation margin @ 20 MHz, Cload = 18 pF	0.24[1]	0.41[1]		kOhm

Note 1: Not tested during production.
Cload is the value of the external load capacitors towards ground. The total load capacitance seen by the quartz will be Cload_tot = (Cload + Cpar)/2. Cpar is the equivalent parasitic capacitance of the oscillator cell inputs and the PCB and is derived from measurements to be about 3.5 … 4.0 pF.

The bus guardian clock has no internal PLL and must be connected to either a 16 MHz Quartz or an external 16 MHz oscillator:

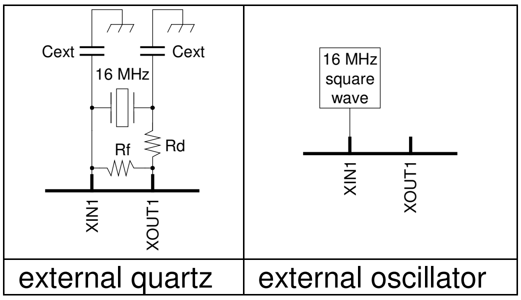


Figure 7. Bus Guardian clock setup

Both the XIN0/XOUT0 (main clock) and the XIN1/XOUT1 (bus guardian clock) cells support driving a quartz crystal oscillation as well as clock input by an external oscillator.

Build-up Characteristics

Parameter	Symbol	Pin	Min	Typ	Max	Note
Oscillator startup time (Main clock)	Tosc_startup0	XIN0/XOUT0			20 ms	Quartz frequency: 10 MHz
Oscillator startup time (Bus Guardian clock)	Tosc_startup1	XIN1/XOUT1			20 ms	Quartz frequency: 16 MHz

Parameter	Symbol	Pin	Min	Typ	Max	Note
PLL startup time (Main clock)	Tpll_startup0	XIN0/XOUT0			20 ms	Quartz frequency: 10 MHz

8.3. TTP Bus Interface

The AS8202NF contains two TTP bus units, one for each TTP channel, building the TTP bus interface. Each TTP bus channel contains a transmitter and a receiver and can be configured to be either in the asynchronous or synchronous mode of operation. Note that the two channels (channel 0 and channel 1) can be configured independently for either of these modes.

The drivers of the TXD and CTS pins are actively driven only during a transmission window, all the other time the drivers are switched off and the weak pull resistors are active. External pull resistors must be used to define the signal levels during idle phases. Note that the transmission window may be different for each channel.

Pin Name	TX inactive
TXD[0]	weak pull-up
CTS[0]	weak pull-down
TXD[1]	weak pull-up
CTS[1]	weak pull-down

8.4. TTP Asynchronous Bus Interface

When in asynchronous mode of operation the channel's bus unit uses a self-clocking transmission encoding which can be either MFM or Manchester at a maximum data rate of 5 Mbit/s on a shared media (physical bus). The pins can either be connected to drivers using recessive/dominant states on the wire as well as drivers using active push/pull functionality.

The RXD signal uses '1' as the inactivity level. In the so-called RS485 compatible mode longer periods of '0' are treated as inactivity, too. If the RS485 compatible mode is not used, the application must care to drive RXD to '1' during inactivity on the bus.

Pin Name	Mode	Connect to PHY	Comment
TXD[0]	out	TXD	Transmit data channel 0
CTS[0]	out	CTS	Transmit enable channel 0
TXCLK[0]	in		No function (do not connect)
RXER[0]	in		No function (do not connect)
RXCLK[0]	in		No function (do not connect)
RXDV[0]	in		No function (do not connect)
RXD[0]	in	RXD	Receive data channel 0
TXD[1]	out	TXD	Transmit data channel 1
CTS[1]	out	CTS	Transmit enable channel 1
TXCLK[1]	in		No function (do not connect)
RXER[1]	in		No function (do not connect)
RXCLK[1]	in		No function (do not connect)
RXDV[1]	in		No function (do not connect)
RXD[1]	in	RXD	Receive data channel 1

8.5. TTP Synchronous Bus Interface

When in synchronous mode of operation, the bus unit uses a synchronous transfer method to transfer data at a rate between 5 and 25 Mbit/s. The interface is designed to run at 25 Mbit/s and to be gluelessly compatible with the commercial 100 Mbit/s Ethernet MII (Media Independent Interface) according to IEEE standard 802.3 (Ethernet CSMA/CD).

Connecting the synchronous TTP bus unit to a 100 Mbit/s Ethernet PHY is done by connecting TXD, CTS, TXCLK, RXER, RXCLK, RXDV and RXD of any channel to TXD0, TXEN, TXCLK, RXER, RXCLK, RXDV and RXD0 of the PHY's MII. The pins TXD1, TXD2 and TXD3 of the PHY's MII should be linked to VSS. The signals RXD1, RXD2, RXD3, COL and CRS as well as the MMII (Management Interface) should be left open or can be used for diagnostic purposes by the application.

Note that the frames sent by the AS8202NF are not Ethernet compatible and that an Ethernet Hub (not a Switch) can be used as a 'star coupler' for proper operation. Also note that the Ethernet PHY must be configured for Full Duplex operation (even though the Hub does not support full duplex), because TTP has its own collision management that should not interfere with the PHY's Half-Duplex collision management. In general, the PHY must not be configured for automatic configuration ('Auto negotiation') but be hard-configured for 100 Mbit/s, Full Duplex operation. Note that to run the interface at a rate other than 25 Mbit/s other transceiver PHY components have to be used.

Pin Name	Mode	Connect to PHY	Comment
TXD[0]	out	TXD0	Transmit data channel 0
CTS[0]	out	TXEN	Transmit enable channel 0
TXCLK[0]	in	TXCLK	Transmit clock channel 0
RXER[0]	in	RXER	Receive error channel 0
RXCLK[0]	in	RXCLK	Receive clock channel 0
RXDV[0]	in	RXDV	Receive data valid channel 0
RXD[0]	in	RXD0	Receive data channel 0
TXD[1]	out	TXD0	Transmit data channel 1
CTS[1]	out	TXEN	Transmit enable channel 1
TXCLK[1]	in	TXCLK	Transmit clock channel 1
RXER[1]	in	RXER	Receive error channel 1
RXCLK[1]	in	RXCLK	Receive clock channel 1
RXDV[1]	in	RXDV	Receive data valid channel 1
RXD[1]	in	RXD0	Receive data channel 1

8.6. Test Interface

The Test Interface supports the manufacturing test and characterization of the chip. In the application environment test pins have to be connected as following:

STEST, FTEST, FIDIS: connect to VSS
TTEST: connect to VDD

Warning: Any other connection of these pins may cause permanent damage to the device and to additional devices of the application.

8.7. LED Signals

The LED port consists of three pins. Via the MEDL each of these pins can be independently configured for any of the three modes of operation. At Power-Up and after Reset the LED port is inactive and only weak pull-down resistors are connected. After the controller is switched on by the host and when it is processing its initialization, the LED port is initialized to the selected mode of operation.

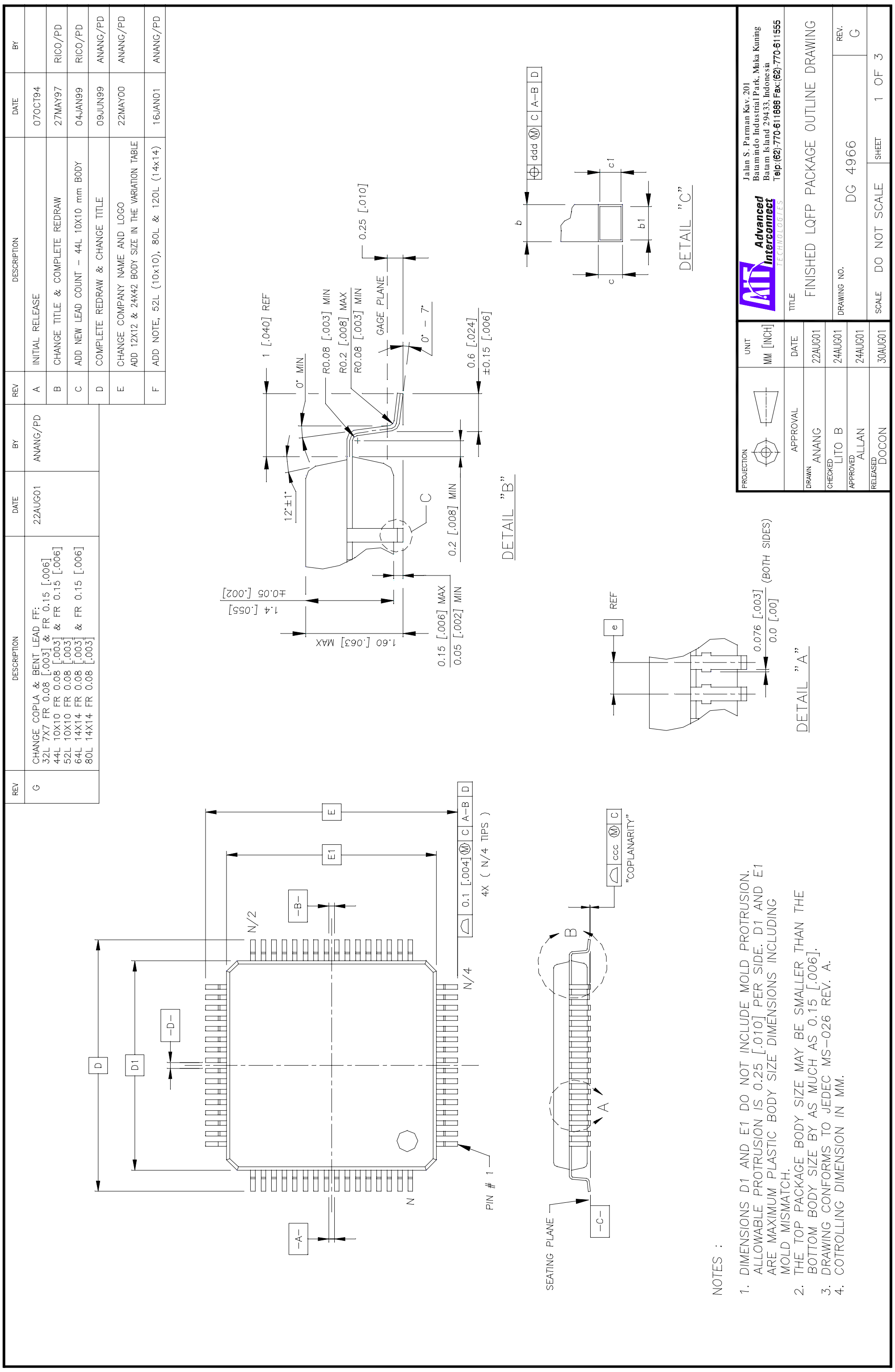
Pin Name	Protocol Mode	Timing Mode	Bus Guardian Mode
LED2	RPV[1] or Protocol activity[7]	Time Overflow[2]	Action Time[4]
LED1	Sync Valid[8]	Time Tick[2]	BDE1[5]
LED0	Protocol activity[6] or RPV[7]	Microtick[3]	BDE0[5]

Note 1: RPV is Remote Pin Voting. RPV is a network-wide agreed signal used typically for agreed power-up or power-down of the application's external drivers.
Note 2: Time Overflow is active for one clock cycle at the event of an overflow of the internal 16-bit time counter. Time Tick is active for one clock cycle when the internal time is counted up. Time Overflow and Time Tick can be used to externally clone the internal time control unit (TCU). With this information the application can precisely sample and trigger events, for example.
Note 3: Microtick is the internal main clock signal.
Note 4: Action Time signals the start of a bus access cycle.
Note 5: BDE0 and BDE1 show the Bus Guardian's activity, '1' signals an activated transmitter gate on the respective channel.
Note 6: Protocol activity is typically connected to an optical LED. The flashing frequency and rhythm give a simple view to the internal TTP protocol state.
Note 7: LED2's RPV mode and LED0's Protocol activity mode can be swapped with a MEDL parameter.
Note 8: The controller sets this output when cluster synchronization is achieved (after integration from the LISTEN state, after acknowledge in the COLDSTART state).

Each LED pin can be configured to be either a push/pull driver (drives both LOW and HIGH) or to be only an open-drain output (drives only LOW).

9. Package

Type: LQFP80



austriamicrosystems TTChip

SYMBOL	14x14												20x20			24x24		
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
D	15.8	16	16.2	15.8	16	16.2	15.8	16	16.2	15.8	16	16.2	21.8	22	22.2	25.8	26	26.2
	.622	.630	.638	.622	.630	.638	.622	.630	.638	.622	.630	.638	.858	.866	.874	1.016	1.024	1.032
D1	13.9	14	14.1	13.9	14	14.1	13.9	14	14.1	13.9	14	14.1	19.9	20	20.1	23.9	24	24.1
	.547	.551	.555	.547	.551	.555	.547	.551	.555	.547	.551	.555	.783	.787	.791	.941	.945	.949
E	15.8	16	16.2	15.8	16	16.2	15.8	16	16.2	15.8	16	16.2	21.8	22	22.2	25.8	26	26.2
	.622	.630	.638	.622	.630	.638	.622	.630	.638	.622	.630	.638	.858	.866	.874	1.016	1.024	1.032
E1	13.9	14	14.1	13.9	14	14.1	13.9	14	14.1	13.9	14	14.1	19.9	20	20.1	23.9	24	24.1
	.547	.551	.555	.547	.551	.555	.547	.551	.555	.547	.551	.555	.783	.787	.791	.941	.945	.949
b	0.3	0.37	0.45	0.22	0.32	0.38	0.17	0.22	0.27	0.13	0.18	0.23	0.17	0.22	0.27	0.17	0.22	0.27
	.012	.015	.018	.009	.013	.015	.007	.009	.011	.005	.007	.009	.007	.009	.011	.007	.009	.011
b1	0.3	0.35	0.4	0.22	0.3	0.33	0.17	0.2	0.23	0.13	0.16	0.19	0.17	0.2	0.23	0.17	0.2	0.23
	.012	.014	.016	.009	.012	.013	.007	.008	.009	.005	.006	.007	.007	.008	.009	.007	.008	.009
c	0.09		0.2	0.09		0.2	0.09		0.2	0.09		0.2	0.09		0.2	0.09		0.2
	.004		.008	.004		.008	.004		.008	.004		.008	.004		.008	.004		.008
c1	0.09		0.16	0.09		0.16	0.09		0.16	0.09		0.16	0.09		0.16	0.09		0.16
	.004		.006	.004		.006	.004		.006	.004		.006	.004		.006	.004		.006
e		0.8			0.65			0.5			0.4			0.5			0.5	
		.031			.026			.020			.016			.020			.020	
ccc		0.10			0.10			0.08			0.08			0.08			0.08	
		.004			.004			.003			.003			.003			.003	
ddd		0.20			0.13			0.08			0.07			0.08			0.08	
		.008			.005			.003			.003			.003			.003	
N		64			80			100			120			144			176	
N/2		32			40			50			60			72			88	
N/4		16			20			25			30			36			44	
		G			G													

PROJECTION	UNIT: MM [INCH]	Advanced Interconnect Technologies — Jalan S. Parman Kav. 201, Batamindo Industrial Park, Muka Kuning, Batam Island 29433, Indonesia. Telp:(62)-770-611686 Fax:(62)-770-611555
APPROVAL	DATE	TITLE: FINISHED LQFP PACKAGE OUTLINE DRAWING
DRAWN ANANG	22AUG01	
CHECKED LITO B	24AUG01	DRAWING NO. DG 4966 — REV. G
APPROVED ALLAN	24AUG01	
RELEASED DOCON	30AUG01	SCALE: DO NOT SCALE — SHEET 3 OF 3

10. Ordering Information and Support

Part Number: AS8202NF
Part Name: TTP-C2NF Communication Controller
Package: LQFP80

Please contact one of the following austriamicrosystems sales offices for further assistance:

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11. Related Products

Software tools, hardware development boards, evaluation systems and extensive support on TTP system integration as well as consulting are provided by:

TTChip Entwicklungsgesellschaft mbH
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Web: www.tttech.com

Appendix

Feature Comparison

Feature	C2 AS8202	C2NF AS8202NF
Conformance with TTP Specification Version 1.0.	yes	yes
TTP controller	RISC CPU (PCU)	RISC CPU (PCU)
Firmware on Chip	yes (Flash)	no[1]
Data load phase at power-on	no (MEDL in Flash)	yes (MEDL in RAM)
Interface to TTP Physical Layer	- asynch. - synch.(MII)	- asynch. - synch.(MII)
TTP Bus data coding (asynchronous interface)	MFM	MFM Manchester
IFG (Inter Frame Gap)	45µs	23µs
Interface to Host CPU	16 Bit	16 Bit
Supported Host CPU Bus Type	Intel	Intel
Host CPU access speed (without “read ahead”)	<250ns	<150ns (Intel)
Read ahead / Posted write	no	yes (access time <100ns)
CNI-RAM configuration	fixed	configurable (4kB to 28kB in 4kB steps)
MEDL check method	one CRC (firmware)	„block“ CRC (firmware)
Instruction RAM (I-RAM) check Method	once (firmware)	Parity Bit (+firmware)
Support for X-Frames	yes	yes
Baudrate on TTP Bus asynchronous mode synchronous mode	 up to 5MBd 25MBd	 up to 5MBd up to 25MBd
Process	0,35µ CMOS+Flash	0,35µ CMOS
SRAM	12kByte	40kByte
ROM	8kByte	32kByte[1]
Flash	32kByte	-
Power supply	3,3V	3,3V
Temperature range (°C)	0 to +70	-40 to +125
Package	LQFP80	LQFP80

Note 1: The chip is designed to allow inclusion of a stable protocol code (or customized protocol code) into the ROM by changing the ROM mask in the production process. This would eliminate the need of loading the protocol firmware code into the instruction code RAM.

List of Application Notes

The following is a list of the public application notes of the AS8202NF:

- AN123 Host Read Access Speedup in AS8202NF
- AN134 Reception scheme changed for ignoring IFG traffic during synchronized operation
- AN136 Changed Transformer Noise Tolerance in Manchester Mode in AS8202NF
- AN145 TTP Protocol Binary Release 2.04 for the AS8202NF Controller

The following application notes are **obsolete** for this data sheet:

- AN133 TTP Protocol Binary Release 1.02 for the AS8202NF Controller
- AN139 TTP Protocol Binary Release 2.02 for the AS8202NF Controller
- AN140 TTP Protocol Binary Release 2.03 for the AS8202NF Controller

List of Known Bugs

The following is a list of the known bugs of the AS8202NF.

1. AS8202NF RX001 Receiver Bug

TTP requires a maximum level of error detection on the physical layer as well as on the semantic layer for a received message. Among others the AS8202NF has a built-in ability to detect frames that are shorter or longer than expected. This feature does not correctly work for all situations with MFM and Manchester encoding. Frames that are too short or too long can appear to have the correct size. In this case the CRC check invalidates the frame. This bug is reported as bug report AN120.

The following bug reports apply to firmware versions prior to 2.02 and are **obsolete** for this data sheet:

- AN130 Manchester Decoding Bug
- AN132 AS8202/AS8202NF MFM/MII Async Reception Bug

Document Revision History

Revision	Date	Modification	Author
0.1	Dec. 17, 2002	Initial release	Matthias Wächter, Rastislav Hindak
0.2	Dec. 18, 2002	a) Updated austriamicrosystems' logo (front page and header on each page). b) The expected maximum current is now 95 mA instead of 65 mA. The actual tested limits will be given by austriamicrosystems after the first test runs.	Matthias Wächter
0.3	Jan. 9, 2003	a) "HBM: R=1.5KOhm, C=100pF" changed to "HBM: 1KV Mil.std.883, Method 3015.7" b) Operating Supply Current changed to: Imin=- , Imax=~90mA (TBD) c) Soldering Temperature changed from 260C to 235C d) Updated austriamicrosystems' logo (front page and header on each page). e) Updated input current values	Rastislav Hindak
0.4	Jan. 20, 2003	Feature Comparison AS8202 <-> AS8202NF added	Rastislav Hindak
0.4.5	Feb. 3, 2003	CEB, OEB to READYB (Read Access Time) – min. = 1 Tc changed to 1.5 Tc (37.5 ns) Asynchronous and synchronous definition of READYB signal changed.	Rastislav Hindak
0.5	Feb. 5, 2003	Renamed TXPADSOFF pin with TTEST, removed all TXPADSOFF feature description. Synchronous READYB generation added.	Matthias Wächter Rastislav Hindak
0.6	Feb. 10, 2003	Added timing for synchronous READYB Figure 3. & 4. updated	Matthias Wächter Rastislav Hindak

Revision	Date	Modification	Author
		Added max. current for weak-pull input/bidir pads Redraw tables, removed typos Updated Host Access inactivity time	
0.7	Mar. 13, 2003	Input currents at XIN and XOUT updated	Rastislav Hindak
0.8	Mar. 14, 2003	Note 2 on page 7 changed from “Values not tested, guaranteed by design” to “Typical value, not tested during production”. Supply voltage slope updated.	Rastislav Hindak
	Apr. 3, 2003	Appendix – Bug List added Updated protocol code handling Removed oscillator driving at XOUT	Rastislav Hindak Matthias Wächter
0.9	Apr. 8, 2003	DC Electrical Characteristics: TTL Input Pins and TTL Bidirectional Pins in Input/Tristate Mode & Outputs and TTL Bidirectional Pins in Output Mode updated, Transition times added, Note 3 added. Integrated Power-On Reset – supply voltage slope: Note 1 added. Host Read Access Inactivity drawing added.	Rastislav Hindak
1.0	Apr. 16, 2003	DC Electrical Characteristics: Outputs and TTL Bidirectional Pins in Output Mode: Cload changed from 40 pF to 35 pF. Oscillator circuitry: oscillation margins added.	Rastislav Hindak
	Apr. 24, 2003	DC Electrical Characteristics: Outputs and TTL Bidirectional Pins in Output Mode: Parameter Output Low/High Voltage removed. Asynchronous DPRAM interface: common note added.	Rastislav Hindak
	May 23, 2003	Added note for clock requirement when using external oscillator and internal PLL	Matthias Wächter
	Aug. 6, 2003	Updated for Protocol V1.02 functionality, updated LED functionality according to protocol, added references to all existing public application notes and bug reports	Matthias Wächter
	Aug. 21, 2003	Substitute “TTP “ for “TTP/C”, add contact page, minor changes in wording and formatting	Bernhard Wenzl
	Aug. 25, 2003	Minor changes in wording and formatting	Matthias Wächter
1.1	Oct. 01, 2003	Figure 4.: Read Access Timing (CEB & OEB Controlled) updated. Timing of Asynchronous DPRAM interface updated (Symbol: 1b, 2b, 6, 11 (changed to 11a, 11b, 11c) and 15.	Rastislav Hindak
	Oct. 23, 2003	Added Input Capacitance Cin for Input pins Updated values for 11a, 11b Updated data sheet, app notes, for protocol version 2.02	Matthias Wächter
1.2	Nov. 05, 2003	Updated data sheet, app notes for protocol version 2.03	Matthias Wächter
1.3	May 07, 2004	Updated app notes for protocol version 2.04	Matthias Wächter
1.4	Jul. 15, 2005	Updated access inactivity times	Matthias Wächter

