19-2049; Rev 0; 5/01

MAXIM

Dual-Audio, Log Taper Digital Potentiometers

General Description

The MAX5408/MAX5409 are dual logarithmic taper digital potentiometers with 32-tap points each. The MAX5408 is a dual potentiometer with one wiper per potentiometer. The MAX5409 is a dual potentiometer with two wipers per potentiometer (see *Functional Diagram*). An SPI™-compatible serial interface controls the wipers. The MAX5408/MAX5409 have a factory-set resistance of 10kΩ per potentiometer. A zero-crossing detect feature minimizes the audible noise generated by wiper transitions. These devices are ideal for audio applications requiring digitally controlled resistors. The MAX5408/MAX5409 have nominal resistor temperature-coefficients of 35ppm/°C end-to-end and 5ppm/°C ratiometric. The MAX5408/MAX5409 are available in 16-pin QSOP and 16-pin QFN packages and are specified over the extended temperature range (-40°C to +85°C).

Applications

Stereo Volume Control

Fading and Balancing Stereo Signals

Mechanical Potentiometer Replacement

SPI is a trademark of Motorola Inc.

Functional Diagram appears at end of data sheet.

Features

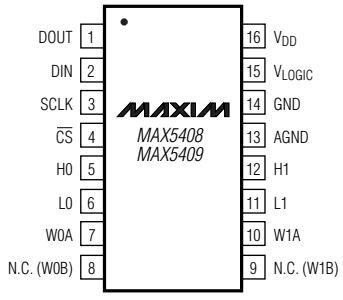
- **Log Taper with 2dB Steps Between Taps**
- **32-Tap Positions for Each Wiper**
- **Small 16-Pin QSOP/QFN Packages**
- **+2.7V to +3.6V Single-Supply Operation**
- **Low 1µA Supply Current**
- **Zero-Crossing Detection for Clickless Switching**
- **Mute Function to -90dB**
- **10kΩ Fixed Resistance Value**
- **3-Wire SPI-Compatible Serial Data Interface**
- **Power-On Reset: Wiper Goes to Maximum Attenuation**
- **Digital Output for Readback and Daisy-Chaining Capabilities**

Ordering Information

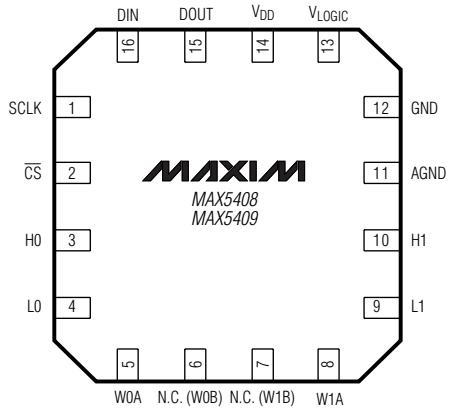
PART	TEMP. RANGE	PIN-PACKAGE	WIPERS PER RESISTOR
MAX5408EEE	-40°C to +85°C	16 QSOP	1
MAX5408EGE	-40°C to +85°C	16 QFN	1
MAX5409EEE	-40°C to +85°C	16 QSOP	2
MAX5409EGE	-40°C to +85°C	16 QFN	2

Pin Configurations

TOP VIEW



QSOP
(5mm x 6mm)



( ) ARE FOR MAX5409 ONLY

QFN
(4mm x 4mm)

Dual-Audio, Log Taper Digital Potentiometers

ABSOLUTE MAXIMUM RATINGS

V_{DD}, V_{LOGIC}, $\overline{CS}$, SCLK, DIN to GND .....-0.3V to +6V
H_, L_, and W_ to GND .....-0.3V to (V_{DD} + 0.3V)
DOUT to GND.....-0.3V to (V_{DD} + 0.3V)
AGND to GND .....-0.3V to +0.3V
Input and Output Latchup Immunity.....±200mA
Maximum Continuous Current into H_, L_, and W_.....±500µA

Continuous Power Dissipation (T_A = +70°C)
QSOP (derate 8.3mW/°C above +70°C).....666.7mW
QFN (derate 18.5mW/°C above +70°C) 1481mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-60°C to +150°C
Maximum Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +3.6V, $V_{H\_}$ = V_{LOGIC}, $V_{L\_}$ = 0, T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
End-to-End Resistance			7	10	13	Ω
Maximum Bandwidth			100			kHz
Absolute Tolerance				±0.25		dB
Tap-to-Tap Tolerance				±0.1		dB
Total Harmonic Distortion	THD	V_{IN} = 1V_{RMS}, f = 1kHz, tap = -6dB		0.002		%
Channel Isolation				-100		dB
Interchannel Matching		f = 20Hz to 20kHz, tap = -6dB		±0.5		dB
Mute Attenuation				-90		dB
Power-Supply Rejection Ratio	PSRR			-80		dB
Wiper Resistance	R_W			1000	1700	Ω
Wiper Capacitance	C_W			10		pF
Digital Clock Feedthrough		f_{SCLK} = 20Hz to 20kHz, tap = -6dB		-90		dB
End-to-End Resistance Tempco	TC_R			35		ppm/°C
Ratiometric Resistance Tempco				5		ppm/°C
DIGITAL INPUTS (V_{LOGIC} > 4.5V)						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Leakage Current					±1	µA
Input Capacitance				5		pF
DIGITAL INPUTS (V_{LOGIC} < 4.5V)						
Input High Voltage	V_{IH}		0.7 x V_{LOGIC}			V
Input Low Voltage	V_{IL}				0.3 x V_{LOGIC}	V
Input Leakage Current					±1	µA
Input Capacitance				5		pF
DIGITAL OUTPUT						
Output High Voltage	V_{OH}	I_{SOURCE} = 0.5mA	V_{LOGIC} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA			0.4	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +3.6V, $V_{H\_}$ = V_{LOGIC}, $V_{L\_}$ = 0, T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (Figure 1)						
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Fall to DOUT Valid Propagation Delay	t_{DO}	C_{LOAD} = 200pF			80	ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns
Wiper Settling Time	t_{IW}	Zero-Crossing Detect disabled		1		µs
POWER SUPPLIES						
Supply Voltage	V_{DD}		2.7		3.6	V
Active Supply Current	I_{DD}	f_{SCLK} = 2MHz, (Note 1)			100	µA
Standby Supply Current		(Note 2)		0.2	10	
Logic Supply Voltage	V_{LOGIC}		2.7		5.5	V
Logic Active Supply Current	I_{LOGIC}	f_{SCLK} = 2MHz, DOUT = floating (Note 3)			120	µA
Logic Standby Supply Current		DOUT = floating (Note 2)		1	10	

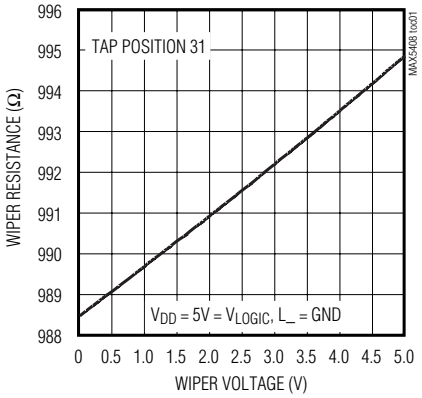
Note 1: Supply current measured while changing, wiper position with zero-crossing enabled.
Note 2: Supply current measured while wiper position is fixed.
Note 3: Supply current measured changing wiper position.

Dual-Audio, Log Taper Digital Potentiometers

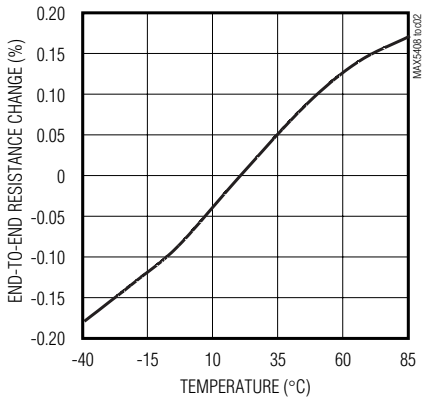
Typical Operating Characteristics

(V_{DD} = 5V, T_A = +25°C, unless otherwise specified)

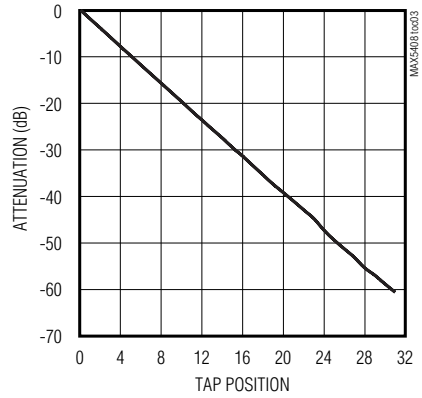
WIPER RESISTANCE vs. WIPER VOLTAGE



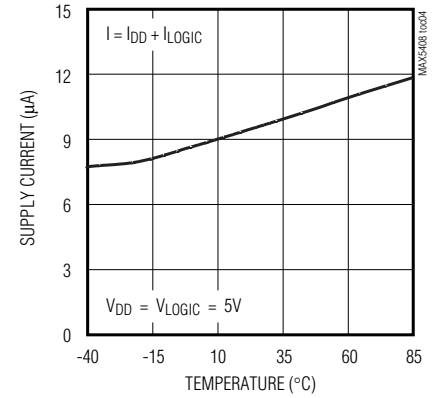
END-TO-END RESISTANCE % CHANGE vs. TEMPERATURE



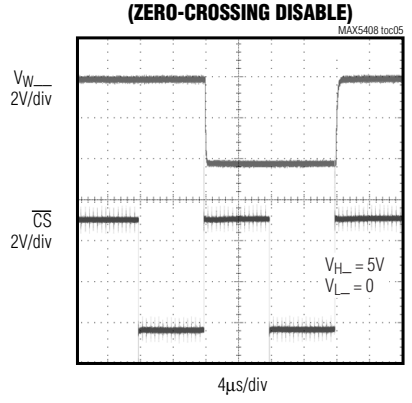
ATTENUATION vs. TAP POSITION



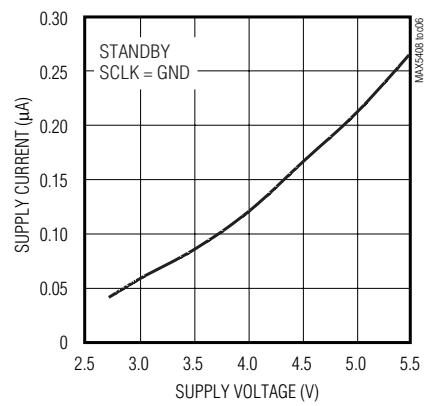
SUPPLY CURRENT vs. TEMPERATURE



TAP-TO-TAP SWITCHING TRANSIENT (ZERO-CROSSING DISABLE)



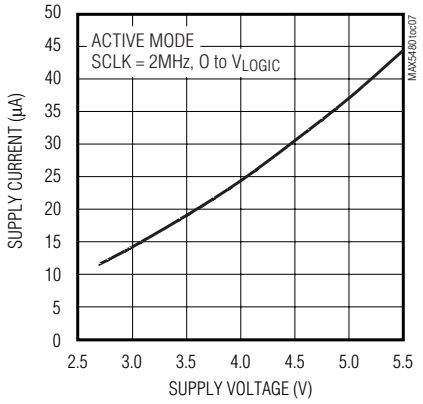
LOGIC CURRENT vs. LOGIC VOLTAGE



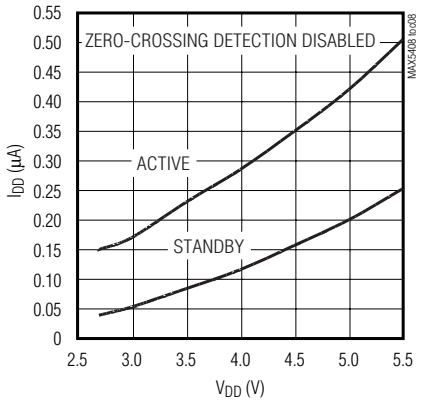
Typical Operating Characteristics (continued)

(V_{DD} = 5V, T_A = +25°C, unless otherwise specified)

LOGIC CURRENT vs. LOGIC VOLTAGE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



Pin Description

PIN				NAME	FUNCTION
MAX5408 QFN	MAX5408 QSOP	MAX5409 QFN	MAX5409 QSOP		
1	3	1	3	SCLK	Serial Data Clock Input
2	4	2	4	$\overline{CS}$	Chip Select for Wiper Control
3	5	3	5	H0	High Terminal of Resistor 0
4	6	4	6	L0	Low Terminal of Resistor 0
5	7	5	7	W0A	Wiper Terminal A of Resistor 0
—	—	6	8	W0B	Wiper Terminal B of Resistor 0
—	—	7	9	W1B	Wiper Terminal B of Resistor 1
8	10	8	10	W1A	Wiper Terminal A of Resistor 1
9	11	9	11	L1	Low Terminal of Resistor 1
10	12	10	12	H1	High Terminal of Resistor 1
11	13	11	13	AGND	Analog Ground
12	14	12	14	GND	Ground
13	15	13	15	V_{LOGIC}	Power Supply for Interface Logic
14	16	14	16	V_{DD}	Power Supply for Wiper Switches
15	1	15	1	DOUT	Serial Data Out
16	2	16	2	DIN	Serial Data In
6, 7	8, 9	—	—	N.C	Not Connected

Table 1. Serial Interface Programming Commands for MAX5408

8-BIT SERIAL WORD				FUNCTION
A0	A1	A2	D4–D0	
0	0	0	5-bit DAC Data	Program position of wiper W0A
0	0	1	5-bit DAC Data	Undefined
0	1	0	5-bit DAC Data	Program position of wiper W1A
0	1	1	5-bit DAC Data	Undefined
1	0	0	4-bit Mute Data, D0 = “don’t care”	Data for mute register (see Table 3)
1	0	1	4-bit Zero-Crossing Detection Data, D0 = “don’t care”	Data for zero-crossing detection register (see Table 5)
1	1	0	00000	Return wiper register for W0A
1	1	0	00001	Undefined
1	1	0	00010	Return wiper register for W1A
1	1	0	00011	Undefined
1	1	0	00100	Return mute register
1	1	0	00101	Return zero-crossing detection register
1	1	1	D4 = 0, D3–D0 = “don’t care	Analog power-down
1	1	1	D4 = 1, D3–D0 = “don’t care”	Analog power-up

Detailed Description

Digital Serial Interface

An SPI-compatible serial interface controls the MAX5408/MAX5409. The input word to the device is eight bits long, composed of three address bits (A0, A1, and A2), followed by five data bits, with MSB first (see Tables 1 and 2). The first three address bits set the value of internal registers. The five data bits control the wiper position. For certain commands, some of the five data bits are “don’t cares”, but must be sent to the device.

The serial data is listed in Tables 1 and 2.

The control code determines:

- Potentiometer to update or register to set.
- Data for mute register (Tables 3 and 4).
- Data for zero-crossing detection register (Tables 5 and 6).

The data bits control the position of the wiper (Table 7). A logic low on the chip-select input ($\overline{CS}$) enables the device’s serial interface. A logic high on $\overline{CS}$ disables the interface control circuitry. See Figure 1 for serial-interface timing description.

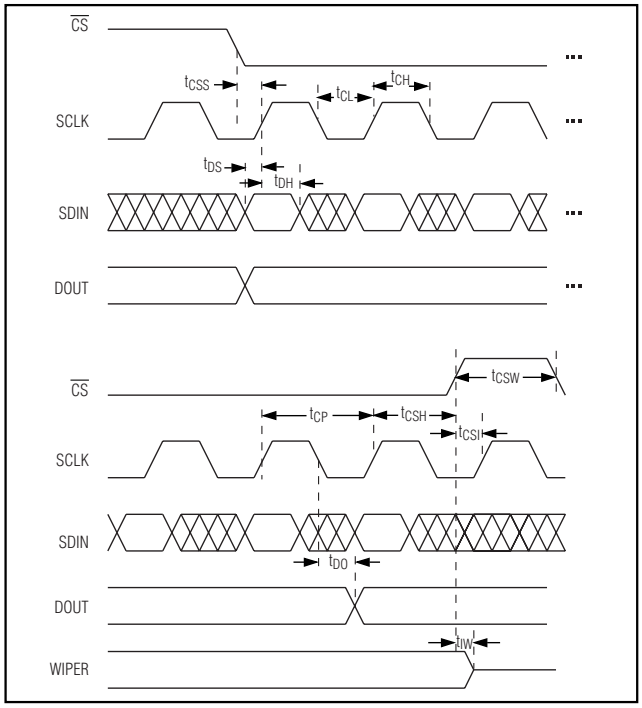


Figure 1. Serial Timing Diagram

Table 2. Serial Interface Programming Commands for MAX5409

8-BIT SERIAL WORD				FUNCTION
A0	A1	A2	D4–D0	
0	0	0	5-bit DAC Data	Program position of wiper W0A
0	0	1	5-bit DAC Data	Program position of wiper W0B
0	1	0	5-bit DAC Data	Program position of wiper W1A
0	1	1	5-bit DAC Data	Program position of wiper W1B
1	0	0	4-bit Mute Data, D0 = “don’t care”	Data for mute register (see Table 4)
1	0	1	4-bit Zero-Crossing Detection Data, D0 = “don’t care”	Data for zero-crossing detection register (see Table 6)
1	1	0	00000	Return wiper register for W0A
1	1	0	00001	Return wiper register for W0B
1	1	0	00010	Return wiper register for W1A
1	1	0	00011	Return wiper register for W1B
1	1	0	00100	Return mute register
1	1	0	00101	Return zero-crossing detection register
1	1	1	D4 = 0, D3–D0 = “don’t care	Analog power-down
1	1	1	D4 = 1, D3–D0 = “don’t care”	Analog power-up

Table 3. Mute Register Bit Definitions for MAX5408

DATA BIT	VALUE	FUNCTION
D4	0	Set wiper W0A to preprogrammed value (-62dB on power-up)
	1	Set wiper W0A to L0
D3	“don’t care”	Undefined
D2	0	Set wiper W1A to preprogrammed value (-62dB on power-up)
	1	Set wiper W1A to L0
D1	“don’t care”	Undefined
D0	“don’t care”	Undefined

Table 4. Mute Register Bit Definitions for MAX5409

DATA BIT	VALUE	FUNCTION
D4	0	Set wiper W0A to preprogrammed value (-62dB on power-up)
	1	Set wiper W0A to L0
D3	0	Set wiper W0B to preprogrammed value (-62dB on power-up)
	1	Set wiper W0B to L0
D2	0	Set wiper W1A to preprogrammed value (-62dB on power-up)
	1	Set wiper W1A to L1
D1	0	Set wiper W1B to preprogrammed value (-62dB on power-up)
	1	Set wiper W1B to L1
D0	“don’t care”	Undefined

Table 5. Zero-Crossing Detection Register Bit Definitions for MAX5408

DATA BIT	VALUE	FUNCTION
D4	0	Disable wiper W0A zero-crossing detection circuit
	1	Enable wiper W0A zero-crossing detection circuit
D3	"don't care"	Undefined
D2	0	Disable wiper W1A zero-crossing detection circuit
	1	Enable wiper W1A zero-crossing detection circuit
D1	"don't care"	Undefined
D0	"don't care"	Undefined

Table 6. Zero-Crossing Detection Register Bit Definitions for MAX5409

DATA BIT	VALUE	FUNCTION
D4	0	Disable wiper W0A zero-crossing detection circuit
	1	Enable wiper W0A zero-crossing detection circuit
D3	0	Disable wiper W0B zero-crossing detection circuit
	1	Enable wiper W0B zero-crossing detection circuit
D2	0	Disable wiper W1A zero-crossing detection circuit
	1	Enable wiper W1A zero-crossing detection circuit
D1	0	Disable wiper W1B zero-crossing detection circuit
	1	Enable wiper W1B zero-crossing detection circuit
D0	"don't care"	Undefined

Table 7. Attenuation and Wiper Position

POSITION	OUTPUT LEVEL (dB)
0	0
1	-2
2	-4
3	-6
4	-8
⋮	⋮
30	-60
31	-62
MUTE	<-90

The digital output, DOUT, lags the digital input signal, DIN by 8.5 clock cycles. Force $\overline{CS}$ high to disable DOUT, placing DOUT in three-state mode. Force $\overline{CS}$ low to enable DOUT and disable three-state mode.

Force $\overline{CS}$ high, after a word has been written to the MAX5408/MAX5409 to make a readback request. The next $\overline{CS}$ low period writes the requested data to DOUT.

A readback request overwrites any previous data in the shift register. Note that the data appears at DOUT in the order: A0, A1, A2, D4, D3, D2, D1, D0. A0 will be available after the first high-to-low transition of SCLK when $\overline{CS}$ is low. The input continues to load the shift register while data is being read out of the MAX5408/MAX5409. The input data appears at DOUT 8.5 clock cycles later. A $\overline{CS}$ transition from low-to-high latches the input data. For any control byte, the state of SCLK must be the same for both $\overline{CS}$ low-to-high transitions and $\overline{CS}$ high-to-low transitions, in order to preserve the data at DOUT while $\overline{CS}$ transitions.

Zero-Crossing Detection

The zero-crossing detection register enables the zero-crossing detect feature. The zero-crossing detect feature reduces the audible noise ("clicks and pops") that result from wiper transitions. The wiper changes position only when the voltage at L_ is the same as the voltage at H_. The MAX5408/MAX5409 timeout and change the wiper position, if after 50ms no zero-crossing is detected.

Power-On Reset

The power-on reset (POR) feature sets the wiper to the maximum attenuation (tap position 31, -62 dB) at power-up.

Mute Function

When mute is enabled, the wiper stays at its previous position. If a command to update the wiper position is issued when the device is in mute, the wiper will be set to its new position when mute is removed.

Applications Information

Attenuation Control

Figure 2 shows the application of an attenuation control. The op amps are connected in a follower configuration with a fixed gain. The digitally controlled potentiometer attenuates the input signal.

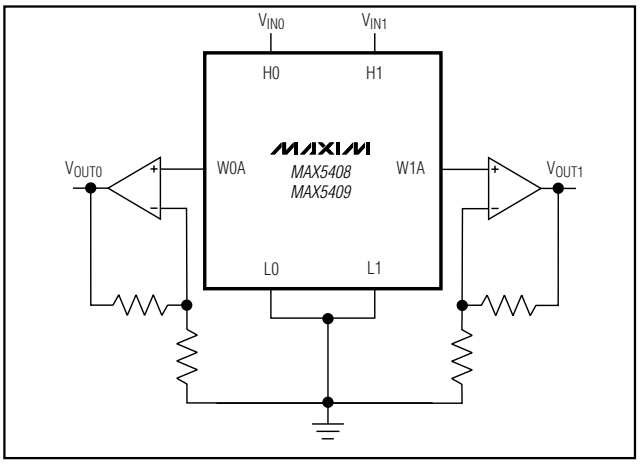


Figure 2. Attenuation Control

Stereo Volume Control

Figure 3 shows the application of stereo volume control. The op amps are connected in a follower configuration with fixed gain. The digitally controlled potentiometer attenuates the input signals. The second wiper of each potentiometer controls the signal amplitude at the rear set of speakers.

Daisy-Chaining

Figure 4 shows an application daisy-chaining the serial-interfaces of the MAX5408/MAX5409. A single-write command updates multiple devices from a single digital port in this configuration (see *Digital Serial Interface* section).

Gain Control

Figure 5 shows the application of a gain control. **Note:** Muting the potentiometer creates unpredictable behavior at the output of the op amp, and may seriously degrade the performance of the op amp.

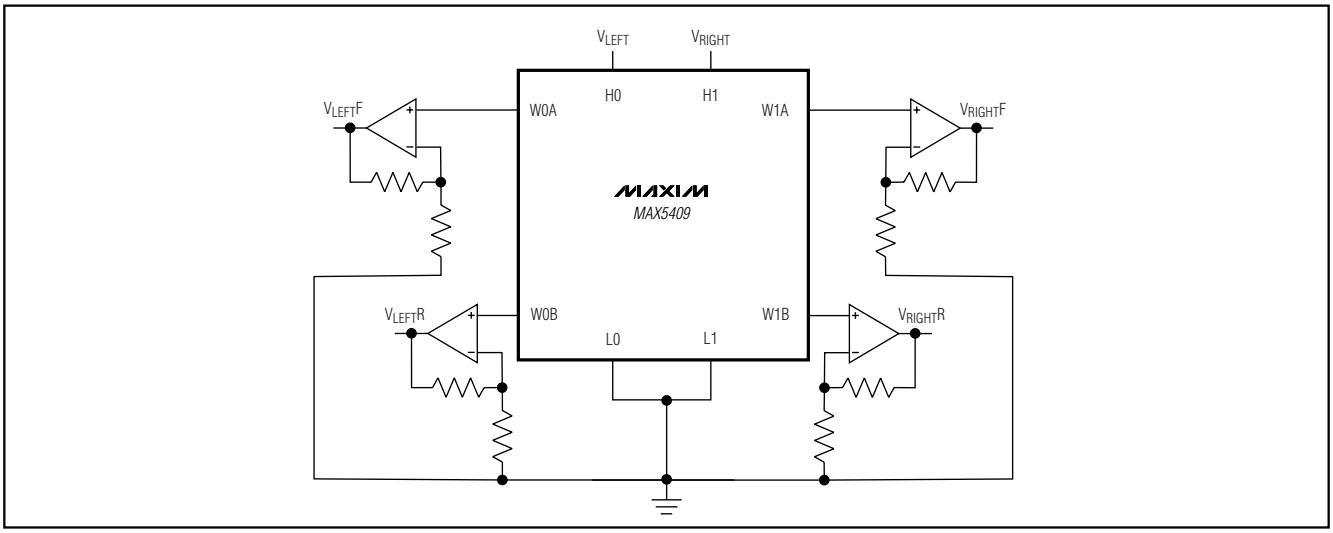


Figure 3. Stereo Volume Control with Front and Rear Fade

Dual-Audio, Log Taper Digital Potentiometers

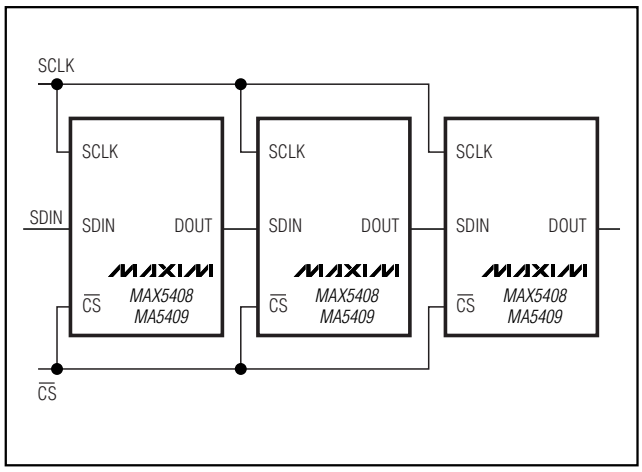


Figure 4. Daisy-Chaining of Serial Interfaces

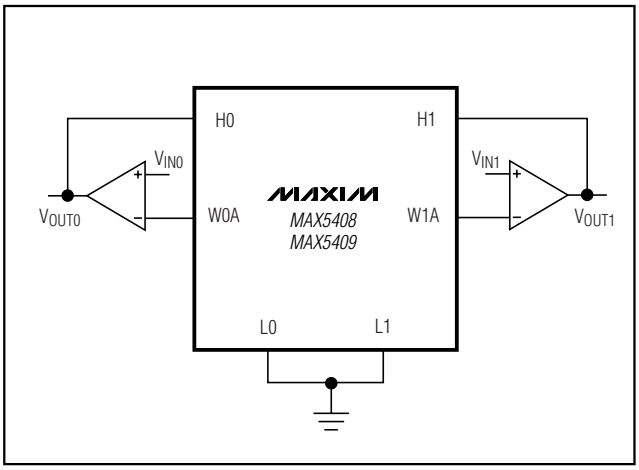


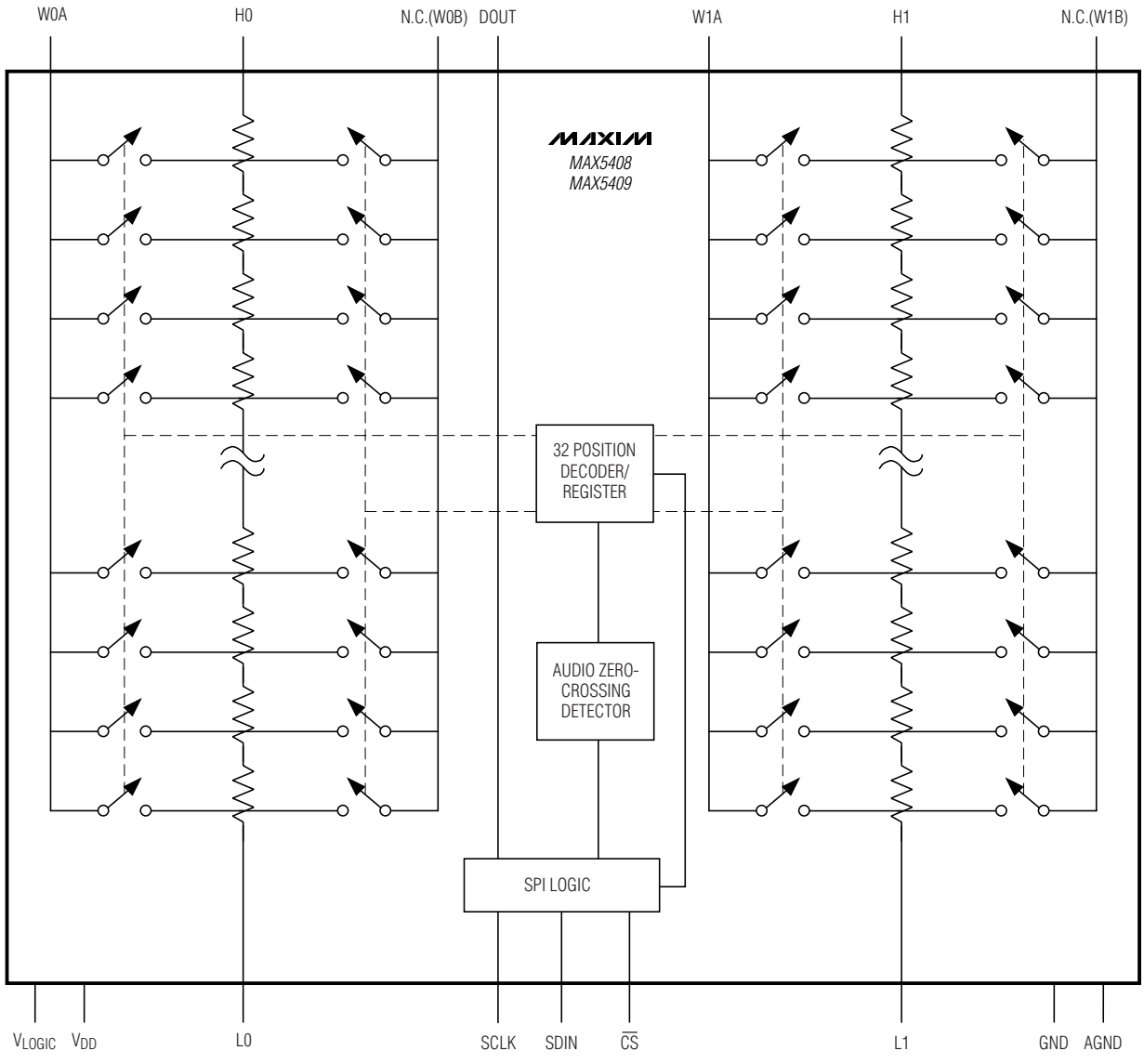
Figure 5. Gain Control

Chip Information

TRANSISTOR COUNT: 12759

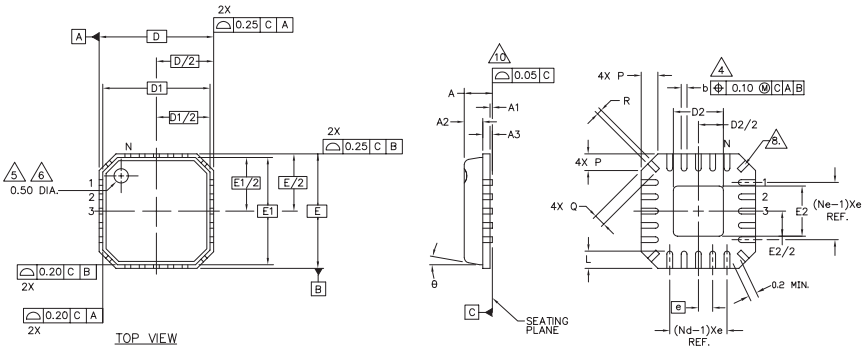
PROCESS: BiCMOS

Functional Diagram



Package Information

12, 16,20, 24L QFN.EPS



PROPRIETARY INFORMATION			
TITLE: PACKAGE OUTLINE, 12,16,20,24L QFN, 4x4x0.90 MM			
APPROVAL	DOCUMENT CONTROL NO. 21-0106	REV B	1/2

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM MUST TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. PACKAGE WARPAGE MAX 0.05mm.
10. APPLIED FOR EXPOSED PAD AND TERMINALS.
    EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
11. APPLIED ONLY FOR TERMINALS.
12. MEETS JEDEC MO220.

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	–	0.85	1.00	
A1	0.00	0.01	0.05	11
A2	–	0.65	0.80	
A3		0.20 REF.		
D		4.00 BSC		
D1		3.75 BSC		
E		4.00 BSC		
E1		3.75 BSC		
θ			12°	
P	0.24	0.42	0.60	
R	0.13	0.17	0.23	

SYMBOL	PITCH VARIATION A MIN.	NOM.	MAX.	NOTE	PITCH VARIATION B MIN.	NOM.	MAX.	NOTE	PITCH VARIATION C MIN.	NOM.	MAX.	NOTE	PITCH VARIATION D MIN.	NOM.	MAX.	NOTE
e	0.80 BSC				0.65 BSC				0.50 BSC				0.50 BSC			
N	12			3	16			3	20			3	24			3
Nd	3			3	4			3	5			3	6			3
Ne	3			3	4			3	5			3	6			3
L	0.50	0.60	0.75		0.50	0.60	0.75		0.50	0.60	0.75		0.30	0.40	0.55	
b	0.28	0.33	0.40	4	0.23	0.28	0.35	4	0.18	0.23	0.30	4	0.18	0.23	0.30	4
Q	0.30	0.40	0.65		0.30	0.40	0.65		0.30	0.40	0.65		0.00	0.20	0.45	
D2	SEE EXPOSED PAD VARIATION: A, B				SEE EXPOSED PAD VARIATION: A, B				SEE EXPOSED PAD VARIATION: A, B				SEE EXPOSED PAD VARIATION: A			
E2	SEE EXPOSED PAD VARIATION: A, B				SEE EXPOSED PAD VARIATION: A, B				SEE EXPOSED PAD VARIATION: A, B				SEE EXPOSED PAD VARIATION: A			

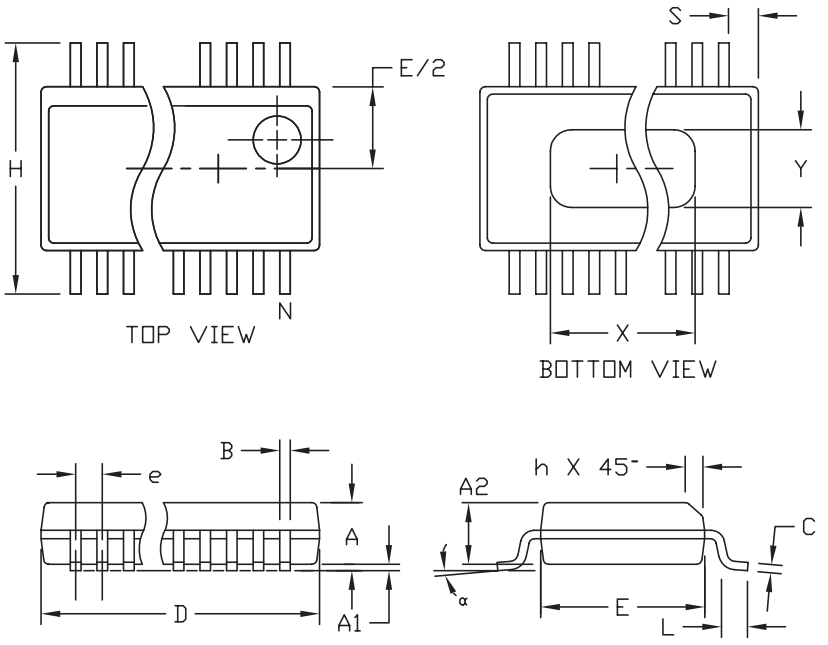
SYMBOLS		D2 MIN	D2 NOM	D2 MAX	E2 MIN	E2 NOM	E2 MAX	NOTE
EXPOSED PAD VARIATIONS	A	1.95	2.10	2.25	1.95	2.10	2.25	
	B	1.55	1.70	1.85	1.55	1.70	1.85	

EXAMPLE: WE CAN CALL VARIATION "BB" FOR 16 TERMINAL QFN WITH 1.70x1.70 mm NOMINAL EXPOSED PAD DIMENSION. THE FORMER ONE IN VARIATION IS FOR PITCH VARIATION AND THE LATTER ONE IS FOR EXPOSED PAD VARIATION.

PROPRIETARY INFORMATION			
TITLE: PACKAGE OUTLINE, 12,16,20,24L QFN, 4x4x0.90 MM			
APPROVAL	DOCUMENT CONTROL NO. 21-0106	REV B	2/2

Package Information (continued)

QSOP.EXP. PADS.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.084	.108	2.13	2.74
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.078	.102	1.98	2.59	EXPOSED PAD	

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. DIMENSIONS X AND Y APPLY ONLY TO EXPOSED PAD QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, QSOP, .150" EXPOSED PAD
APPROVAL | DOCUMENT CONTROL NO. 21-0112 | REV A | 1/1