Ordering number : ENN*5539

CMOS IC

LC866020/16/12/08C

8-Bit Single Chip Microcontroller with On-Chip 20/16/12/08K-Byte ROM and 384-Byte RAM

Preliminary

Overview

The LC866020C/16C/12C/08C microcontrollers are 8-bit single chip microcontrollers with the following on-chip functional blocks :

- CPU : Operable at a minimum bus cycle time of 0.5µs (microsecond)
- On-chip ROM maximum capacity : 20K bytes
- On-chip RAM capacity : 384 bytes
- VFD automatic display controller/driver
- 16-bit timer/counter (or two 8-bit timers)
- 16- bit timer/PWM (or two 8-bit timers)
- 4 channels 8-bit AD converter
- Two 8-bit synchronous serial interface circuits
- 14-source 10-level vectored interrupt system

All of the above functions are fabricated on a single chip.

Features

(1) Read-Only Memory (ROM) :

LC866020C	20480 × 8 bits
LC866016C	16384 × 8 bits
LC866012C	12288 × 8 bits
LC866008C	8192 × 8 bits

(2) Random Access Memory (RAM) : LC866020C/16C/12C/08C 384 × 8 bits

(3) Minimum bus cycle time : 0.5µs (using 12MHz CF resonator oscillation)
Bus cycle time means ROM-read period.

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TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

(4) Minimum instruction cycle time : 1μs (using 12MHz CF resonator oscillation)
ROM data is accessed twice in a instruction cycle time. The operation of the microcomputers herein is about 1.7 times that of LC66000 series, our products in the same specified cycle time.

(5) Ports
- Input/output ports : 2 ports (16 terminals)
- Input/output port programmable in nibble units : 1 port (8 terminals)
- Input/output port programmable in a bit : 1 port (8 terminals)
- Input ports : 2 ports (8 port pins)
- VFD output ports : 30 terminals
- Large current output for digit : 16 terminals
- Pull-down resistor option available

(6) VFD automatic display controller
- Segment/digit output pattern programmable
  Any segment/digit combination available
  VFD parallel-drive available
- 16-step dimmer function available

(7) AD converter
- 4-channels 8-bit AD converter

(8) Serial interface
- Two 8-bit serial-interface circuits
- LSB first/MSB first function available
- Internal 8-bit baud-rate generator in common with two serial-interface circuits

(9) Timers
- Timer0 : 16-bit timer / counter with 2-bit prescaler + 8-bit programmable prescaler
  Mode 0 : Two 8-bit timers with programmable prescaler
  Mode 1 : 8-bit timer with programmable prescaler + 8-bit counter
  Mode 2 : 16-bit timer with programmable prescaler
  Mode 3 : 16-bit counter
  The resolution of Timer0 is 1 tCYC, the cycle time.
- Timer1 : 16-bit timer / PWM
  Mode 0 : Two 8-bit timers
  Mode 1 : 8-bit timer + 8-bit PWM
  Mode 2 : 16-bit timer
  Mode 3 : Variable bit PWM (9 to 16 bits)
  In Mode 0 and Mode 1, the resolution of Timer1 and PWM is tCYC.
  In Mode 2 and Mode 3, the resolution is selectable by program ; tCYC or 1/2tCYC
- Base timer
  Every 500ms overflow system for a clock application (using 32.768kHz crystal oscillation for base timer clock)
  Every 976μs, 3.9ms, 15.6ms, 62.5ms overflow system (using 32.768kHz crystal oscillation for base timer clock)
  The base timer clock selectable, 32.768kHz crystal oscillation, system clock, and programmable prescaler output of Timer0.

(10) Buzzer output
- The buzzer sound frequency selectable ; 4kHz, 2kHz (using 32.768kHz crystal oscillation for timer clock)

(11) Remote control receiver circuit (connected to the P73/INT3/T0IN terminal)
- Noise rejection function
- Polarity switching

(12) Watchdog timer
- The watchdog timer is taken on RC outside.
- Watchdog timer operation selectable : interrupt system, system reset

(13) Interrupt system
- 14-source 10-level vectored interrupts :
  1. External interrupt INT0 (includes watchdog timer)
  2. External interrupt INT1
  3. External interrupt INT2, timer/counter T0L (Lower 8 bits)
  4. External interrupt INT3, base timer
  5. Timer/counter T0H (Upper 8 bits)
  6. Timer T1H /T1L
  7. Serial interface SIO0
  8. Serial interface SIO1
  9. AD converter
  10. VFD display controller, port 0
- Interrupt priority control available

  The interrupt priority control register included.

  These microcomputers allows 3-level interrupt ; low-level, high-level and highest-level of multiplex interrupt. It can specify a low-level or a high-level interrupt priority from INT2/T0L through VFD display controller/port 0 (the above interrupt number from 3 to 10).

  It can also specify a low-level or the highest-level interrupt priority to INT0 and INT1.

(14) Real-time service operation

The Real-Time Service (RTS) functions the data-transfer between the Special Function Registers at acknowledging the interrupt request.

The RTS starts within 1 cycle-time and completes within 5 cycle-times after occurring the interrupt request.

(15) Sub-routine stack levels
- 128 levels (Max.) : Stack area included in RAM area.

(16) Multiplication and division
- 16 bits × 8 bits (7 instruction cycle times)
- 16 bits ÷ 8 bits (7 instruction cycle times)

(17) 3 oscillation circuits
- On-chip RC oscillation circuit using for the system clock
- On-chip CF oscillation circuit using for the system clock
- On-chip X'tal oscillation circuit using for the system clock and for time-base clock

(18) Standby function
- HALT mode function

  The HALT mode is used to reduce the power dissipation. In this operation mode, the program execution is stopped. This operation mode can be released by the interrupt request signals or the system reset.
- HOLD mode function

  The HOLD mode is used to stop all the oscillations ; the RC (internal), CF and X'tal oscillations. This mode can be released by the following conditions.
  - Reset terminal ($\overline{RES}$) set to low level.
  - P70/INT0/T0IN, P71/INT1/T0IN terminals set to assigned level (programmable).
  - Port 0 terminal/terminals set to low level (programmable).

(19) Factory shipment

DIP64S delivery form

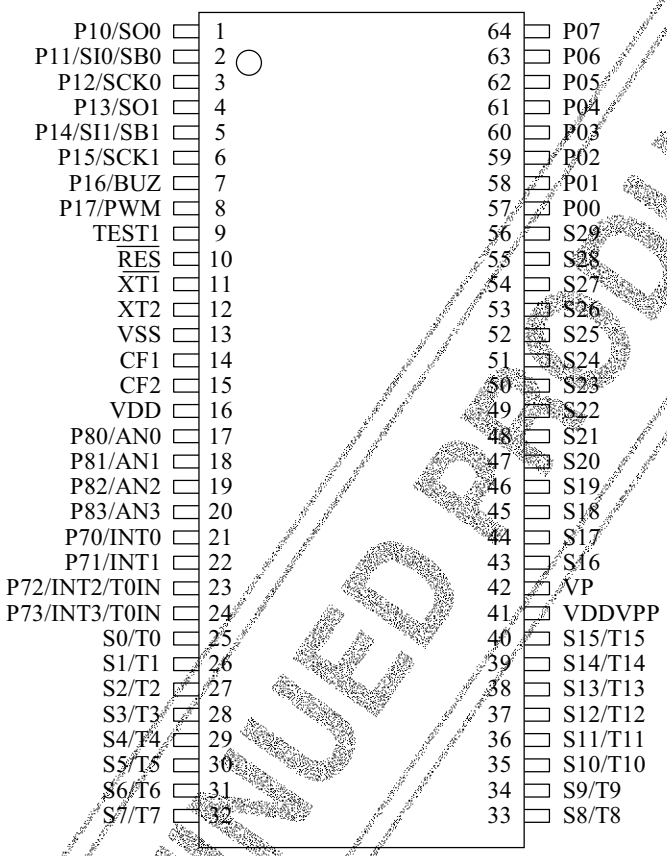
QFP64E delivery form

(20) Development Tools

- Evaluation chip : LC866098
- EPROM version : LC86E6032
- One time version : LC86P6032
- Emulator : EVA86000 + ECB866000 (Evaluation chip board)
  + POD866000 (Pod : DIP64S) / POD866010 (Pod : QIP64E)

Pin Assignment

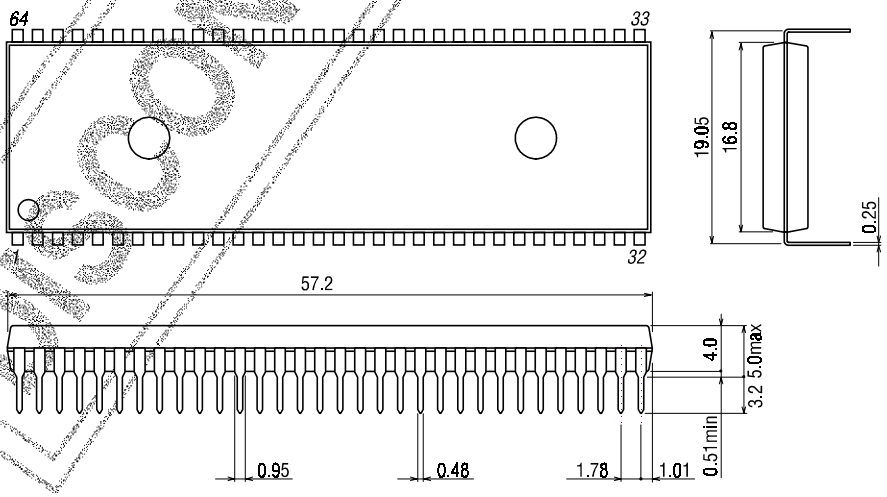
•DIP64S



Package Dimension

(unit : mm)

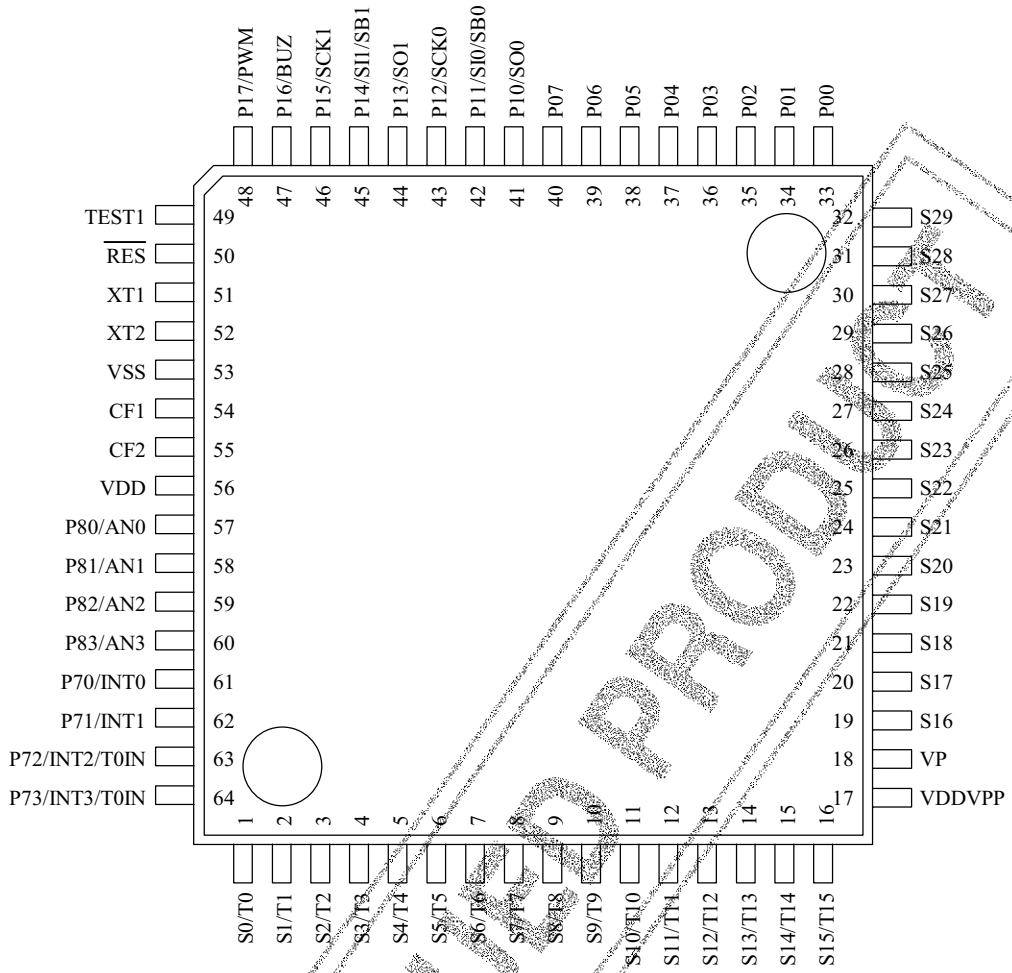
3071



SANYO : DIP-64S(750mil)

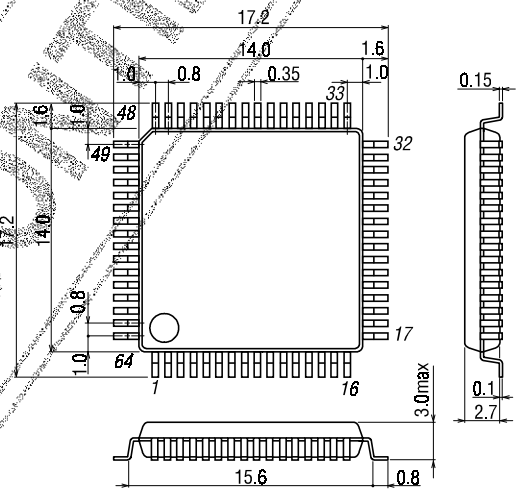
Pin Assignment

•QIP64E



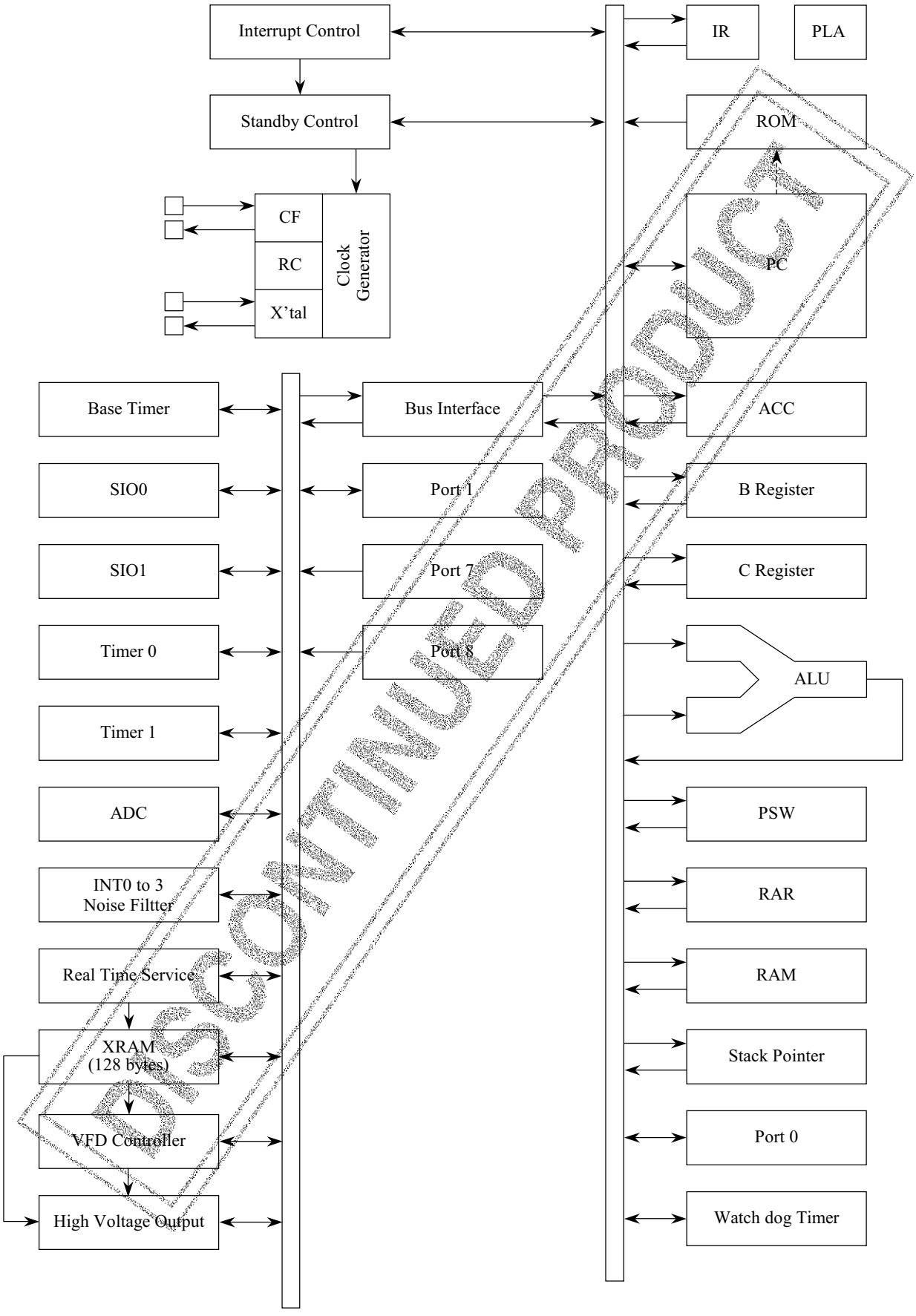
Package Dimension

(unit : mm)
3159



SANYO : QIP-64E

System Block Diagram



Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Functions</th><th>Option</th></tr>
<tr><td>VSS</td><td></td><td>Power pin (-)</td><td></td></tr>
<tr><td>VDD</td><td></td><td>Power pin (+)</td><td></td></tr>
<tr><td>VP</td><td></td><td>Power pin (-) for VFD output pulldown resistor</td><td></td></tr>
<tr><td>VDDVPP</td><td></td><td>Power pin (+) *1</td><td></td></tr>
<tr><td>PORT0
P00 to P07</td><td>I/O</td><td>•8-bit input/output port
•Input for port 0 interrupt
•Input/output in nibble units
•Input for HOLD release</td><td>•Pullup resistor:
Provided/Not provided
•Output form: CMOS/
N-channel open drain</td></tr>
<tr><td>PORT1
P10 to P17</td><td>I/O</td><td>•8-bit input/output port
•Input/output can be specified in bit unit.
•Other pin functions
P10: SIO0 data output
P11: SIO0 data input/bus inpu/output
P12: SIO0 clock input/output
P13: SIO1 data output
P14: SIO1 data input/bus input/output
P15: SIO1 clock input/output
P16: Buzzer output
P17: Timer 1 output (PWM output)</td><td>•Output form: CMOS/
N-channel open drain</td></tr>
<tr><td>PORT7
P70
P71 - P73</td><td>I/O
I</td><td>•4-bit input port
•Other functions
P70: INT0 input / HOLD release / Nch-Tr. output for watchdog timer
P71: INT1 input / HOLD release
P72: INT2 input / timer 0 event input
P73: INT3 input with noise filter / timer 0 event input
•Interrupt received form, vector address
<table>
<tr><th></th><th>rising</th><th>falling</th><th>rising/
falling</th><th>H level</th><th>L level</th><th>Vector</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>03H</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>0BH</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>13H</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>1BH</td></tr>
</table></td><td>Pullup resistor:
Provided/Not provided</td></tr>
<tr><td>PORT8
P80 to P83</td><td>I</td><td>•4-bit input port
•Other functions
AD input port (4 port pins)</td><td></td></tr>
<tr><td>S0/T0 to S6/T6</td><td>O</td><td>Output for VFD display controller segment/timing in common
(Usable for static output port at pulldown registor Not provided.)</td><td>Pullup resistor:
Provided/Not provided</td></tr>
<tr><td>S7/T7 to
S15/T15</td><td>O</td><td>Output for VFD display controller segment/timing with internal pulldown resistor in common.</td><td></td></tr>
<tr><td>S16 to S29</td><td>O</td><td>Output for VFD display controller segment
(Usable for static output port at pulldown registor Not provided.)</td><td>Pullup resistor:
Provided/Not provided</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>I</td><td>Reset pin</td><td></td></tr>
<tr><td>TEST1</td><td>O</td><td>Test pin
Should be left unconnected. Fixed high level output.</td><td></td></tr>
<tr><td>XT1</td><td>I</td><td>Input pin for 32.768kHz crystal oscillation.
In case of non use, connect to VDD.</td><td></td></tr>
<tr><td>XT2</td><td>O</td><td>Output pin for 32.768kHz crystal oscillation.
In case of non use, should be left unconnected.</td><td></td></tr>
<tr><td>CF1</td><td>I</td><td>Input pin for ceramic resonator oscillation</td><td></td></tr>
<tr><td>CF2</td><td>O</td><td>Output pin for ceramic resonator oscillation</td><td></td></tr>
</table>

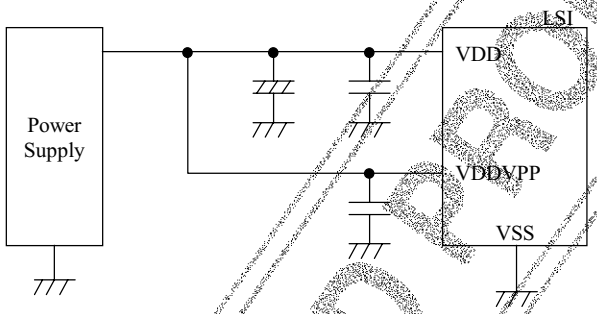
* All of port options can be specified in bit unit.

* A state of pins at reset.

Pin name	Input/output mode	A state of pullup resistor specified at pullup option
Ports 0,7	Input	Fixed pullup resistor exist
Port 1	Input	Programmable pullup resistor OFF

Pin name	A state of P-channel transistor
S0/T0 to S15/T15	P-channel transistor OFF
S16 to S29	P-channel transistor OFF

*1 Connect like the following figure to reduce noise into a VDD terminal
Shorten the VDD terminal to the VDDVPP terminal.



1. Absolute Maximum Ratings at VSS=0V and Ta=25°C

Parameter		Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Supply voltage		VDDMAX	VDD, VDDVPP	VDD=VDDVPP		-0.3		+7.0	V
Input voltage		VI(1)	•Ports 71,72,73 •Port 8 • $\overline{RES}$			-0.3		VDD+0.3	
		VI(2)	VP			VDD-45		VDD+0.3	
Output voltage		VO	•S0/T0 to S15/T15 •S16 to S29			VDD-45		VDD+0.3	
Input/output voltage		VIO	Ports 0,1,70			-0.3		VDD+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0,1	•CMOS output •For each pin.		-4			mA
		IOPH(2)	S0/T0 to S15/T15	For each pin.		-30			
		IOPH(3)	S16 to S29	For each pin.		-15			
	Total output current	∑IOAH(1)	Port 0	Total all pins.		-10			
		∑IOAH(2)	Port 1	Total all pins.		-10			
		∑IOAH(3)	•S0/T0 to S15/T15 •S16 to S29	Total all pins.		-130			
Low level output current	Peak output current	IOPL(1)	Ports 0,1	At each pin.				20	
		IOPL(2)	Port 70	At each pin.				15	
	Total output current	∑IOAL(1)	Port 0	Total all pins.				40	
		∑IOAL(2)	Ports 1,70	Total all pins.				40	
Maximum power dissipation		Pdmax(1)	DIP64S	Ta=-30 to +70°C				670	mW
		Pdmax(2)	QFP64E	Ta=-30 to +70°C				380	
Operating temperature range		Topg				-30		+70	°C
Storage temperature range		Tstg				-65		+150	

2. Recommended Operating Range at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Operating supply voltage range	VDD(1)	VDD	0.98μs ≤ tCYC ≤ 400μs		4.5		6.0	V
	VDD(2)		3.9μs ≤ tCYC ≤ 400μs		2.5		6.0	
Hold voltage	VHD	VDD	RAM and registers contain data at HOLD mode		2.0		6.0	
Pulldown voltage	VP	VP		2.5 - 6.0	-35		VDD	
Input high voltage	VIH(1)	Port 0 (Schumitt)	Output disable	2.5 - 6.0	0.4VDD +0.9		VDD	
	VIH(2)	•Port 1 •Ports 72, 73 (Schumitt)	Output disable	2.5 - 6.0	0.75VDD		VDD	
	VIH(3)	•Port 70 port input/interrupt •Port 71 • $\overline{\text{RES}}$ (Schumitt)	Output N-channel Tr. OFF	2.5 - 6.0	0.75VDD		VDD	
	VIH(4)	Port 70 Watchdog timer input	Output N-channel Tr. OFF	2.5 - 6.0	0.9VDD		VDD	
	VIH(5)	Port 8		2.5 - 6.0	0.75VDD		VDD	
Input low voltage	VIL(1)	Port 0 (Schumitt)	Output disable	2.5 - 6.0	VSS		0.2VDD	
	VIL(2)	•Port 1 •Ports 72, 73 (Schumitt)	Output disable	2.5 - 6.0	VSS		0.25VDD	
	VIL(3)	•Port 70 port input/interrupt •Port 71 • $\overline{\text{RES}}$ (Schumitt)	N-channel Tr. OFF	2.5 - 6.0	VSS		0.25VDD	
	VIL(4)	Port 70 Watchdog timer	N-channel Tr. OFF	2.5 - 6.0	VSS		0.8VDD -1.0	
	VIL(5)	Port 8		2.5 - 6.0	VSS		0.25VDD	
Operation cycle time	tCYC			4.5 - 6.0	0.98		400	μs
				2.5 - 6.0	3.9		400	
Oscillation frequency range (Note 1)	FmCF(1)	CF1,CF2	•12MHz (ceramic resonator oscillation) •Refer to figure 1	4.5 - 6.0	11.76	12	12.24	MHz
	FmCF(2)	CF1,CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 1	2.5 - 6.0	2.94	3	3.06	
	FmRC		RC oscillation	2.5 - 6.0	0.4	0.8	3.0	
	FsXtal	XT1, XT2	•32.768kHz (X'tal oscillation) •Refer to figure 2	2.5 - 6.0		32.768		kHz
Oscillation stabilizing time period (Note 1)	tmsCF(1)	CF1,CF2	•12MHz (ceramic resonator oscillation) •Refer to figure 3	4.5 - 6.0		0.02	0.2	ms
	tmsCF(2)	CF1,CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 3	4.5 - 6.0		0.1	1	
				2.5 - 6.0		0.1	3	
	tssXtal	XT1, XT2	•32.768kHz (X'tal oscillation) •Refer to figure 3	4.5 - 6.0		1	1.5	s
				2.5 - 6.0		1	3	

(Note 1) The oscillation constant is shown on table 1 and table 2.

3. Electrical Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions		Ratings			unit
				VDD[V]	min.	typ.	max.	
Input high current	IIH(1)	•Port 1 •Port 0 without pullup MOS Tr.	•Output disable •Pull-up MOS Tr. OFF •VIN=VDD (including the off-leak current of the output Tr.)	2.5 - 6.0			1	μA
	IIH(2)	•Port 7 without pullup MOS Tr. •Port 8	VIN=VDD	2.5 - 6.0			1	
	IIH(3)	$\overline{RES}$	VIN=VDD	2.5 - 6.0			1	
Input low current	IIL(1)	•Port 1 •Port 0 without pullup MOS Tr.	•Output disable •Pull-up MOS Tr. OFF •VIN=VSS (including the off-leak current of the output Tr.)	2.5 - 6.0	-1			
	IIL(2)	•Port 7 without pullup MOS Tr. •Port 8	VIN=VSS	2.5 - 6.0	-1			
	IIL(3)	$\overline{RES}$	VIN=VSS	2.5 - 6.0	-1			
Output high voltage	VOH(1)	CMOS output of ports 0, 1	IOH=-1.0mA	4.5 - 6.0	VDD-1			V
	VOH(2)		IOH=-0.1mA	2.5 - 6.0	VDD-0.5			
	VOH(3)	S0/T0 to S15/T15	IOH=-20mA	4.5 - 6.0	VDD-1.8			
	VOH(4)		•IOH=-1.0mA •The current of each pin is not over 1mA	2.5 - 6.0	VDD-1			
	VOH(5)	S16 to S29	IOH=-5mA	4.5 - 6.0	VDD-1.8			
	VOH(6)		•IOH=-1.0mA •The current of each pin is not over 1mA	2.5 - 6.0	VDD-1			
Output low voltage	VOL(1)	Ports 0, 1	IOL=10mA	4.5 - 6.0			1.5	
	VOL(2)		•IOL=1.6mA •The total current of the ports 0,1 is not over 40mA	4.5 - 6.0			0.4	
	VOL(3)		•IOL=1.0mA •The current of each pin is not over 1mA	2.5 - 6.0			0.4	
	VOL(4)	Port 70	IOL=1mA	4.5 - 6.0			0.4	
	VOL(5)		IOL=0.5mA	2.5 - 6.0			0.4	
Pull-up MOS Tr. resistance	Rpu	•Ports 0, 1	VOH=0.9VDD	4.5 - 6.0	15	40	70	KΩ
		•Port 7	VOH=0.9VDD	2.5 - 4.5	25	70	150	
Output off-leakage current	IOFF(1)	•S0/T0 to S6/T6 •S16 to S29 (Without pull down resistor.)	•Output P-channel Tr. OFF •VOUT=VSS	2.5 - 6.0	-1			μA
	IOFF(2)		•Output P-channel Tr. OFF •VOUT=VDD-40V	2.5 - 6.0	-30			
Pulldown transistor resistor	Rpd	•S0/T0 to S15/T15 •S16 to S29 (With pull down resistor.)	•Output P-channel Tr. OFF •VOUT=3V •Vp=-30V	5.0	60	100	200	kΩ
Hysteresis voltage	VHIS	•Ports 0, 1 •Port 7 •$\overline{RES}$	Output disable	2.5 - 6.0		0.1VDD		V
Pin capacitance	CP	All pins	•f=1MHz •Terminals other then unloaded terminals set to VIN=VSS •Ta=25°C	2.5 - 6.0		10		pF

4. Serial Input/Output Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter			Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Serial clock	Input clock	Cycle	tCKCY(1)	SCK0, SCK1	Refer to figure 5.	2.5 - 6.0	2			tCYC
		Low Level pulse width	tCKL(1)				1			
		High Level pulse width	tCKH(1)				1			
	Output clock	Cycle	tCKCY(2)	SCK0, SCK1	•Use a pull-up resistor (1kΩ) when an open drain output. •Refer to figure 5	2.5 - 6.0	2			
		Low Level pulse width	tCKL(2)					1/2tCKCY		
		High Level pulse width	tCKH(2)					1/2tCKCY		
Serial input	Data set up time		tICK	•SI0, SI1 •SB0,SB1	•Data set-up to SCK0, 1. •Data hold from SCK0, 1. •Refer to figure 5.	4.5 - 6.0	0.1			µs
						2.5 - 6.0	0.4			
	Data hold time		tCKI			4.5 - 6.0	0.1			
						2.5 - 6.0	0.4			
Serial output	Output delay time (External serial clock)		tCKO(1)	•SO0, SO1 •SB0,SB1	•Use a pull-up resistor (1kΩ) when an open drain output. •Data set-up to SCK0, 1 falling •Data hold from SCK0, 1 falling •Refer to figure 5	4.5 - 6.0			7/12tCYC +0.2	
						2.5 - 6.0			7/12tCYC +1	
	Output delay time (Internal serial clock)		tCKO(2)			4.5 - 6.0			1/3tCYC +0.2	
						2.5 - 6.0			1/3tCYC +1	

5. Pulse Input Conditions at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
High/low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2/T0IN	•Interrupt acceptable •Timer0-countable	2.5 - 6.0	1			tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (The noise rejection clock is selected to 1/1.)	•Interrupt acceptable •Timer0-countable	2.5 - 6.0	2			
	tPIH(3) tPIL(3)	INT3/T0IN (The noise rejection clock is selected to 1/64.)	•Interrupt acceptable •Timer0-countable	2.5 - 6.0	128			
	tPIL(4)	$\overline{\text{RES}}$	Reset acceptable	2.5 - 6.0	200			µs

6. AD Converter Characteristics at Ta=-30°C to + 70°C, VSS=0V

Parameter	Symbol	Pins	Conditions		Ratings			unit
				VDD[V]	min.	typ.	max.	
Resolution	N			4.5 - 6.0		8		bit
Absolute precision	ET		(Note 2)				±1.5	LSB
Conversion time	tCAD		AD conversion time = 16 × tCYC (ADCR2=0) (Note 3)		15.68 (tCYC= 0.98µs)		65.28 (tCYC= 4.08µs)	µs
			AD conversion time = 32 × tCYC (ADCR2=1) (Note 3)		31.36 (tCYC= 0.98µs)		130.56 (tCYC= 4.08µs)	
Analog input voltage range	VAIN	AN0 - AN3		4.5 - 6.0	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	4.5 - 6.0			1	µA
	IAINL		VAIN=VSS	4.5 - 6.0	-1			

(Note 2) Absolute precision excepts quantizing error (±1/2 LSB).
(Note 3) The conversion time means the time from executing the AD conversion instruction to setting the complete digital conversion value to the register.

7. Current Dissipation Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	typ.	max.	unit
Current dissipation during basic operation (Note 4)	IDDOP(1)	VDD	•FmCF=12MHz Ceramic resonator oscillation •FsX'tal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops	4.5 - 6.0		10	20	mA
	IDDOP(2)		•FmCF=3MHz Ceramic resonator oscillation •FsX'tal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops	4.5 - 6.0		3	6	
	IDDOP(3)			2.5 - 4.5		1.5	5	
	IDDOP(4)		•FmCF=0Hz (When oscillation stops) •FsX'tal=32.768kHz crystal oscillation •System clock : RC oscillation	4.5 - 6.0		0.7	1.4	
	IDDOP(5)			2.5 - 4.5		0.4	1.2	
	IDDOP(6)		•FmCF=0Hz (When oscillation stops) •FsX'tal=32.768kHz crystal oscillation •System clock : 32.768kHz •Internal RC oscillation stops	4.5 - 6.0		35	70	µA
	IDDOP(7)			2.5 - 4.5		15	50	

Continue.

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Current dissipation in HALT mode (Note 4)	IDDHALT(1)	VDD	•HALT mode •FmCF=12MHz Ceramic resonator oscillation •FsX'tal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops	4.5 - 6.0		5	10	mA
	IDDHALT(2)		•HALT mode	4.5 - 6.0		1.8	4.6	
	IDDHALT(3)		•FmCF=3MHz Ceramic resonator oscillation •FsX'tal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops	2.5 - 4.5		0.8	2.5	
	IDDHALT(4)		•HALT mode	4.5 - 6.0		400	800	µA
	IDDHALT(5)		•FmCF=0Hz (When oscillation stops) •FsX'tal=32.768kHz crystal oscillation •System clock : RC oscillation	2.5 - 4.5		200	600	
	IDDHALT(6)		•HALT mode	4.5 - 6.0		20	60	
	IDDHALT(7)		•FmCF=0Hz (When oscillation stops) •FsX'tal=32.768kHz crystal oscillation •System clock : 32.768kHz •Internal RC oscillation stops	2.5 - 4.5		7	40	
Current dissipation in HOLD mode (Note 4)	IDDHOLD(1)	VDD	HOLD mode	4.5 - 6.0		0.05	30	
	IDDHOLD(2)			2.5 - 4.5		0.02	20	

(Note 4) The currents of the output transistors and the pull-up MOS transistors are ignored.

Table 1. Ceramic resonator oscillation recommended constant (main clock)

Oscillation type	Maker	Oscillator	C1	C2
12MHz ceramic resonator oscillation	Murata	CSA12.0MTZ	33pF	33pF
		CST12.0MTW	on chip	
	Kyocera	KBR-12.0M	33pF	33pF
3MHz ceramic resonator oscillation	Murata	CSA3.00MG	33pF	33pF
		CST3.00MGW	on chip	
	Kyocera	KBR-3.0MS	47pF	47pF

* Both C1 and C2 must use K rank (±10%) and SL characteristics.

Table 2. Crystal oscillation recommended constant (sub clock)

Oscillation type	Maker	Oscillator	C3	C4
32.768kHz crystal oscillation	Dai Sinku	DT-38(1TA252E00)	18pF	18pF
	Kyocera	KF-38G-13P0200	4pF	4pF

* Both C3 and C4 must use J rank (±5%) and CH characteristics.
(It is about the application which is not in need of high precision. Use K rank (±10%) and SL characteristics.)

(Notes) •Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.
•If you use other oscillators herein, we provide no guarantee for the characteristics.

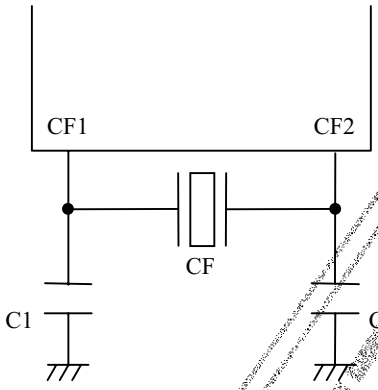


Figure 1 Main-clock circuit
Ceramic resonator oscillation

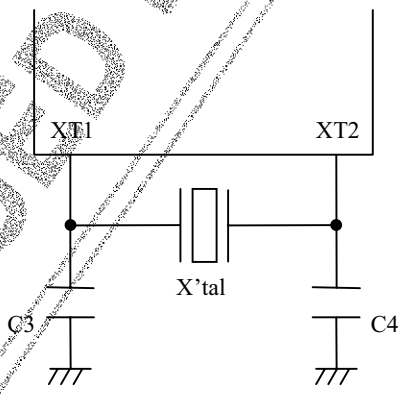


Figure 2 Sub-clock circuit
Crystal oscillation

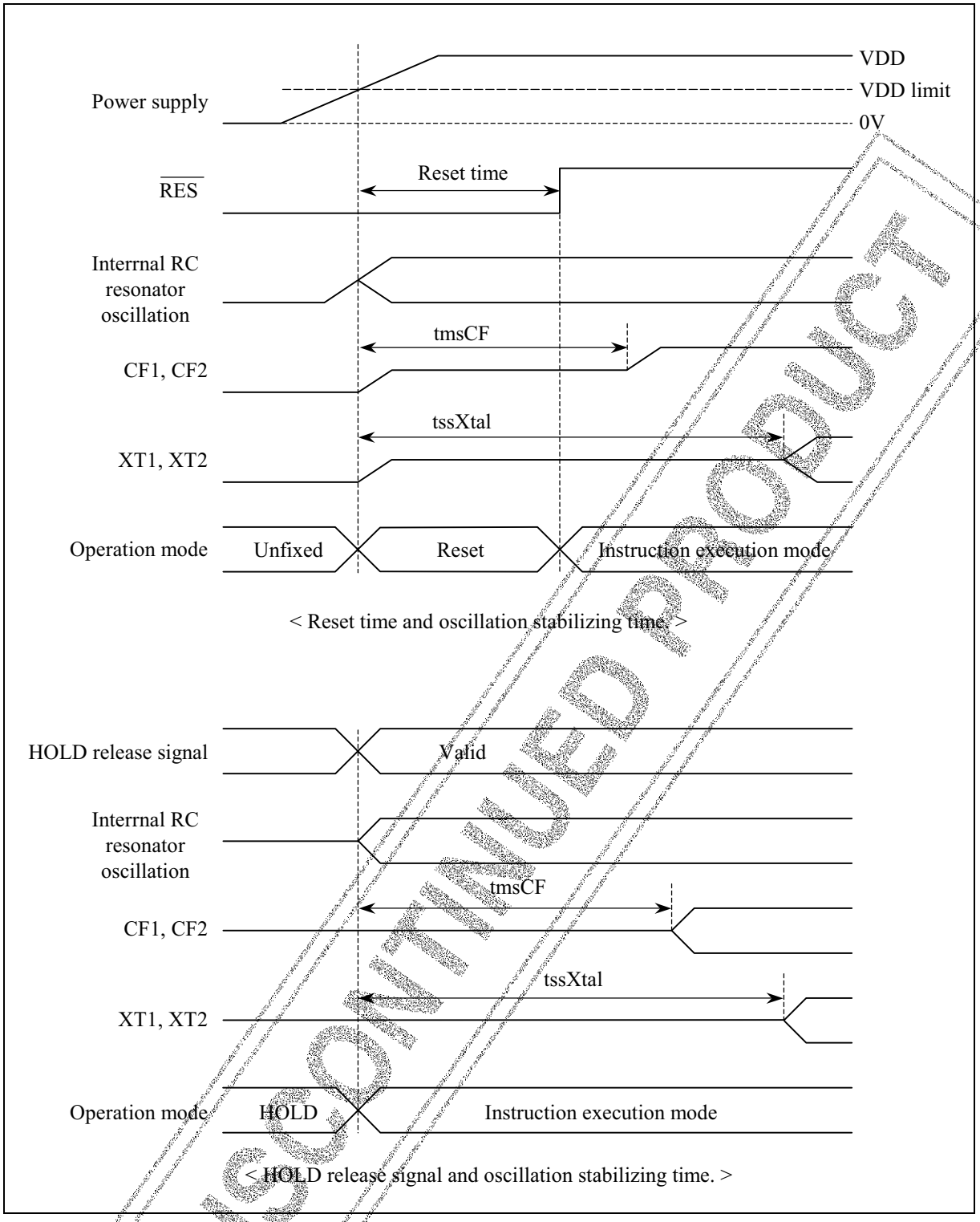
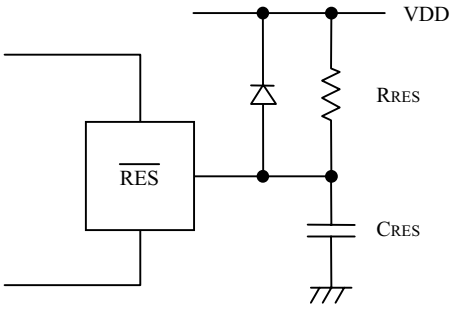


Figure 3 Oscillation stabilizing time



(Note) Fix the value of CRES, RRES that is sure to reset until 200μs, after Power supply has been over inferior limit of supply voltage.

Figure 4 Reset circuit

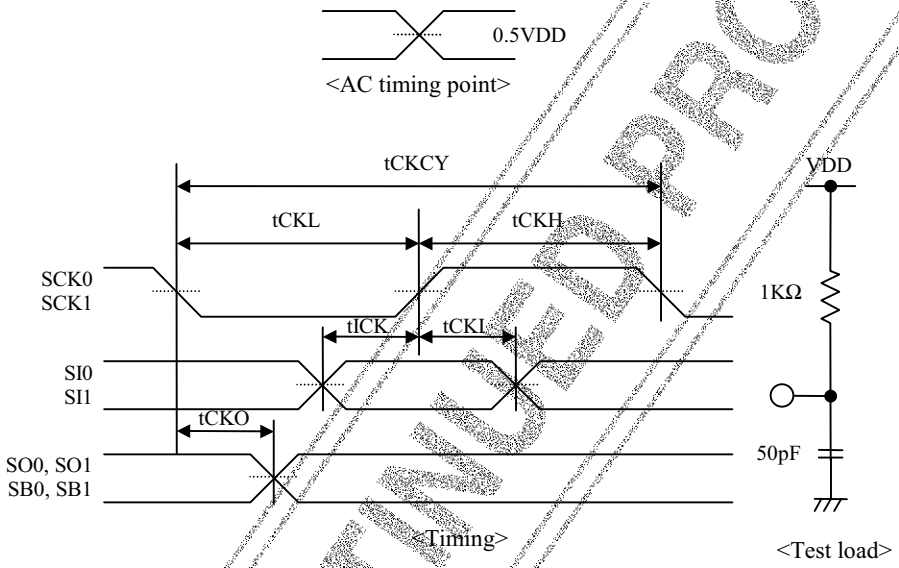


Figure 5 Serial input / output test condition

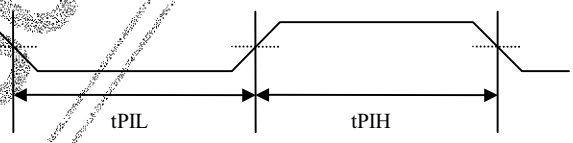


Figure 6 Pulse input timing condition

memo: