

3.3V 168 pin Registered SDRAM Modules

**64MB, 128MB, 256MB,
512MB & 1GB Densities**

**HYS72V8200GR
HYS72V16200GR
HYS72V32200GR
HYS72V32220GR
HYS72V64200GR
HYS72V128220GR**

- 168 Pin JEDEC Standard, Registered 8 Byte Dual-In-Line SDRAM Module for PC and Server main memory applications
- One bank 8M x 72, 16M x 72, 32M x 72 and 64M x 72 organisation
two bank 32M x 72 & 128M x 72 organisation
- Optimized for ECC applications with very low input capacitances
- JEDEC standard Synchronous DRAMs (SDRAM)
- Performance:

		-8	-8B	Units
f _{CK}	Clock frequency (max.)	100	100	MHz
t _{CK}	Clock cycle time (min.)	10	10	ns
t _{AC}	Clock access time (min.)			
	CAS latency = 3	6	6	ns
	CAS latency = 2	6	7	ns

- Single +3.3V(± 0.3V) power supply
- Programmable $\overline{\text{CAS}}$ Latency, Burst Length and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All inputs, outputs are LVTTTL compatible
- Serial Presence Detect with E²PROM
- Utilizes 64M & 256M SDRAMs in TSOPII-54 packages with registers and PLL.
The two bank module uses stacked TSOP54 packages
- 4096 refresh cycles every 64 ms
- Card Size: 133,35 mm x 38.1mm / 43.18mm x 4,00 / 6.50mm with Gold contact pads
- This specification largely follows the JEDEC STANDARD 21-C / Release 8 / Section 4.5.7 specification and as far as applicable - INTEL's "PC SDRAM Registered DIMM Specification" Rev.1.0 (Feb.98 and Rev.1.1 (Aug. 98).

The HYS72Vx2x0GR family are industry standard 168-pin 8-byte Dual in-line Memory Modules (DIMMs) which are organised as 8M x 72, 16M x 72, 32M x 72, 64M x 72 & 128M x 72 high speed memory arrays designed with Synchronous DRAMs (SDRAMs) for ECC applications. All control and address signals are registered on-DIMM and the design incorporates a PLL circuit for the Clock inputs. The 256MB module is available as one bank and two bank module version. Use of an on-board register reduces capacitive loading on the input signals but are delayed by one cycle in arriving at the SDRAM devices. Decoupling capacitors are mounted on the PC board. The DIMMs use a serial presence detects scheme implemented via a serial E²PROM using the two pin I²C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user. All SIEMENS 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 133,35 mm long footprint.

Ordering Information

Type	Speed Code	Descriptions	SDRAM Technology
HYS72V8200GR-8 HYS72V8200GR-8B	PC100-222-620R PC100-323-620R	one bank 64 MB Reg. DIMM INTEL Rev. 1.0	64 MBit
HYS72V16200GR-8 HYS72V16200GR-8B	PC100-222-620R PC100-323-620R	one bank 128 MB Reg. DIMM INTEL Rev. 1.0	64 MBit
HYS72V32220GR-8 HYS72V32220GR-8B	PC100-222-620R PC100-323-620R	two bank 256 MB Reg. DIMM INTEL Rev. 1.1	64 MBit (stacked)
HYS72V32200GR-8 HYS72V32200GR-8B	PC100-222-620R PC100-323-620R	one bank 256 MB Reg. DIMM INTEL Rev. 1.0	256 MBit
HYS72V64200GR-8 HYS72V64200GR-8B	PC100-222-620R PC100-323-620R	one bank 512 MB Reg. DIMM INTEL Rev. 1.0	256 MBit
HYS72V128220GR-8 HYS72V128220GR-8B	PC100-222-620R PC100-323-620R	two bank 1 GByte Reg. DIMM INTEL Rev. 1.1	256 MBit (stacked)

Pin Names

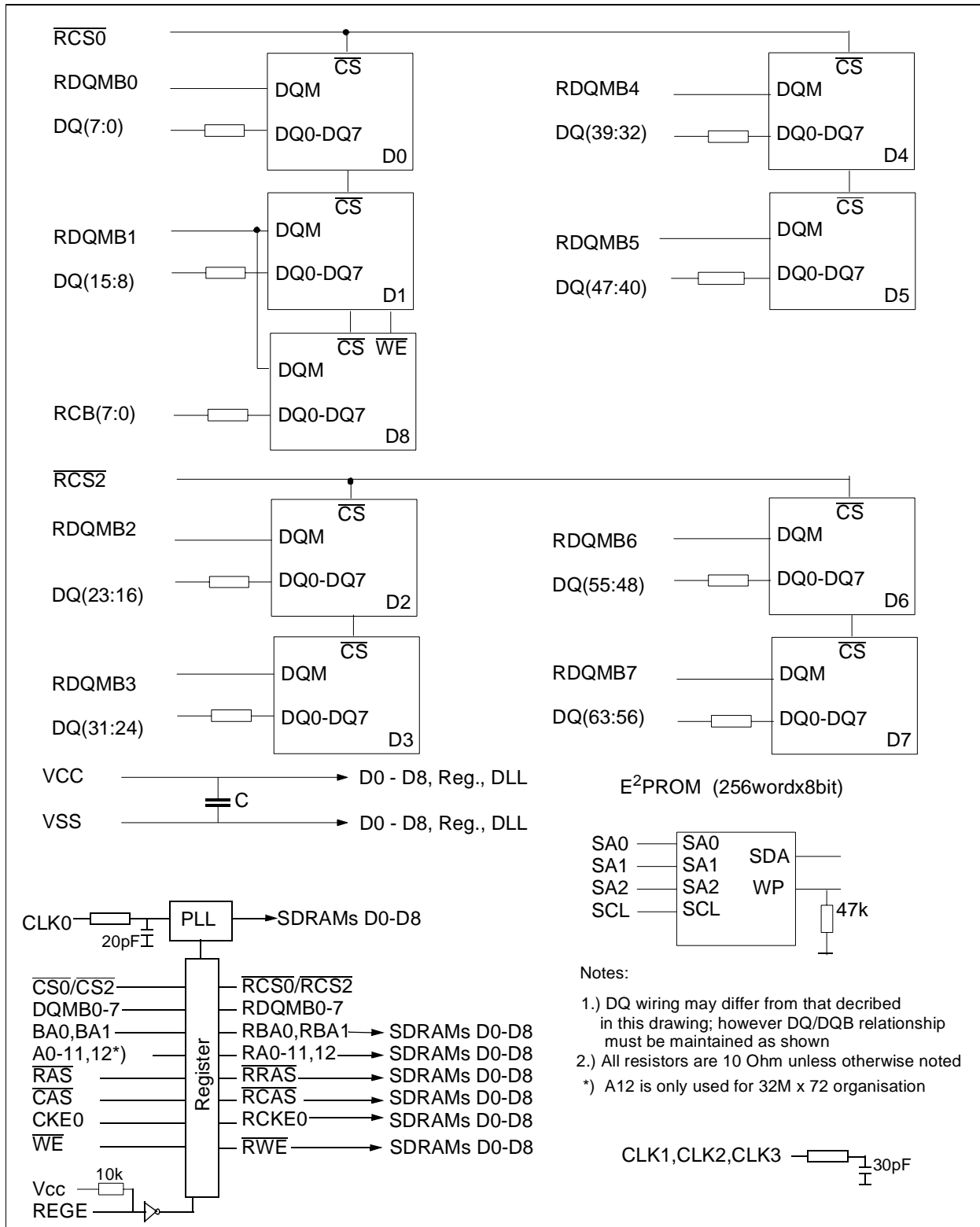
A0-A11,A12	Address Inputs	DQMB0 - DQMB7	Data Mask
BA0, BA1	Bank Selects	CS0 - CS3	Chip Select
DQ0 - DQ63	Data Input/Output	REGE	Register Enable
CB0-CB7	Check Bits (x72 organisation only)	VDD	Power (+3.3 Volt)
\overline{RAS}	Row Address Strobe	VSS	Ground
\overline{CAS}	Column Address Strobe	SCL	Clock for Presence Detect
\overline{WE}	Read / Write Input	SDA	Serial Data Out
$\overline{CKE0}, \overline{CKE1}$	Clock Enable	N.C.	No Connection
CLK0 - CLK3	Clock Input		

Address Format:

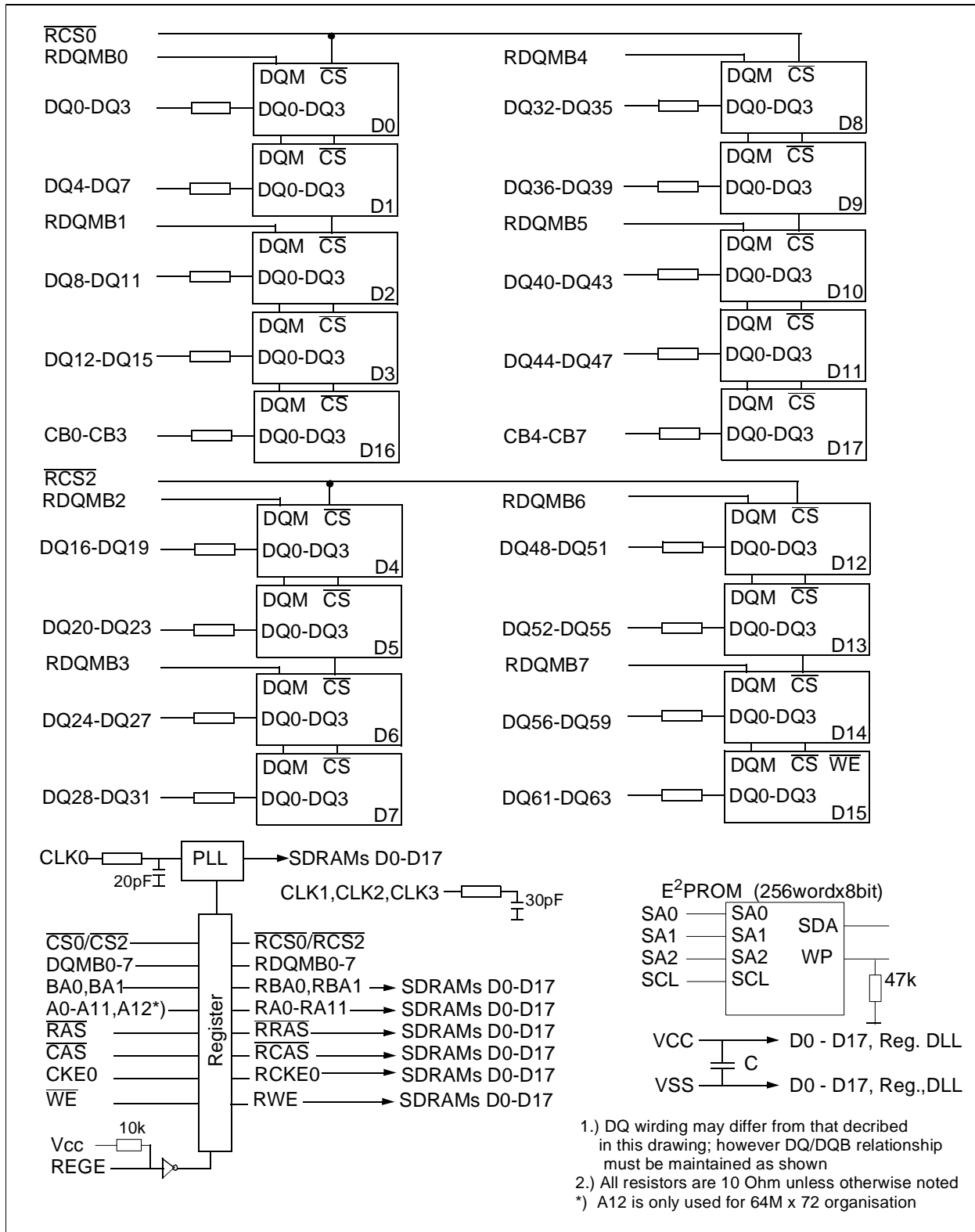
Density	Org.	Memory Banks	SDRAMs	# of SDRAMs	# of row/bank/ column bits	Refresh	Period	Interval
64 MB	8M x 72	1	8M x 8	9	12 / 2 / 9	4k	64 ms	15,6 μ s
128 MB	16M x 72	1	16M x 4	18	12 / 2 / 10	4k	64 ms	15,6 μ s
256 MB	32M x 72	2	16M x 4	36	12 / 2 / 10	4k	64 ms	15,6 μ s
256 MB	32M x 72	1	32M x 8	9	13 / 2 / 10	8k	64 ms	7,8 μ s
512 MB	64M x 72	1	64M x 4	18	13 / 2 / 11	8k	64 ms	7,8 μ s
1 GB	64M x 72	2	64M x 4	36	13 / 2 / 11	8k	64ms	7,8 μ s

Pin Configuration

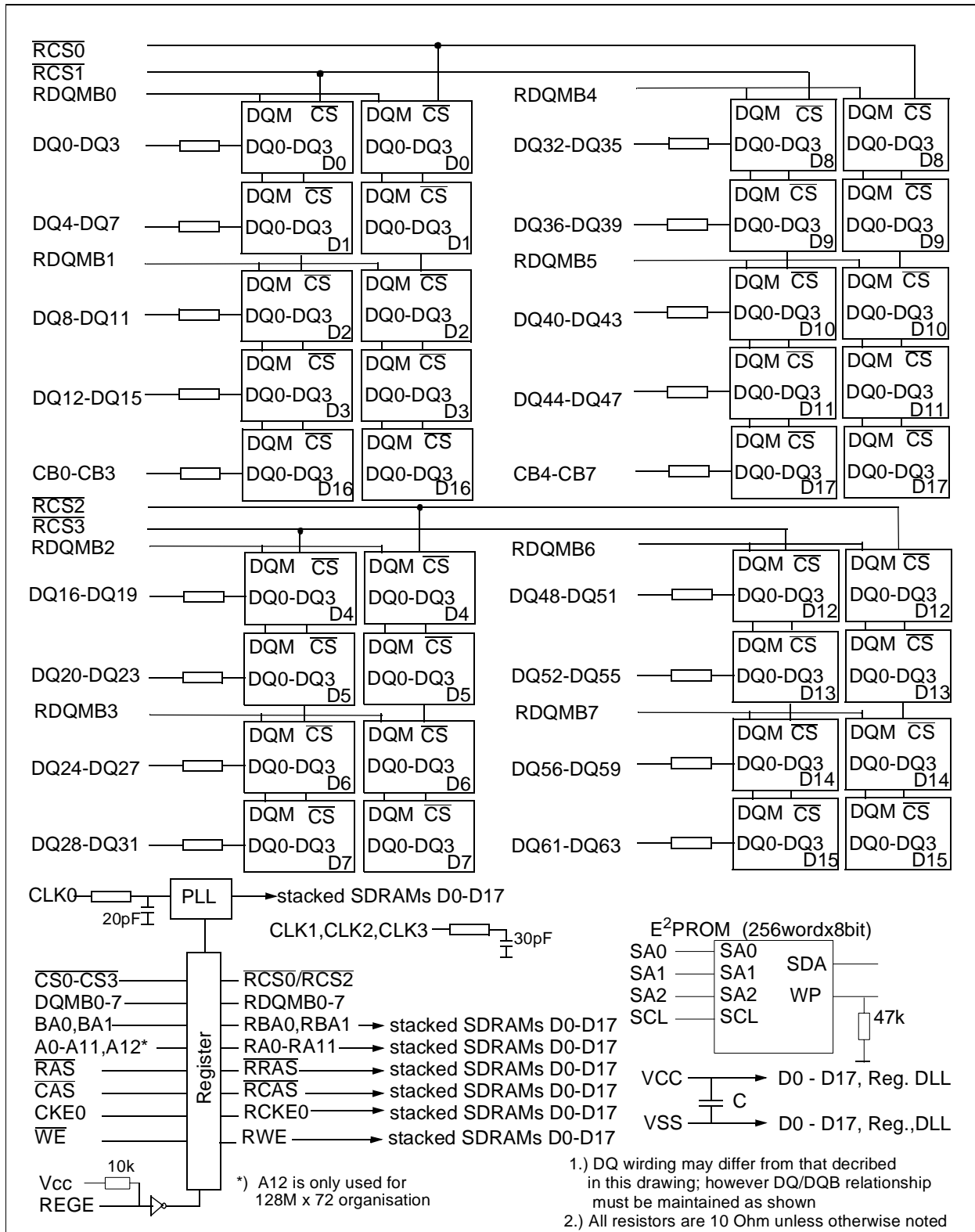
PIN #	Symbol	PIN #	Symbol	PIN #	Symbol	PIN #	Symbol
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	DU	86	DQ32	128	CKE0
3	DQ1	45	CS2	87	DQ33	129	CS3
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	VCC	48	DU	90	VCC	132	NC
7	DQ4	49	VCC	91	DQ36	133	VCC
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VCC	101	DQ45	143	VCC
18	VCC	60	DQ20	102	VCC	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	DU	104	DQ47	146	DU
21	CB0	63	CKE1	105	CB4	147	REGE
22	CB1	64	VSS	106	CB5	148	VSS
23	VSS	65	DQ21	107	VSS	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VCC	68	VSS	110	VCC	152	VSS
27	WE	69	DQ24	111	CAS	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	CS0	72	DQ27	114	NC	156	DQ59
31	DU	73	VCC	115	RAS	157	VCC
32	VSS	74	DQ28	116	VSS	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	CLK2	121	A9	163	CLK3
38	A10 (AP)	80	NC	122	BA0	164	NC
39	BA1	81	WP	123	A11	165	SA0
40	VCC	82	SDA	124	VCC	166	SA1
41	VCC	83	SCL	125	CLK1	167	SA2
42	CLK0	84	VCC	126	A12	168	VCC



**Block Diagram for one bank 8M x 72 & 32M x 72 SDRAM DIMM modules
HYS72V8200GR / HYS72V32200GR using x8 organised SDRAMs**



**Block Diagram for one bank 16M x 72 & 64M x 72 SDRAM DIMM modules
HYS72V16200GR / HYS72V64200GR using x4 organised SDRAMs**



**Block Diagram for two bank 32M x 72 & 128M x 72 SDRAM DIMM modules
HYS72V32220GR / HYS72V128220GR using stacked x4 organised SDRAMs**

DC Characteristics

$T_A = 0$ to 70 °C; $V_{SS} = 0$ V; $V_{DD}, V_{DDQ} = 3.3$ V \pm 0.3 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input high voltage	V_{IH}	2.0	$V_{CC}+0.3$	V
Input low voltage	V_{IL}	- 0.5	0.8	V
Output high voltage ($I_{OUT} = - 2.0$ mA)	V_{OH}	2.4	-	V
Output low voltage ($I_{OUT} = 2.0$ mA)	V_{OL}	-	0.4	V
Input leakage current, any input (0 V < $V_{IN} < 3.6$ V, all other inputs = 0 V)	$I_{I(L)}$	- 10	10	μ A
Output leakage current (DQ is disabled, 0 V < $V_{OUT} < V_{CC}$)	$I_{O(L)}$	- 10	10	μ A

Capacitance

$T_A = 0$ to 70 °C; $V_{DD} = 3.3$ V \pm 0.3 V, $f = 1$ MHz

Parameter	Symbol	Limit Values (max.)		Unit
		one bank modules	two bank modules	
Input Capacitance (all inputs except CLK)	C_{IN}	10	10	pF
Input Capacitance (CLK)	C_{CLK}	30	30	pF
Input / Output capacitance (DQ0-DQ63, CB0-CB7)	C_{IO}	10	15	pF
Input Capacitance (SCL, SA0-2)	C_{SC}	8	8	pF
Input/Output Capacitance (SDA)	C_{SD}	10	10	pF

64MBit SDRAM Operating Currents ($T_A = 0$ to 70°C , $V_{dd} = 3.3\text{V} \pm 0.3\text{V}$)

(Recommended Operating Conditions unless otherwise noted)

Parameter & Test Condition	Symb.	-8/-8B	Note
		max.	
OPERATING CURRENT trc=trcmin., tck=tckmin. Outputs open, Burst Length = 4, CL=3 All banks operated in random access, all banks operated in ping-pong manner to maximize gapless data access	ICC1 x4 x8	100 110	mA mA 1
PRECHARGE STANDBY CURRENT in Power Down Mode tck = min.	ICC2P	2	mA 1
$\overline{\text{CS}} = \text{VIH}(\text{min.}), \text{CKE} \leq \text{Vil}(\text{max})$ tck = Infinity	ICC2PS	1	mA 1
PRECHARGE STANDBY CURRENT in Non-Power Down Mode tck = min.	ICC2N	35	mA 1
$\overline{\text{CS}} = \text{VIH}(\text{min.}), \text{CKE} \geq \text{Vih}(\text{min})$ tck = Infinity	ICC2NS	5	mA 1
NO OPERATING CURRENT tck = min., $\overline{\text{CS}} = \text{VIH}(\text{min})$, active state (max. 4 banks)	ICC3N ICC3P	45 8	mA mA 1 1
BURST OPERATING CURRENT tck = min., Read command cycling	ICC4 x4 x8	60 70	mA mA 1,2
AUTO REFRESH CURRENT tck = min., Auto Refresh command cycling	ICC5	130	mA 1
SELF REFRESH CURRENT Self Refresh Mode, CKE=0.2V	ICC6	1	mA 1

256MBit Operating Currents ($T_A = 0$ to 70°C , $V_{dd} = 3.3\text{V} \pm 0.3\text{V}$)

(Recommended Operating Conditions unless otherwise noted)

Parameter & Test Condition	Symb.	-8/-8B	Note
		max.	
OPERATING CURRENT trc=trcmin., tck=tckmin. Outputs open, Burst Length = 4, CL=3 All banks operated in random access, all banks operated in ping-pong manner to maximize gapless data access	ICC1 x4 x8	210 210	mA mA mA 1
PRECHARGE STANDBY CURRENT in Power Down Mode $\overline{\text{CS}} = V_{IH}$ (min.), $\text{CKE} \leq V_{il}(\text{max})$	tck = min. ICC2P	2	mA 1
PRECHARGE STANDBY CURRENT in Non-Power Down Mode $\overline{\text{CS}} = V_{IH}$ (min.), $\text{CKE} \geq V_{ih}(\text{min})$	tck = min. ICC2N	19	mA 1
NO OPERATING CURRENT tck = min., $\overline{\text{CS}} = V_{IH}(\text{min})$, active state (max. 4 banks)	$\text{CKE} \geq V_{IH}(\text{min.})$ ICC3N	45	mA 1
	$\text{CKE} \leq V_{IL}(\text{max.})$ ICC3P	10	mA 1
BURST OPERATING CURRENT tck = min., Read command cycling	ICC4 x4 x8	210 210	mA mA 1,2
AUTO REFRESH CURRENT tck = min., Auto Refresh command cycling	ICC5	240	mA 1
SELF REFRESH CURRENT Self Refresh Mode, $\text{CKE}=0.2\text{V}$	ICC6	2.5	mA 1

AC Characteristics (SDRAM Device Specification) 3)4)

$T_A = 0$ to 70 °C; $V_{SS} = 0$ V; $V_{CC} = 3.3$ V \pm 0.3 V, $t_T = 1$ ns

Parameter	Symbol	Limit Values				Unit
		-8		-8B		
		min.	max.	min.	max.	

Clock and Clock Enable

Clock Cycle Time	$\overline{\text{CAS}}$ Latency = 2	t_{CK}	10	–	12	–	ns	
	$\overline{\text{CAS}}$ Latency = 3		10	–	10	–		
Clock Frequency	$\overline{\text{CAS}}$ Latency = 2	t_{CK}	–	100	–	83	MHz	
	$\overline{\text{CAS}}$ Latency = 3		–	100	–	100		
Access Time from Clock	$\overline{\text{CAS}}$ Latency = 2	t_{AC}	–	6	–	7	ns	4
	$\overline{\text{CAS}}$ Latency = 3		–	6	–	6		
Clock High Pulse Width		t_{CH}	3	–	3	–	ns	
Clock Low Pulse Width		t_{CL}	3	–	3	–	ns	
Transition time		t_T	0.5	10	0.5	10	ns	

Setup and Hold Times

Input Setup Time	t_{IS}	2	–	2	–	ns	5
Input Hold Time	t_{IH}	1	–	1	–	ns	5
CKE Setup Time	t_{CKS}	2	–	2	–	ns	5
CKE Hold Time	t_{CKH}	1	–	1	–	ns	5
Mode Register Set-up time	t_{RSC}	16	–	20	–	ns	
Power Down Mode Entry Time	t_{SB}	0	8	0	10	ns	

Common Parameters

Row to Column Delay Time	t_{RCD}	20	–	20	–	ns	6
Row Precharge Time	t_{RP}	20	–	30	–	ns	6
Row Active Time	t_{RAS}	45	100k	60	100k	ns	6
Row Cycle Time	t_{RC}	70	–	80	–	ns	6
Activate(a) to Activate(b) Command period	t_{RRD}	16	–	20	–	ns	6
$\overline{\text{CAS}}$ (a) to $\overline{\text{CAS}}$ (b) Command period	t_{CCD}	1	–	1	–	CLK	

Parameter	Symbol	Limit Values				Unit
		-8		-8B		
		min.	max.	min.	max.	

Refresh Cycle

Refresh Period	t_{REF}						
64M SDRAM based modules		–	15,6	–	15,6	μ s	
256M SDRAM based modules		–	7,8	–	7,8	μ s	
Self Refresh Exit Time	t_{SREX}	10		10		ns	

Read Cycle

Data Out Hold Time	t_{OH}	3	–	3	–	ns	
Data Out to Low Impedance Time	t_{LZ}	0	–	0	–	ns	
Data Out to High Impedance Time	t_{HZ}	3	8	3	10	ns	8
DQM Data Out Disable Latency	t_{DQZ}	–	2	–	2	CLK	

Write Cycle

Data Input to Precharge (write recovery)	t_{WR}	2	–	2	–	CLK	
Data In to Active / Refresh	t_{DAL}	5	–	5	–	CLK	
DQM Write Mask Latency	t_{DQW}	0	–	0	–	CLK	

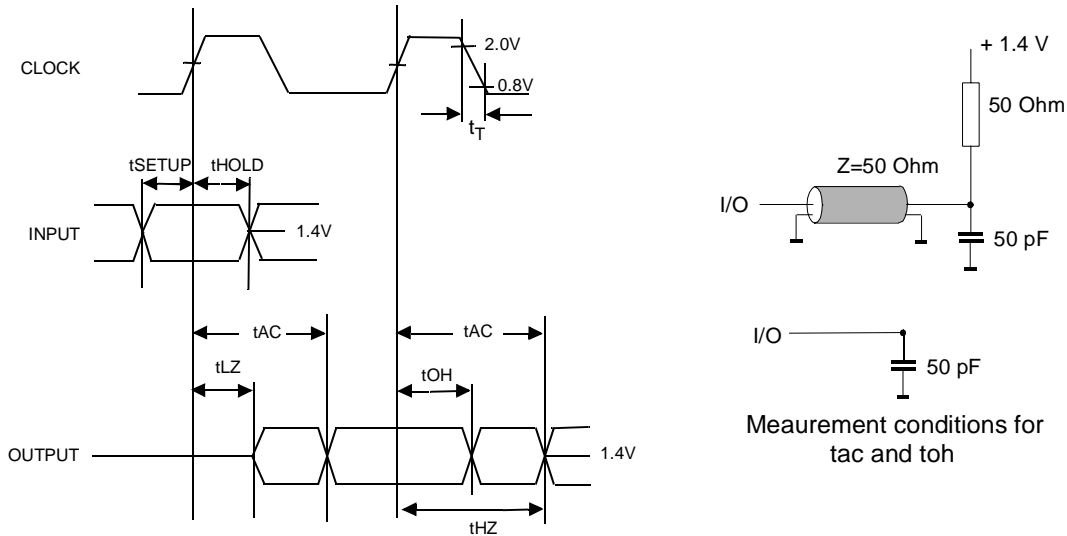
Clock Frequency and Latency (Registered DIMM Module Specification): 9)

Parameter		Symbol	-8	-8B	Unit	Notes
Clock Frequency	max.	t_{CK}	100	100	MHz	
Clock Cycle Time	min.	t_{CK}	10	10	ns	
CAS Latency	min.	t_{AA}	3	4	CLK	10)
RAS to CAS Delay	min.	t_{RCD}	2	2	CLK	
RAS Latency	min.	t_{RL}	6	7	CLK	10)
Precharge Time	min.	t_{RP}	2	3	CLK	
Data In to Precharge	min.	t_{DPL}	2	2	CLK	
Data In to Active / Refresh	min.	t_{DAL}	5	5	CLK	
Bank to Bank Delay Time	min.	t_{RRD}	2	2	CLK	
CAS to CAS delay time	min.	t_{CCD}	1	1	CLK	
Write Latency	fixed	t_{WL}	1	1	CLK	10)
DQM Write Mask Latency	fixed	t_{DQW}	1	1	CLK	
DQM Data Disable Latency	fixed	t_{DQZ}	1	1	CLK	
Clock Suspend Latency	fixed	t_{CSL}	1	1	CLK	10)

Notes:

1. The specified values are valid when addresses are changed no more than once during $t_{CK}(\text{min.})$ and when No Operation commands are registered on every rising clock edge during $t_{RC}(\text{min.})$. Values are shown per SDRAM component.
2. The specified values are valid when data inputs (DQ's) are stable during $t_{RC}(\text{min.})$.
3. An initial pause of 100 μs is required after power-up, then a Precharge All Banks command must be given followed by 8 Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin. Also the on-DIMM PLL must be given enough clock cycles to stabilize (t_{STAB}) before any operation can be guaranteed.
4. AC timing tests have $V_{ij} = 0.8\text{V}$ and $V_{ih} = 2.0\text{V}$ with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{ih} and V_{ij} . All AC measurements assume $t_T=1\text{ns}$

with the AC output load circuit shown. Specified t_{ac} and t_{oh} parameters are measured with a 50



pF only, without any resistive termination and with a input signal of 1V / ns edge rate between 0.8V and 2.0 V.

5. Any time that the refresh Period has been exceeded, a minimum of two Auto (CRB) Refresh commands must be given to "wake-up" the device.
6. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to t_{RC} is satisfied once the Self Refresh Exit command is registered.
7. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels.
8. t_{DAL} is equivalent to $t_{DPL} + t_{RP}$.
9. Due to the usage of a register device on all input and address signals, all external command cycle are delayed by one clock (Reg-DIMM Latency = 1) on the module board.
10. Delayed by one clock cycle due to the use of the register device.

A serial presence detect storage device - E²PROM 34C02 - is assembled onto the module. Information about the module configuration, speed, etc. is written into the E²PROM device during module production using a serial presence detect protocol (I²C synchronous 2-wire bus)

SPD-Table for -8 Registered DIMM Modules with PLL:

Byte#	Description	SPD Entry Value	Hex					
			64MB with PLL 1 bank	128MB with PLL 1 bank	256MB with PLL 2 banks	256MB with PLL 1 bank	512MB with PLL 1 bank	1GB with PLL 2 bank
0	Number of SPD bytes	128	80	80	80	80	80	80
1	Total bytes in Serial PD	256	08	08	08	08	08	08
2	Memory Type	SDRAM	04	04	04	04	04	04
3	Number of Row Addresses (without BS bits)	12 / 13	0C	0C	0C	0D	0D	0D
4	Number of Column Addresses	9 / 10 / 11	09	0A	0A	0A	0B	0B
5	Number of DIMM Banks	1	01	01	02	01	01	02
6	Module Data Width	72	48	48	48	48	48	48
7	Module Data Width (cont'd)	0	00	00	00	00	00	00
8	Module Interface Levels	LVTTTL	01	01	01	01	01	01
9	Cycle Time at CL=3	10.0 ns	A0	A0	A0	A0	A0	A0
10	Access time from Clock at CL=3	6.0 ns	60	60	60	60	60	60
11	Dimm Config (Error Det/Corr.)	ECC	02	02	02	02	02	02
12	Refresh Rate/Type	Self-Refresh, 15.6µs	80	80	80	80	80	80
13	SDRAM width, Primary	x4, x8	08	04	04	08	04	04
14	Error Checking SDRAM data width	n/a / x4	08	04	04	08	04	04
15	Minimum tCCD	1 CLK	01	01	01	01	01	01
16	Burst Length supported	1, 2, 4, 8 & full page	8F	8F	8F	8F	8F	8F
17	Number of SDRAM banks	4	04	04	04	04	04	04
18	SDRAM Supported CAS Latencies	2 & 3	06	06	06	06	06	06
19	SDRAM CS Latencies	0	01	01	01	01	01	01
20	SDRAM WE Latencies	0	01	01	01	01	01	01
21	SDRAM DIMM module attributes	with PLL	16	16	16	16	16	16
22	SDRAM Device Attributes	Vcc tol +/- 10%	0E	0E	0E	0E	0E	0E
23	Min. Clock Cycle Time at CL = 2	10 ns	A0	A0	A0	A0	A0	A0
24	Max. data access time from Clock for CL=2	6 ns	60	60	60	60	60	60
25	Min. Clock Cycle Time at CL = 1	not supported	FF	FF	FF	FF	FF	FF

Preliminary Information

SPD cont'

Byte#	Description	SPD Entry Value	Hex					
			64MB with PLL 1 bank	128MB with PLL 1 bank	256MB with PLL 2 banks	256MB with PLL 1 bank	512MB with PLL 1 bank	1GB with PLL 2 bank
26	Max. Data Access Time from Clock at CL=1	not supp.	FF	FF	FF	FF	FF	FF
27	SDRAM Minimum tRP	20 ns	14	14	14	14	14	14
28	SDRAM Minimum tRRD	16 ns	10	10	10	10	10	10
29	SDRAM Minimum tRCD	20 ns	14	14	14	14	14	14
30	SDRAM Minimum tRAS	45 ns	2D	2D	2D	2D	2D	2D
31	Module Bank Density (per bank)	64/128/256/ 512 MByte	10	20	20	40	80	80
32	SDRAM input setup time	2 ns	20	20	20	20	20	20
33	SDRAM input hold time	1 ns	10	10	10	10	10	10
34	SDRAM data input setup time	2 ns	20	20	20	20	20	20
35	SDRAM data input hold time	1 ns	10	10	10	10	10	10
36-61	Superset information (may be used in future)		FF	FF	FF	FF	FF	FF
62	SPD Revision	1.2	12	12	12	12	12	12
63	Checksum for bytes 0 -62		08	11	12	3A	73	74
64-125	Manufacturer's information (FFh if not used)							
126	Frequency Specification	100 Mhz	64	64	64	64	64	64
127	Details of Clocks		8F	8F	8F	8F	8F	8F
128+	Unused storage locations							

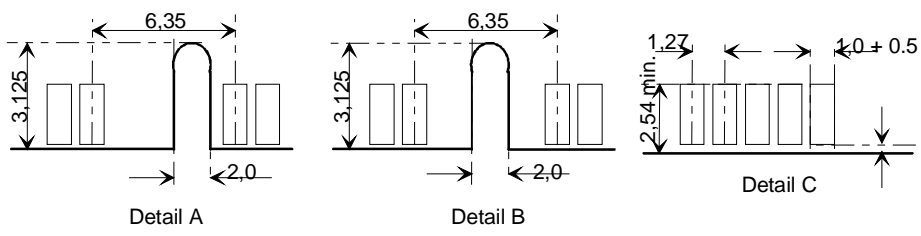
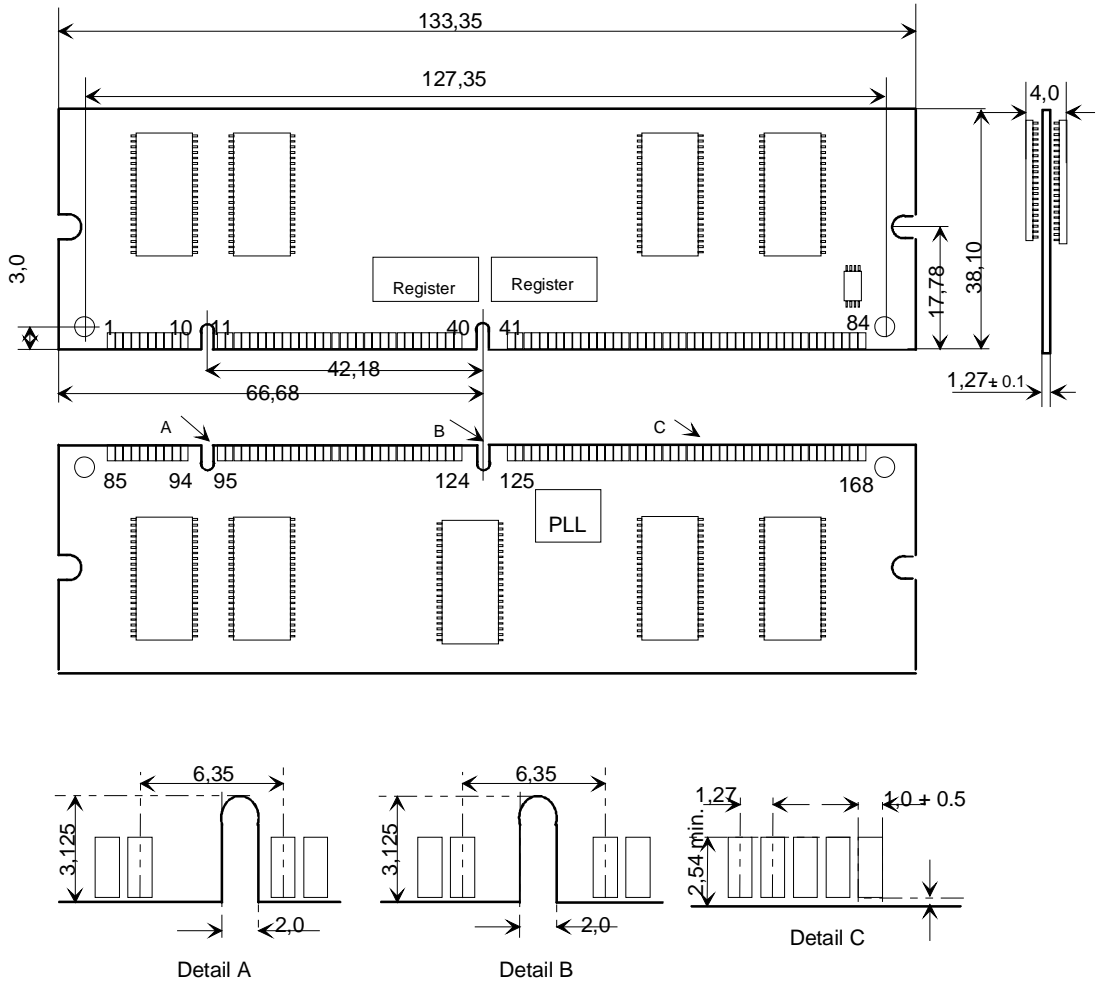
SPD-Table for -8B Registered DIMM Modules with PLL:

Byte#	Description	SPD Entry Value	Hex					
			64MB with PLL 1 bank	128MB with PLL 1 bank	256MB with PLL 2 banks	256MB with PLL 1 bank	512MB with PLL 1 bank	1GB with PLL 2 bank
0	Number of SPD bytes	128	80	80	80	80	80	80
1	Total bytes in Serial PD	256	08	08	08	08	08	08
2	Memory Type	SDRAM	04	04	04	04	04	04
3	Number of Row Addresses (without BS bits)	12 / 13	0C	0C	0C	0D	0D	0D
4	Number of Column Addresses	9 / 10 / 11	09	0A	0A	0A	0B	0B
5	Number of DIMM Banks	1	01	01	02	01	01	02
6	Module Data Width	72	48	48	48	48	48	48
7	Module Data Width (cont'd)	0	00	00	00	00	00	00
8	Module Interface Levels	LVTTL	01	01	01	01	01	01
9	Cycle Time at CL=3	10.0 ns	A0	A0	A0	A0	A0	A0
10	Access time from Clock at CL=3	6.0 ns	60	60	60	60	60	60
11	Dimm Config (Error Det/Corr.)	ECC	02	02	02	02	02	02
12	Refresh Rate/Type	Self-Refresh, 15.6µs	80	80	80	80	80	80
13	SDRAM width, Primary	x4, x8	08	04	04	08	04	04
14	Error Checking SDRAM data width	n/a / x4	08	04	04	08	04	04
15	Minimum tCCD	1 CLK	01	01	01	01	01	01
16	Burst Length supported	1, 2, 4, 8 & full page	8F	8F	8F	8F	8F	8F
17	Number of SDRAM banks	4	04	04	04	04	04	04
18	SDRAM Supported CAS Latencies	2 & 3	06	06	06	06	06	06
19	SDRAM CS Latencies	0	01	01	01	01	01	01
20	SDRAM WE Latencies	0	01	01	01	01	01	01
21	SDRAM DIMM module attributes	with PLL	16	16	16	16	16	16
22	SDRAM Device Attributes	Vcc tol +/- 10%	0E	0E	0E	0E	0E	0E
23	Min. Clock Cycle Time at CL = 2	12 ns	C0	C0	C0	C0	C0	C0
24	Max. data access time from Clock for CL=2	7 ns	70	70	70	70	70	70
25	Min. Clock Cycle Time at CL = 1	not supported	FF	FF	FF	FF	FF	FF

SPD cont'

Byte#	Description	SPD Entry Value	Hex					
			64MB with PLL 1 bank	128MB with PLL 1 bank	256MB with PLL 2 banks	256MB with PLL 1 bank	512MB with PLL 1 bank	1GB with PLL 2 banks
26	Max. Data Access Time from Clock at CL=1	not supp.	FF	FF	FF	FF	FF	FF
27	SDRAM Minimum tRP	30 ns	1E	1E	1E	1E	1E	1E
28	SDRAM Minimum tRRD	20 ns	14	14	14	14	14	14
29	SDRAM Minimum tRCD	20 ns	14	14	14	14	14	14
30	SDRAM Minimum tRAS	60 ns	3C	3C	3C	3C	3C	3C
31	Module Bank Density (per bank)	64/128/256/ 512 MByte	10	20	20	40	80	80
32	SDRAM input setup time	2 ns	20	20	20	20	20	20
33	SDRAM input hold time	1 ns	10	10	10	10	10	10
34	SDRAM data input setup time	2 ns	20	20	20	20	20	20
35	SDRAM data input hold time	1 ns	10	10	10	10	10	10
36-61	Superset information (may be used in future)		FF	FF	FF	FF	FF	FF
62	SPD Revision	1.2	12	12	12	12	12	12
63	Checksum for bytes 0 -62		55	5E	57	87	C0	C1
64-125	Manufacturer's information (FFh if not used)							
126	Frequency Specification	100 Mhz	64	64	64	64	64	64
127	Details of Clocks		8D	8D	8D	8D	8D	8D
128+	Unused storage locations							

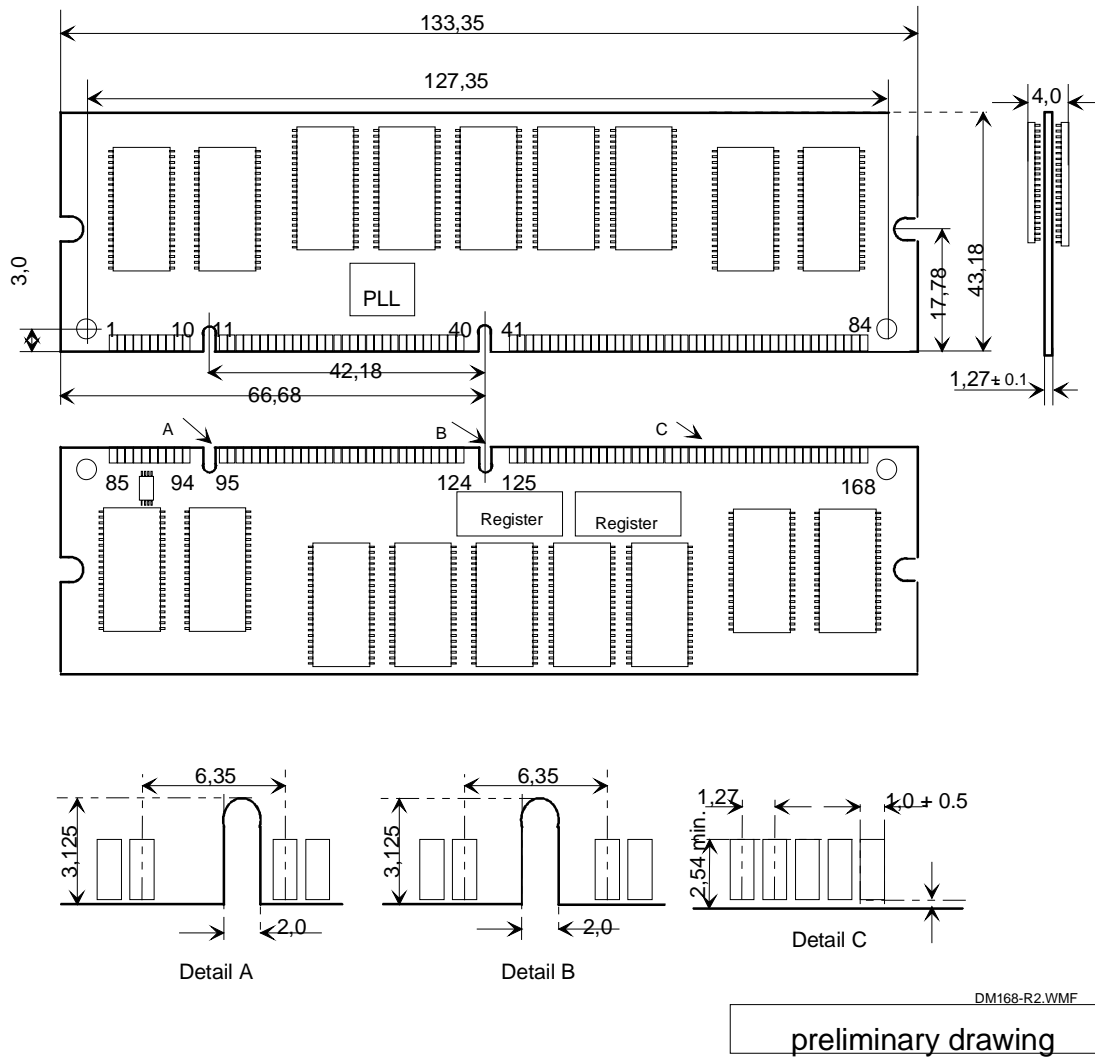
**Module Package
JEDEC MO-161
64 & 256 MByte Registered DIMM Module**



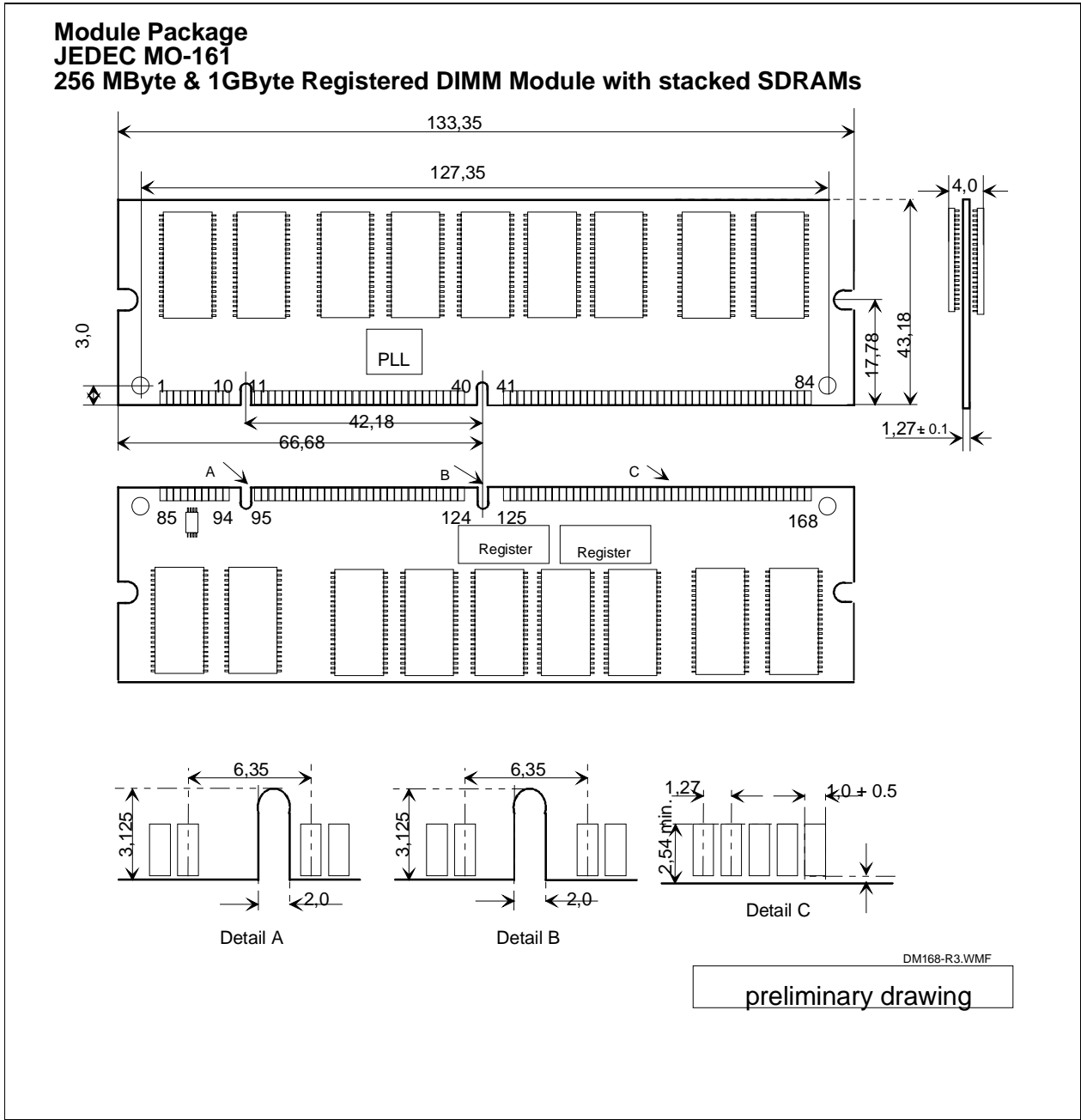
DM168-R1.WMF

preliminary drawing

Module Package
JEDEC MO-161
128 & 512 MByte Registered DIMM Module



Preliminary Information Rev. 1.0/1.1



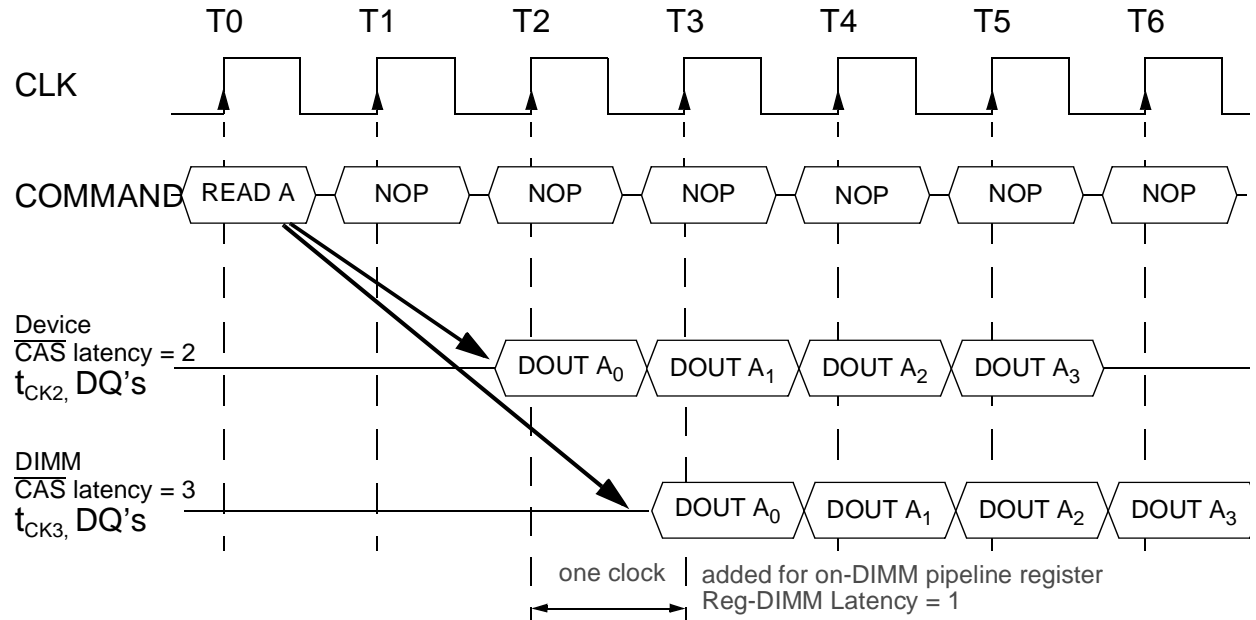
Functional Description

All 168 Pin Registered DIMMs conform to a compatible set of timing and operation characteristics intended to comply with the 100 MHz standards. The Registered DIMMs achieve high speed data transfer rate up to 100 MHz.

All control and address signals are synchronized with the positive edge of externally supplied clocks and are registered on-DIMM and hence delayed by one clock cycle in arriving at the SDRAM devices. The use of the on-board register reduces the capacitive loading of the DIMM on input control and address signals. The SDRAM device data lines (DQ) are connected directly to the DIMM tabs through 10 Ohm series resistors. All the following timing diagrams and explanations show DIMM operation at the tabs, not SDRAM operation.

The picture below depicts an overview of the effect of the Registered Mode on the data outputs (DQs) for a Read operation. Without the registers, the data is delayed according to the device \overline{CAS} latency, in the case two clocks. With the register, the data is delayed according to the device \overline{CAS} latency plus an additional clock cycle. This is known as the DIMM \overline{CAS} latency, and in this example is four clocks. The data path can be thought of as a pipeline in which the register effectively lengthens the pipe by one clock cycle.

Registered DIMM Burst Read Operation (BL=4)



In case of a Burst Write Command the data-in is delayed one clock due to the op-DIMM pipeline register also. Therefore, data for the first Burst Write cycle must be applied on the DQ pins on the next clock cycle after the Write command is issued. The remaining data inputs must be supplied on each subsequent rising clock edge until the burst length is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored.

