
HM62W8128B Series

131,072-word \times 8-bit High Speed CMOS Static RAM

HITACHI

ADE-203-656A (Z)

Rev. 1.0

Oct. 14, 1996

Description

The Hitachi HM62W8128B is a CMOS static RAM organized 131,072-word \times 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8 μ m Hi-CMOS shrink process technology. It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. The device, packaged in a 525-mil SOP (460-mil body SOP) or a 8 mm \times 20 mm TSOP with thickness of 1.2 mm, is available for high density mounting. TSOP package is suitable for cards, and reverse type TSOP is also provided.

Features

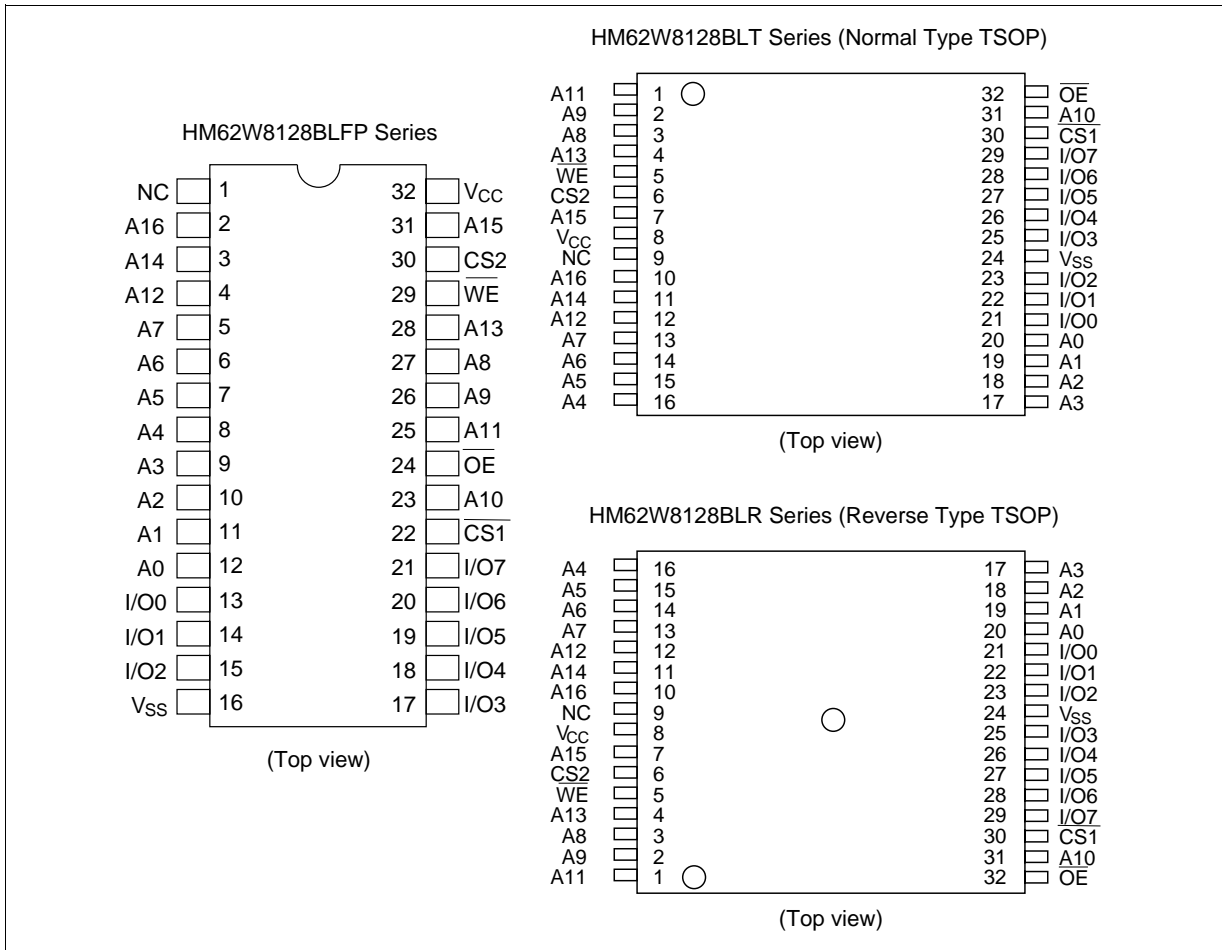
- Single 3.3 V supply
- Fast access time: 100/120 ns (max)
- Power dissipation:
 - Active: 23 mW/MHz (typ)
 - Standby: 4 μ W (typ)
- Completely static memory. No clock or timing strobe required
- Equal access and cycle times
- Common data input and output. Three state output
- Directry CMOS compatible all inputs and outputs.
- Capability of battery backup operation. 2 chip selection for battery backup

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Ordering Information

Type No.	Access time	Package
HM62W8128BLFP-10	100 ns	525-mil 32-pin plastic SOP (FP-32D)
HM62W8128BLFP-12	120 ns	
HM62W8128BLFP-10SL	100 ns	
HM62W8128BLFP-12SL	120 ns	
HM62W8128BLT-10	100 ns	8 mm × 20 mm 32-pin TSOP (normal-bend type) (TFP-32D)
HM62W8128BLT-12	120 ns	
HM62W8128BLT-10SL	100 ns	
HM62W8128BLT-12SL	120 ns	
HM62W8128BLR-10	100 ns	8 mm × 20 mm 32-pin TSOP (reverse-bend type) (TFP-32DR)
HM62W8128BLR-12	120 ns	
HM62W8128BLR-10SL	100 ns	
HM62W8128BLR-12SL	120 ns	

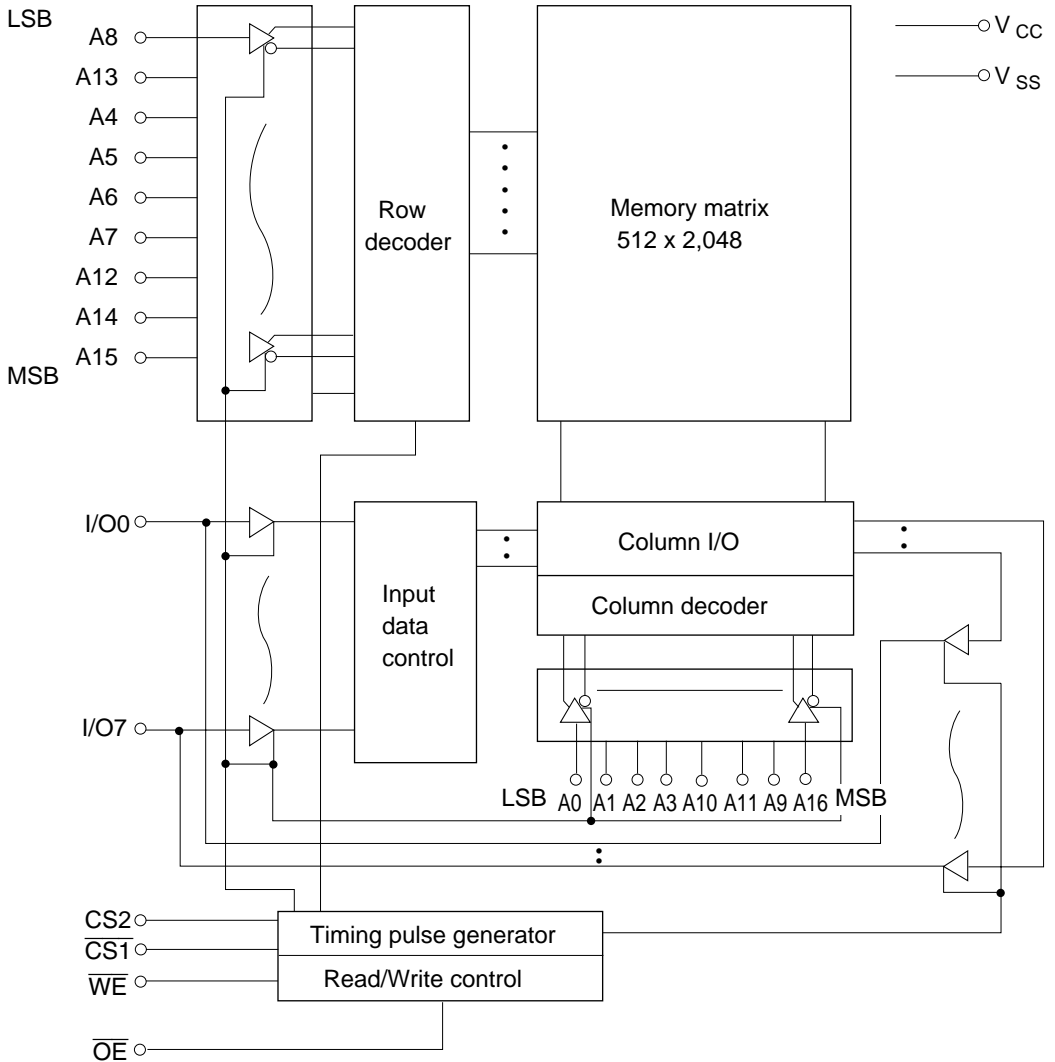
Pin Arrangement



Pin Description

Pin name	Function
A0 to A16	Address input
I/O0 to I/O7	Data input/output
CS1	Chip select 1
CS2	Chip select 2
WE	Write enable
OE	Output enable
NC	No connection
V _{CC}	Power supply
V _{SS}	Ground

Block Diagram



Function Table

\overline{WE}	$\overline{CS1}$	$CS2$	\overline{OE}	Mode	V_{CC} current	I/O pin	Ref. cycle
×	H	×	×	Standby	I_{SB}, I_{SB1}	High-Z	—
×	×	L	×	Standby	I_{SB}, I_{SB1}	High-Z	—
H	L	H	H	Output disable	I_{CC}	High-Z	—
H	L	H	L	Read	I_{CC}	Dout	Read cycle
L	L	H	H	Write	I_{CC}	Din	Write cycle (1)
L	L	H	L	Write	I_{CC}	Din	Write cycle (2)

Note: ×: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage*1	V_{CC}	-0.5 to +4.6	V
Terminal voltage*1	V_T	-0.5*2 to $V_{CC} + 0.3$ *3	V
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C
Storage temperature under bias	T_{bias}	-10 to 85	°C

Notes: 1. Relative to V_{SS}

2. V_T min: -3.0 V for pulse half-width ≤ 30 ns

3. Maximum voltage is 4.6 V

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.0	—	$V_{CC} + 0.3$	V
	V_{IL}	-0.3 *1	—	0.8	V

Note: 1. V_{IL} min: -3.0 V for pulse half-width ≤ 30 ns

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DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ* ¹	Max	Unit	Test conditions
Input leakage current	I _{LI}	—	—	1	μA	V _{in} = V _{SS} to V _{CC}
Output leakage current	I _{LO}	—	—	1	μA	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, V _{I/O} = V _{SS} to V _{CC}
Operating power supply current: DC	I _{CC}	—	6	10	mA	$\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$, Others = V _{IH} /V _{IL} , I _{I/O} = 0 mA
Operating power supply current	HM62W8128B-10 I _{CC1}	—	22	30	mA	Min. cycle, duty = 100%, I _{I/O} = 0 mA, $\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$, Others = V _{IH} /V _{IL}
	HM62W8128B-12 I _{CC1}	—	20	25	mA	
	I _{CC2}	—	7	10	mA	Cycle time = 1 μs, duty = 100%, I _{I/O} = 0 mA, $\overline{CS1} \leq 0.2$ V, $CS2 \geq V_{CC} - 0.2$ V V _{IH} ≥ V _{CC} - 0.2 V, V _{IL} ≤ 0.2 V
Standby power supply current: DC	I _{SB}	—	0.5	1	mA	(1) $\overline{CS1} = V_{IH}$, $CS2 = V_{IH}$ or (2) $CS2 = V_{IL}$
Standby power supply current (1): DC	I _{SB1}	—	1.2* ²	70* ²	μA	0 V ≤ V _{in} (1) 0 V ≤ CS2 ≤ 0.2 V or (2) $\overline{CS1} \geq V_{CC} - 0.2$ V, CS2 ≥ V _{CC} - 0.2 V
	I _{SB1}	—	1.2* ³	30* ³	μA	
Output voltage	V _{OL}	—	—	0.4	V	I _{OL} = 2 mA
		—	—	0.2	V	I _{OL} = 100 μA
	V _{OH}	2.4	—	—	V	I _{OH} = -2 mA
		V _{CC} - 0.2	—	—	V	I _{OH} = -100 μA

Notes: 1. Typical values are at V_{CC} = 3.3 V, Ta = +25°C and not guaranteed.

2. This characteristic is guaranteed only for L version.

3. This characteristic is guaranteed only for L-SL version.

Capacitance (Ta = 25°C, f = 1.0 MHz)

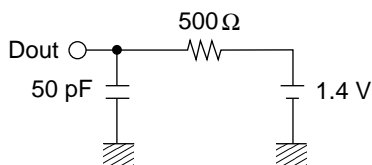
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance* ¹	C _{in}	—	—	8	pF	V _{in} = 0 V
Input/output capacitance* ¹	C _{I/O}	—	—	10	pF	V _{I/O} = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall time: 5 ns
- Input timing reference levels: 1.4 V
- output timing reference levels: 2.0 V/0.8 V
- Output load (Including scope and jig)


Read Cycle

Parameter	Symbol	HM62W8128B				Unit	Notes
		-10		-12			
		Min	Max	Min	Max		
Read cycle time	t_{RC}	100	—	120	—	ns	
Address access time	t_{AA}	—	100	—	120	ns	
Chip selection to output valid	t_{CO1}	—	100	—	120	ns	
	t_{CO2}	—	100	—	120	ns	
Output enable to output valid	t_{OE}	—	50	—	60	ns	
Chip selection to output in low-Z	t_{LZ1}	10	—	10	—	ns	2, 3
	t_{LZ2}	10	—	10	—	ns	
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	ns	2, 3
Chip deselection to output in high-Z	t_{HZ1}	0	35	0	40	ns	1, 2, 3
	t_{HZ2}	0	35	0	40	ns	
Output disable to output in high-Z	t_{OHZ}	0	35	0	40	ns	1, 2, 3
Output hold from address change	t_{OH}	10	—	10	—	ns	

HM62W8128B Series

Write Cycle

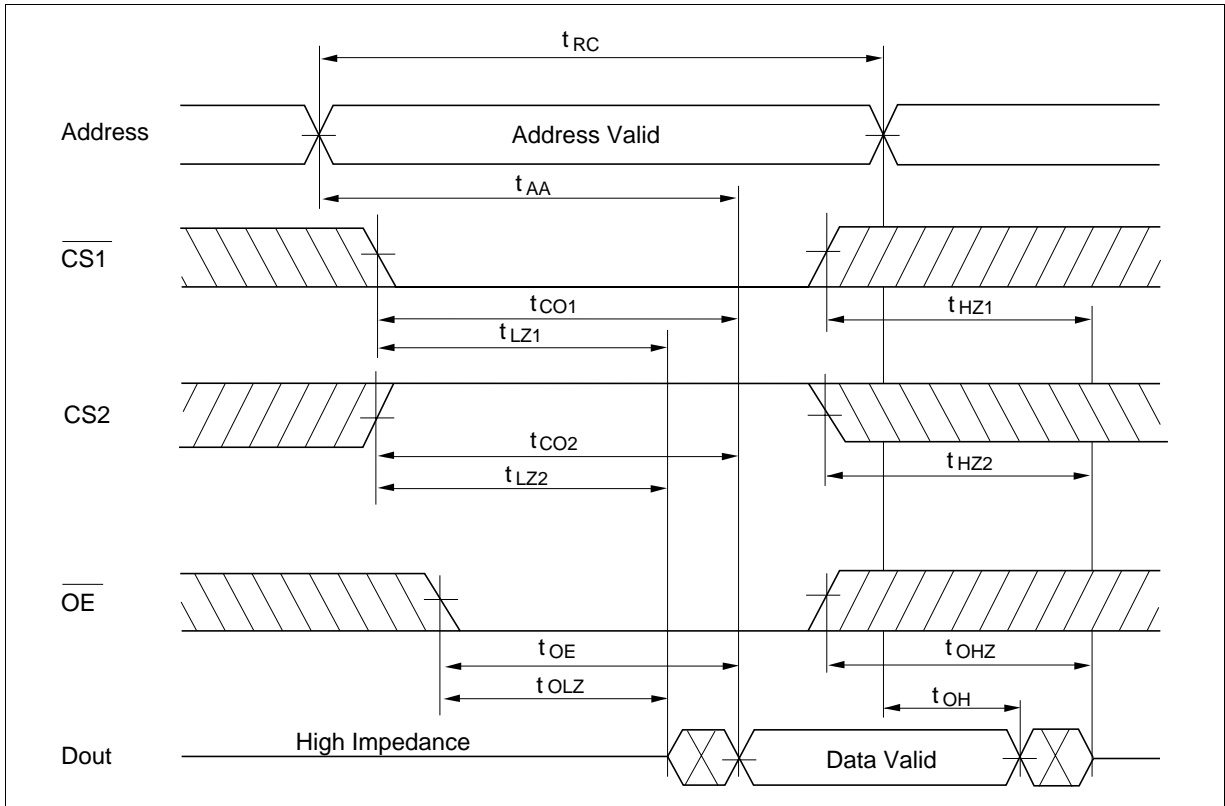
Parameter	Symbol	HM62W8128B				Unit	Notes
		-10		-12			
		Min	Max	Min	Max		
Write cycle time	t_{WC}	100	—	120	—	ns	
Chip selection to end of write	t_{CW}	80	—	85	—	ns	5
Address setup time	t_{AS}	0	—	0	—	ns	6
Address valid to end of write	t_{AW}	80	—	85	—	ns	
Write pulse width	t_{WP}	60	—	65	—	ns	4, 13
Write recovery time	t_{WR}	0	—	0	—	ns	7
Write to output in high-Z	t_{WHZ}	0	35	0	40	ns	1, 2, 8
Data to write time overlap	t_{DW}	40	—	45	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	ns	2
Output disable to output in High-Z	t_{OHZ}	0	35	0	40	ns	1, 2, 8

- Notes:
- t_{HZ} , t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
 - This parameter is sampled and not 100% tested.
 - At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
 - A write occurs during the overlap of a low $\overline{CS1}$, a high CS2, and a low \overline{WE} . A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high, and \overline{WE} going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low, and \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
 - t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
 - t_{AS} is measured from the address valid to the beginning of write.
 - t_{WR} is measured from the earliest of $\overline{CS1}$ or \overline{WE} going high or CS2 going low to the end of write cycle.
 - During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
 - If $\overline{CS1}$ goes low simultaneously with \overline{WE} going low or after \overline{WE} going low, the outputs remain in a high impedance state.
 - Dout is the same phase of the latest written data in this write cycle.
 - Dout is the read data of next address.
 - If $\overline{CS1}$ is low and CS2 high during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
 - In the write cycle with \overline{OE} low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention.

$$t_{WP} \geq t_{DW} \text{ min} + t_{WHZ} \text{ max}$$

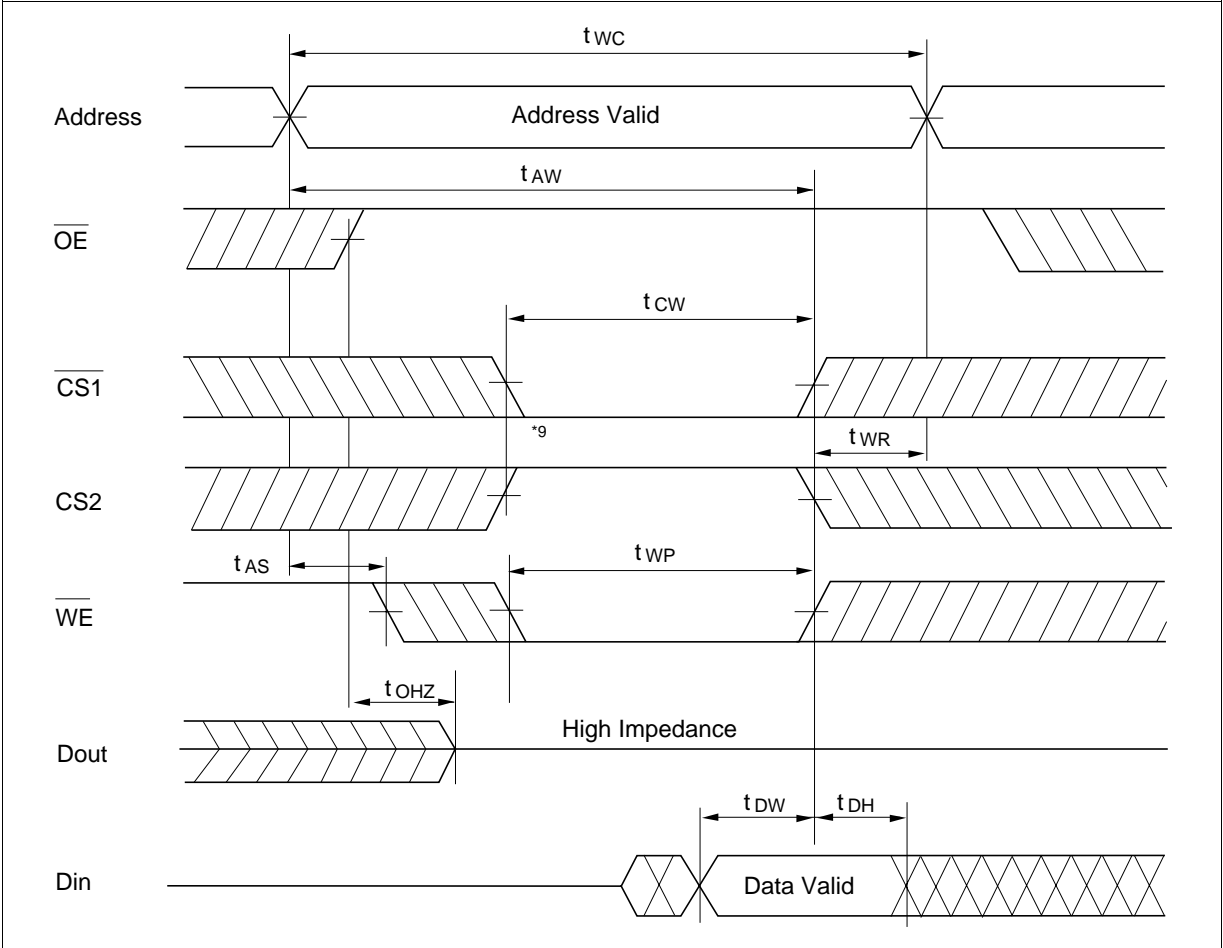
Timing Waveform

Read Timing Waveform ($\overline{WE} = V_{IH}$)

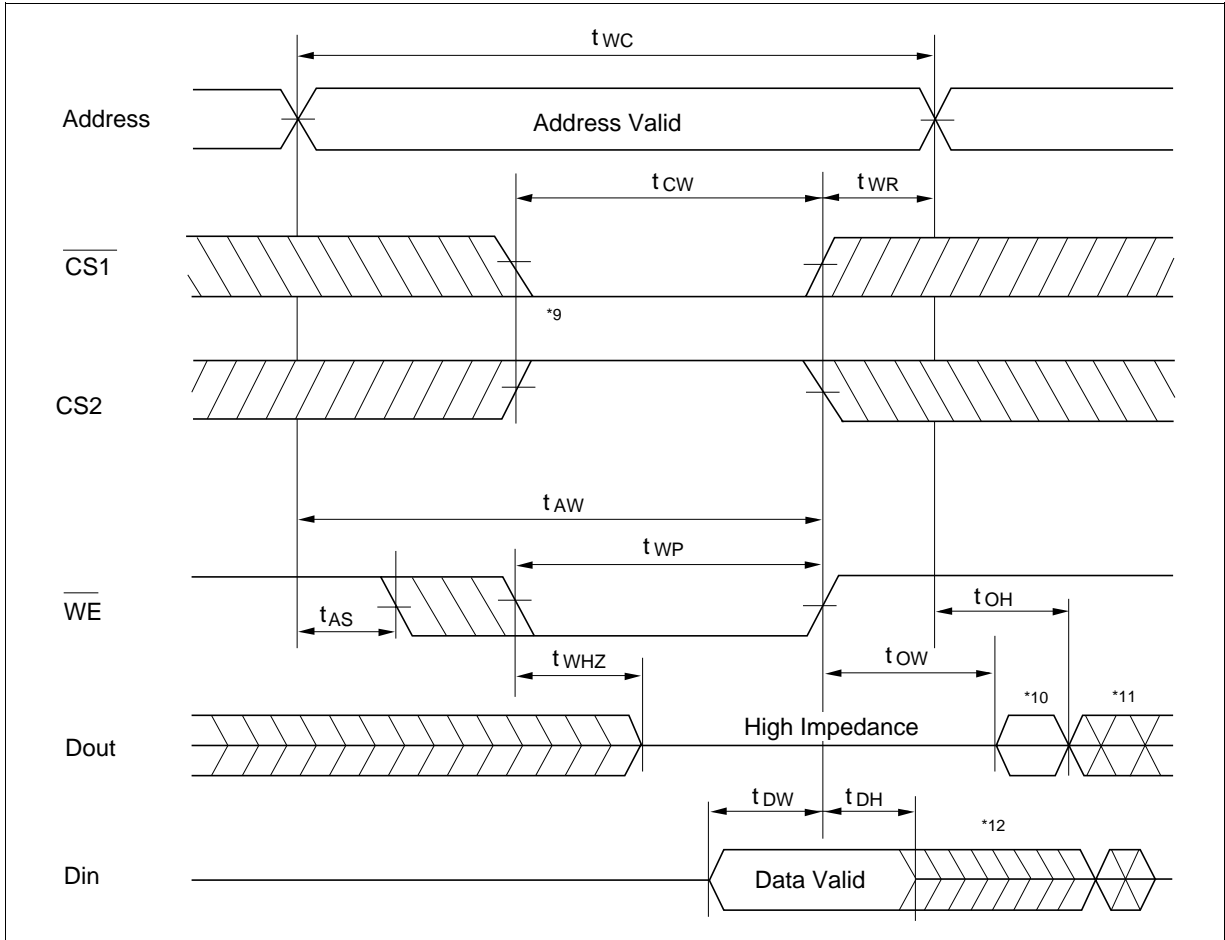


HM62W8128B Series

Write Timing Waveform (1) (\overline{OE} Clock)



Write Timing Waveform (2) (\overline{OE} Low Fixed)

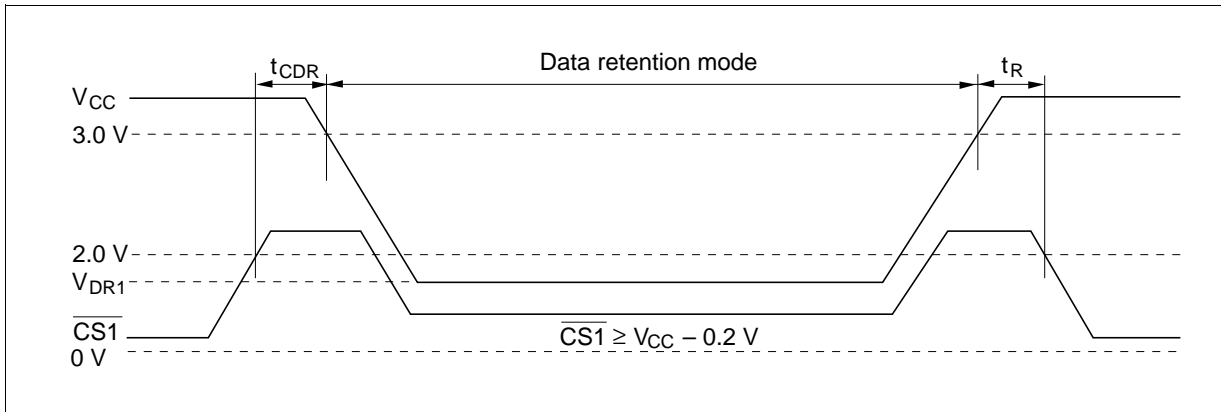


Low V_{CC} Data Retention Characteristics ($T_a = 0$ to $+70^\circ\text{C}$)

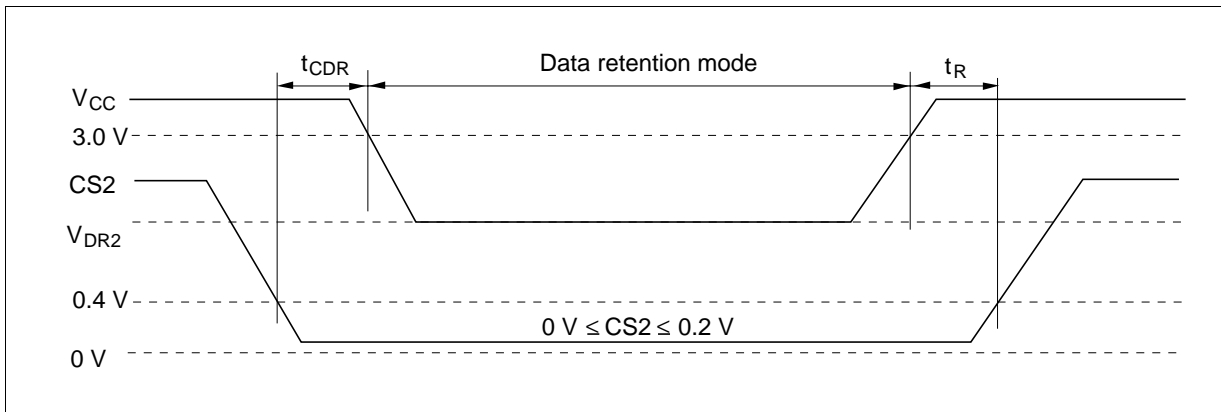
Parameter	Symbol	Min	Typ ^{*4}	Max	Unit	Test conditions ^{*3}
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$V_{in} \geq 0V$ (1) $0V \leq CS2 \leq 0.2V$ or (2) $CS2 \geq V_{CC} - 0.2V$ $CS1 \geq V_{CC} - 0.2V$
Data retention current	I_{CCDR} (L version)	—	1	50^{*1}	μA	$V_{CC} = 3.0V$, $V_{in} \geq 0V$ (1) $0V \leq CS2 \leq 0.2V$ or (2) $CS2 \geq V_{CC} - 0.2V$, $CS1 \geq V_{CC} - 0.2V$
	I_{CCDR} (L-SL version)	—	1	15^{*2}	μA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	5	—	—	ms	

- Notes:
1. This characteristic is guaranteed only for L version, $20\ \mu\text{A}$ max. at $T_a = 0$ to 40°C .
 2. This characteristic is guaranteed only for L-SL version, $3\ \mu\text{A}$ max. at $T_a = 0$ to 40°C .
 3. $CS2$ controls address buffer, \overline{WE} buffer, $\overline{CS1}$ buffer, \overline{OE} buffer, and Din buffer. If $CS2$ controls data retention mode, V_{in} levels (address, \overline{WE} , \overline{OE} , $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, $CS2$ must be $CS2 \geq V_{CC} - 0.2V$ or $0V \leq CS2 \leq 0.2V$. The other input levels (address, \overline{WE} , \overline{OE} , I/O) can be in the high impedance state.
 4. Typical values are at $V_{CC} = 3.0V$, $T_a = +25^\circ\text{C}$ and not guaranteed.

Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)

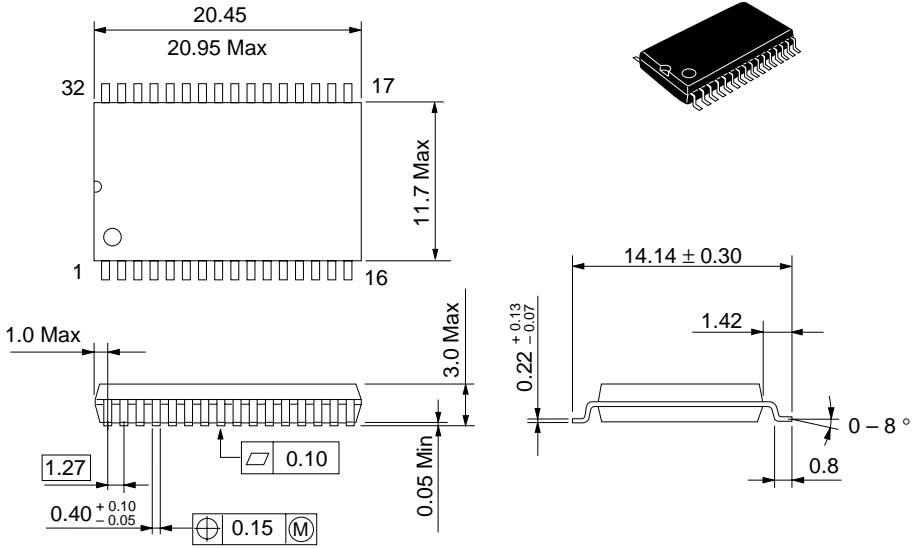


HM62W8128B Series

Package Dimensions

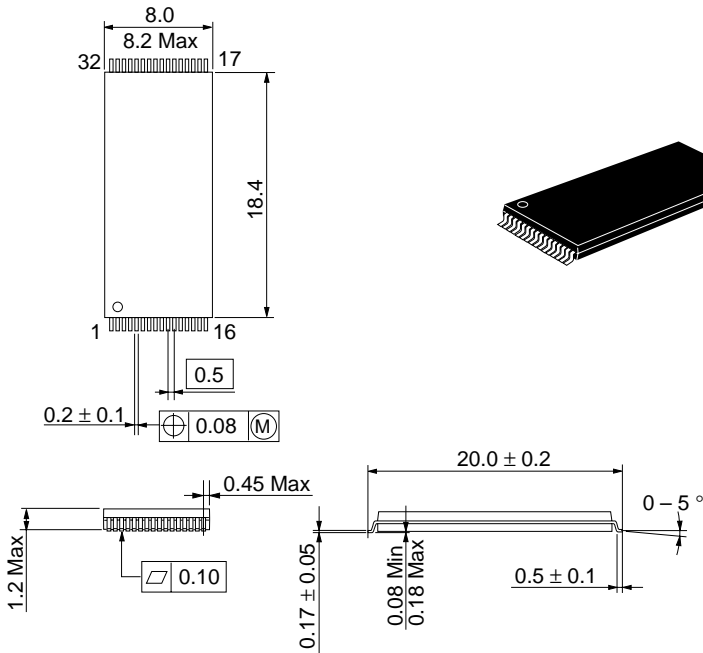
HM62W8128BLFP Series (FP-32D)

Unit: mm



HM62W8128BLT Series (TFP-32D)

Unit: mm

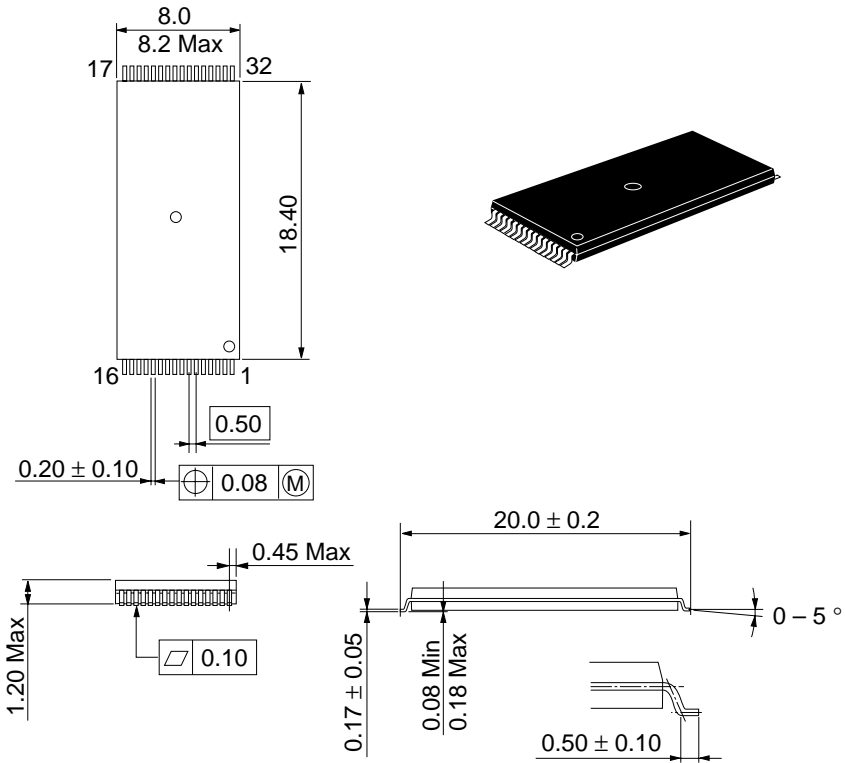


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Package Dimensions (cont.)

HM62W8128BLR Series (TFP-32DR)

Unit: mm



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Revision Record

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1.0	Oct. 14, 1996	Initial issue		
