DATA SHEET

74ALVC573
Octal D-type transparent latch; 3-state

Product specification

2002 Mar 01

Philips Semiconductors

PHILIPS

Octal D-type transparent latch; 3-state 74ALVC573

FEATURES

- Wide supply voltage range from 1.65 to 3.6 V
- Complies with JEDEC standard:
  JESD8-7 (1.65 to 1.95 V)
  JESD8-5 (2.3 to 2.7 V)
  JESD8B/JESD36 (2.7 to 3.6 V).
- 3.6 V tolerant inputs/outputs
- CMOS low power consumption
- Direct interface with TTL levels (2.7 to 3.6 V)
- Power-down mode
- Latch-up performance exceeds ≤250 mA
- ESD protection:
  2000 V Human Body Model (JESD22-A114-A)
  200 V Machine Model (JESD22-A115-A).

DESCRIPTION

The 74ALVC573 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74ALVC573 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all internal latches.

The 74ALVC573 consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the D_n inputs enters the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When $\overline{OE}$ is LOW, the contents of the 8 latches are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches.

The ‘573’ is functionally identical to the ‘373’, but the ‘373’ has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay inputs D_n to output Q_n	V_{CC} = 1.8 V; C_L = 30 pF; R_L = 1 kΩ	3.0	ns
		V_{CC} = 2.5 V; C_L = 30 pF; R_L = 500 Ω	2.3	ns
		V_{CC} = 2.7 V; C_L = 50 pF; R_L = 500 Ω	2.4	ns
		V_{CC} = 3.3 V; C_L = 50 pF; R_L = 500 Ω	2.2	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per buffer	V_{CC} = 3.3 V; notes 1 and 2		
		outputs enabled	37	pF
		outputs disabled	7	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC573D	20	SO	plastic	SOT163-1
74ALVC573PW	20	TSSOP	plastic	SOT360-1

FUNCTION TABLE

See note 1.

OPERATING MODES	INPUT			INTERNAL LATCHES	OUTPUT
	$\overline{OE}$	LE	D_n		Q_0 to Q_7
Enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

Note

1. H = HIGH voltage level;
   h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;
   L = LOW voltage level;
   l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition;
   Z = high-impedance OFF-state.

PINNING

PIN	SYMBOL	DESCRIPTION
1	$\overline{OE}$	output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D_0 to D_7	data inputs
12, 13, 14, 15, 16, 17, 18, 19	Q_7 to Q_0	3-state latch outputs
10	GND	ground (0 V)
11	LE	latch enable input (active HIGH)
20	V_{CC}	supply voltage

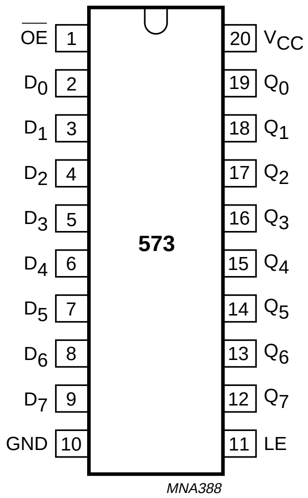


Fig.1 Pin configuration.

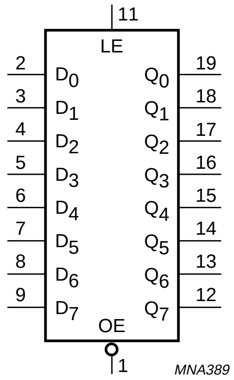


Fig.2 Logic symbol.

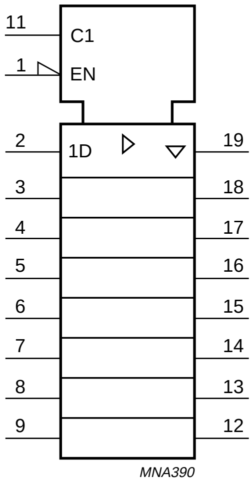


Fig.3 IEE/IEC logic symbol.

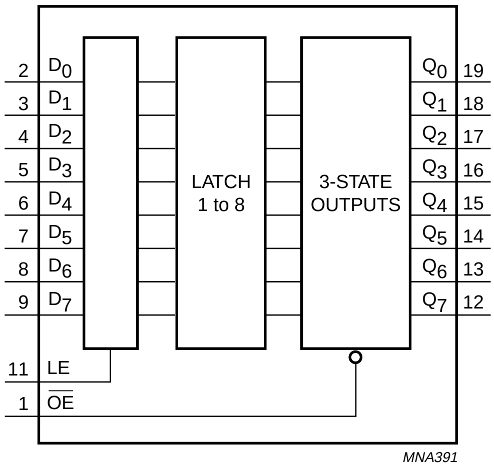


Fig.4 Function diagram.

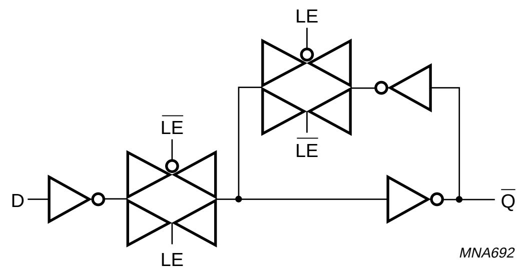


Fig.5 Logic diagram (one latch).

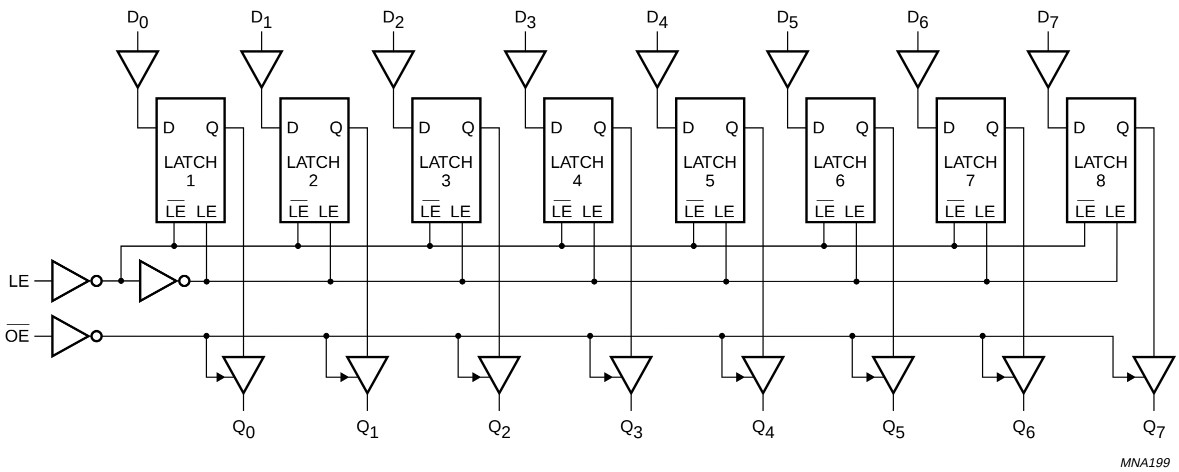


Fig.6 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		1.65	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	V_{CC} = 1.65 to 3.6 V; enable mode	0	V_{CC}	V
		V_{CC} = 1.65 to 3.6 V; disable mode	0	3.6	V
		V_{CC} = 0 V; Power-down mode	0	3.6	V
T_{amb}	operating ambient temperature		–40	+85	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.65 to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 to 3.6 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+4.6	V
I_{IK}	input diode current	$V_I < 0$	–	–50	mA
V_I	input voltage		–0.5	+4.6	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$	–	±50	mA
V_O	output voltage	enable mode; notes 1 and 2	–0.5	V_{CC} + 0.5	V
		disable mode	–0.5	+4.6	V
		Power-down mode; note 2	–0.5	+4.6	V
I_O	output diode current	V_O = 0 to V_{CC}	–	±50	mA
I_{GND}, I_{CC}	V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation per package				
	SO package	above 70 °C derate linearly with 8 mW/K	–	500	mW
	TSSOP package	above 60 °C derate linearly with 5.5 mW/K	–	500	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. When V_{CC} = 0 V (Power-down mode), the output voltage can be 3.6 V in normal operation.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)			UNIT
		OTHER	V_{CC} (V)	–40 to +85			
				MIN.	TYP.[1]	MAX.	
V_{IH}	HIGH-level input voltage		1.65 to 1.95	$0.65 \times V_{CC}$	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2	–	–	V
V_{IL}	LOW-level input voltage		1.65 to 1.95	–	–	$0.35 \times V_{CC}$	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; I_O = 100 μA	1.65 to 3.6	–	–	0.2	V
		$V_I = V_{IH}$ or V_{IL}; I_O = 6 mA	1.65	–	–	0.3	V
		$V_I = V_{IH}$ or V_{IL}; I_O = 12 mA	2.3	–	–	0.4	V
		$V_I = V_{IH}$ or V_{IL}; I_O = 18 mA	2.3	–	–	0.6	V
		$V_I = V_{IH}$ or V_{IL}; I_O = 12 mA	2.7	–	–	0.4	V
		$V_I = V_{IH}$ or V_{IL}; I_O = 18 mA	3.0	–	–	0.4	V
		$V_I = V_{IH}$ or V_{IL}; I_O = 24 mA	3.0	–	–	0.55	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; I_O = –100 μA	1.65 to 3.6	V_{CC} – 0.2	–	–	V
		$V_I = V_{IH}$ or V_{IL}; I_O = –6 mA	1.65	1.25	–	–	V
		$V_I = V_{IH}$ or V_{IL}; I_O = –12 mA	2.3	1.8	–	–	V
		$V_I = V_{IH}$ or V_{IL}; I_O = –18 mA	2.3	1.7	–	–	V
		$V_I = V_{IH}$ or V_{IL}; I_O = –12 mA	2.7	2.2	–	–	V
		$V_I = V_{IH}$ or V_{IL}; I_O = –18 mA	3.0	2.4	–	–	V
		$V_I = V_{IH}$ or V_{IL}; I_O = –24 mA	3.0	2.2	–	–	V
I_I	input leakage current	V_I = 3.6 V or GND	3.6	–	±0.1	±5	μA
I_{OZ}	3-state output OFF-state current	$V_I = V_{IH}$ or V_{IL}; V_O = 3.6 V or GND; note 2	1.65 to 3.6	–	0.1	±10	μA
I_{off}	power OFF leakage current	V_I or V_O = 0 to 3.6 V	0.0	–	±0.1	±10	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0	3.6	–	0.2	10	μA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC}$ – 0.6 V; I_O = 0	3.0 to 3.6	–	5	750	μA

Notes

1. All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.
2. For transceivers, the parameter I_{OZ} includes the input leakage current.

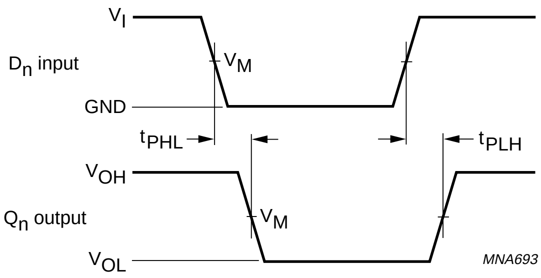
AC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)			UNIT
		WAVEFORMS	V_{CC} (V)	−40 to +85			
				MIN.	TYP.[1]	MAX.	
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n	see Figs 7 and 11	1.65 to 1.95	1.0	2.5	5.4	ns
			2.3 to 2.7	1.0	2.0	3.5	ns
			2.7	1.0	2.3	3.6	ns
			3.0 to 3.6	1.0	2.2	3.3	ns
t_{PHL}/t_{PLH}	propagation delay LE to Q_n	see Figs 8 and 11	1.65 to 1.95	1.0	2.8	6.0	ns
			2.3 to 2.7	1.0	2.1	3.8	ns
			2.7	1.0	2.4	3.7	ns
			3.0 to 3.6	1.0	2.3	3.3	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n	see Figs 9 and 11	1.65 to 1.95	1.5	3.0	6.4	ns
			2.3 to 2.7	1.0	2.4	4.5	ns
			2.7	1.5	3.0	4.6	ns
			3.0 to 3.6	1.0	2.3	4.0	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n	see Figs 9 and 11	1.65 to 1.95	1.5	3.4	7.0	ns
			2.3 to 2.7	1.0	2.2	4.4	ns
			2.7	1.5	2.8	4.4	ns
			3.0 to 3.6	1.0	2.7	4.4	ns
t_W	LE pulse with HIGH	see Figs 8 and 11	1.65 to 1.95	3.8	–	–	ns
			2.3 to 2.7	3.3	–	–	ns
			2.7	3.3	–	–	ns
			3.0 to 3.6	3.3	–	–	ns
t_{su}	set-up time D_n to LE	see Figs 10 and 11	1.65 to 1.95	0.8	–	–	ns
			2.3 to 2.7	0.8	–	–	ns
			2.7	0.8	–	–	ns
			3.0 to 3.6	0.8	–	–	ns
t_h	hold time D_n to LE	see Figs 10 and 11	1.65 to 1.95	0.8	–	–	ns
			2.3 to 2.7	0.8	–	–	ns
			2.7	0.8	–	–	ns
			3.0 to 3.6	0.7	–	–	ns

Note

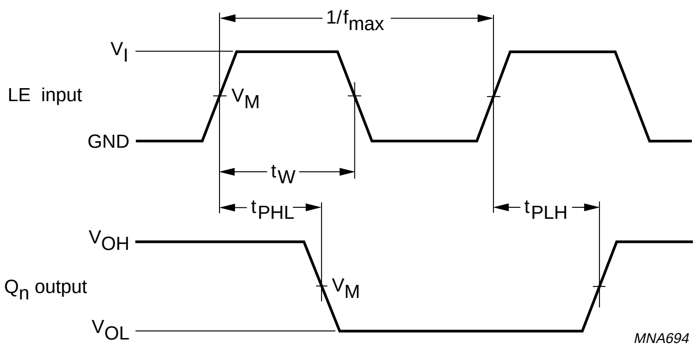
1. All typical values are measured at T_{amb} = 25 °C.

AC WAVEFORMS



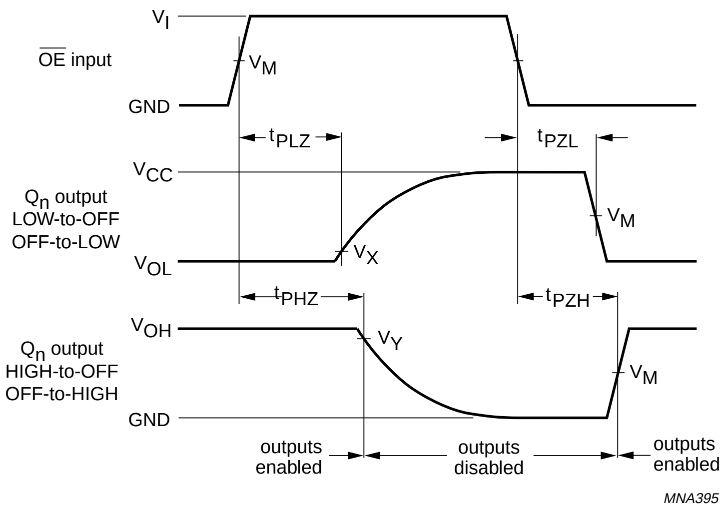
V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.65 to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.3 to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

Fig.7 Input D_n to output Q_n propagation delay times.



V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.65 to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.3 to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

Fig.8 Latch Enable (LE) input pulse width, and latch enable input to output (Q_n) propagation delays.

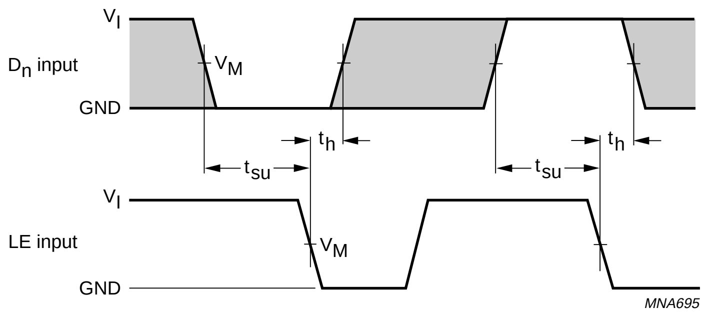


V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.65 to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.3 to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

$V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V;
$V_X = V_{OL} + 0.15$ V at $V_{CC} < 2.7$ V;
$V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V;
$V_Y = V_{OH} - 0.15$ V at $V_{CC} < 2.7$ V.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

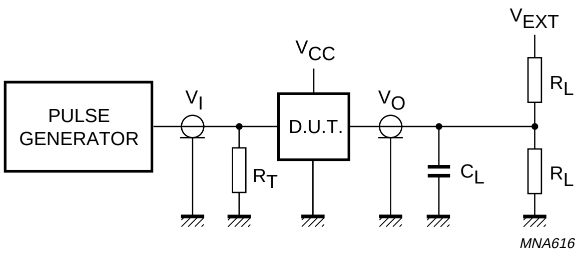
Fig.9 3-state enable and disable times.



V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.65 to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.3 to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.10 Data set-up and hold times for D_n input to LE input.



V_{CC}	V_I	C_L	R_L	V_{EXT}		
				t_{PLH}/t_{PHL}	t_{PZH}/t_{PHZ}	t_{PZL}/t_{PLZ}
1.65 to 1.95 V	V_{CC}	30 pF	1 kΩ	open	GND	$2 \times V_{CC}$
2.3 to 2.7 V	V_{CC}	30 pF	500 Ω	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	50 pF	500 Ω	open	GND	6 V
3.0 to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	6 V

R_L = Load resistor.

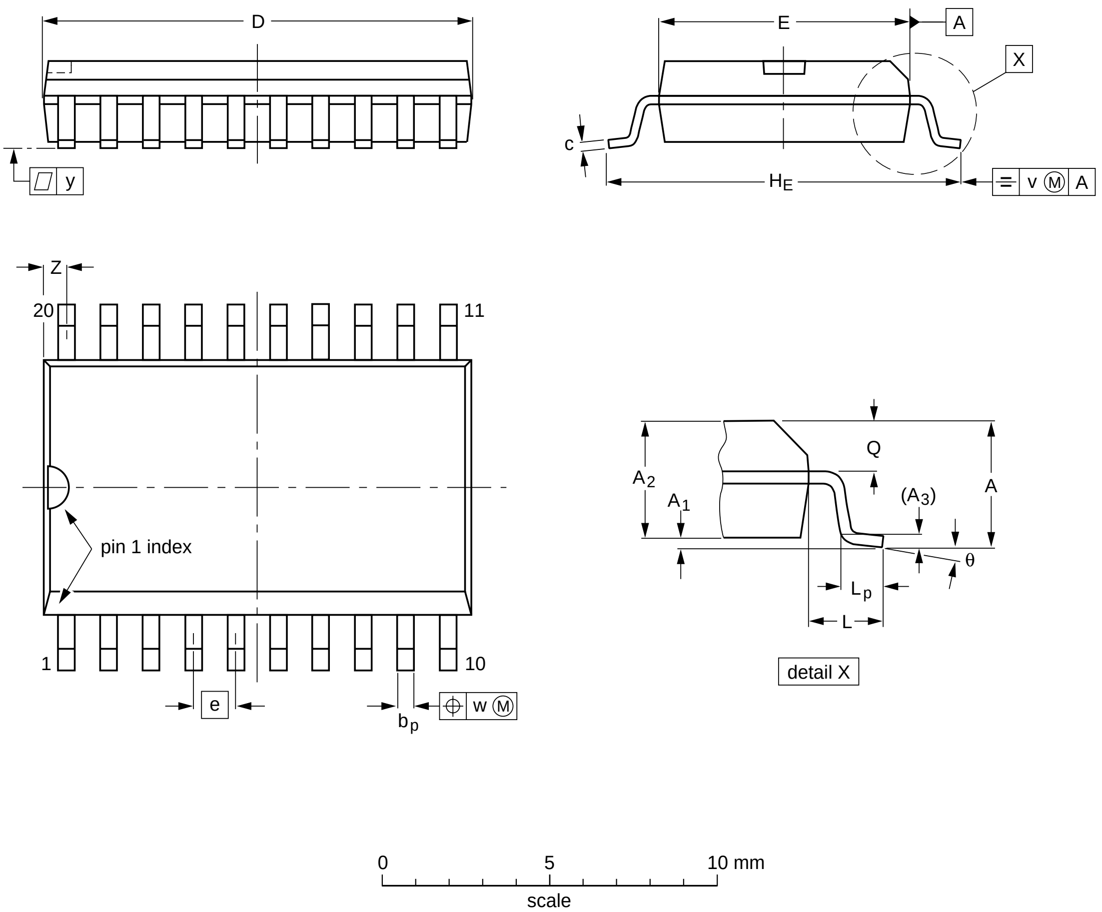
C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.11 Load circuitry for switching times.

PACKAGE OUTLINES

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

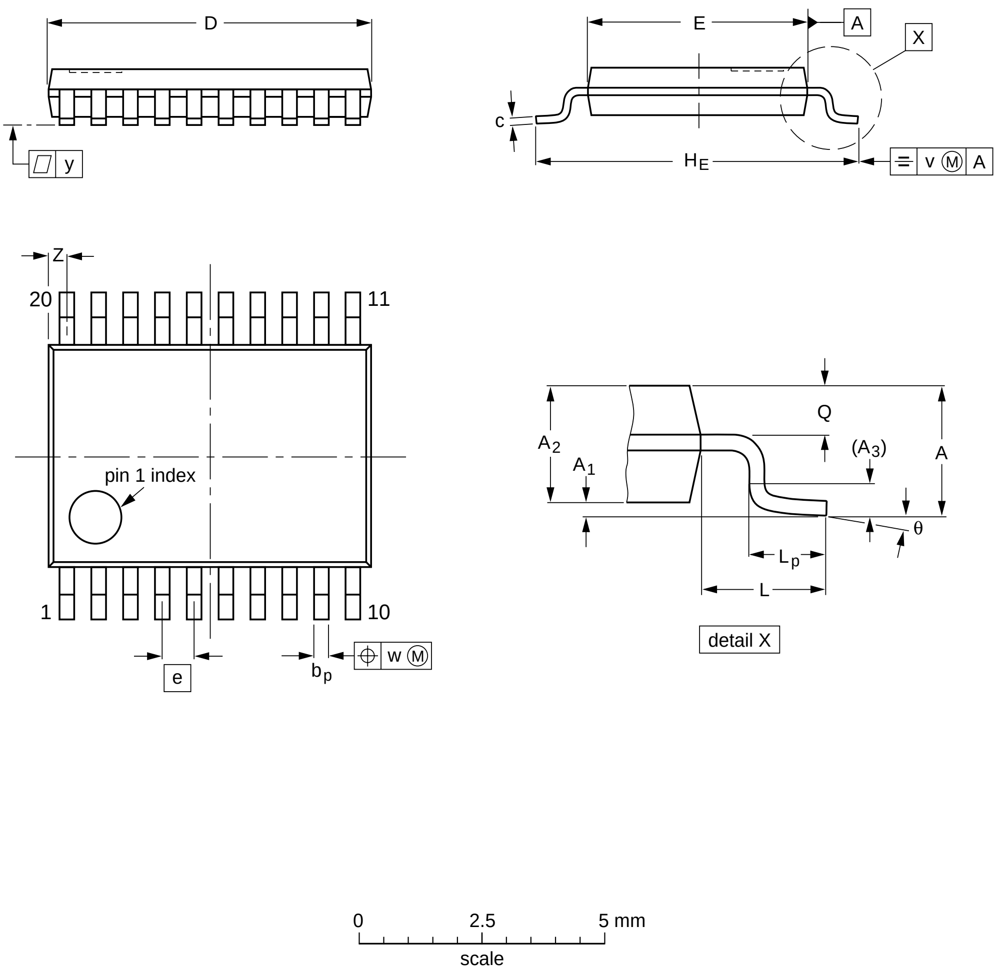
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013				~~97-05-22~~ 99-12-27

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153				~~95-02-04~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[(1)]
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable[(2)]	suitable
PLCC[(3)], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[(3)(4)]	suitable
SSOP, TSSOP, VSO	not recommended[(5)]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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SCA74

Printed in The Netherlands 613508/01/pp20 Date of release: 2002 Mar 01 Document order number: 9397 750 09452

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