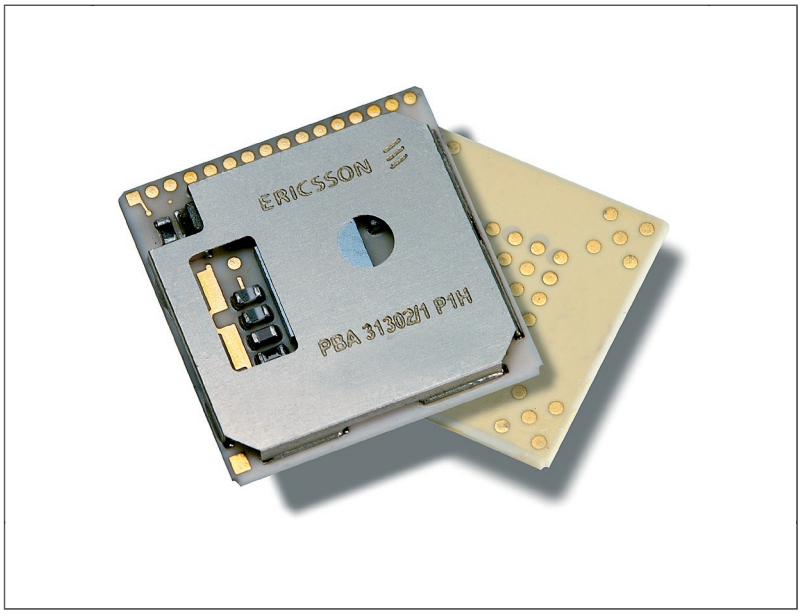
Bluetooth™ Radio

Key features

- A small complete class 1 Bluetooth Radio, no additional RF-components required
- Variable reference frequency, 10 MHz-20 MHz
- Excellent out-band blocking in all GSM bands
- High signal level performance in-band
- Requires no external shielding
- On board software controlled output power
- Qualified for Bluetooth specification 1.1



Description

The Bluetooth Radio PBA 313 02 from Ericsson Microelectronics is a long-range microwave frequency radio transceiver for Bluetooth communication links. Provided in a compact LGA package. No external shield is required.

The Bluetooth Radio offers a combination of compact size, low power consumption, and cost effective assembly. The PBA 313 02 forms a complete radio with only the addition of an antenna, a reference frequency, and digital control. As a result, designers can benefit from a pre-tested and ready-to-use device, providing a robust Bluetooth Radio function in the final OEM application.

PBA 313 02 is built around a BiCMOS ASIC. Antenna filter, RX and TX baluns are all integrated into the circuit. The antenna filter is specially designed for application in GSM environment such as inside a mobile phone. The PBA 313 02 has output power regulation control through software. Power levels have typical 4dB steps. Power control flexibility enables customer to specify smaller or larger power steps. Operating from a 2.7 V supply, the module has a typical supply current consumption of only 60 mA (receive mode) or 50 mA (transmit mode) at 0 dBm output power. In Standby mode the typical current consumption is only 20 µA thus helping to extend battery life for portable equipment.

Suggested applications

- Mobile phones
- PDA
- Modems
- Laptop computers
- Handheld equipment

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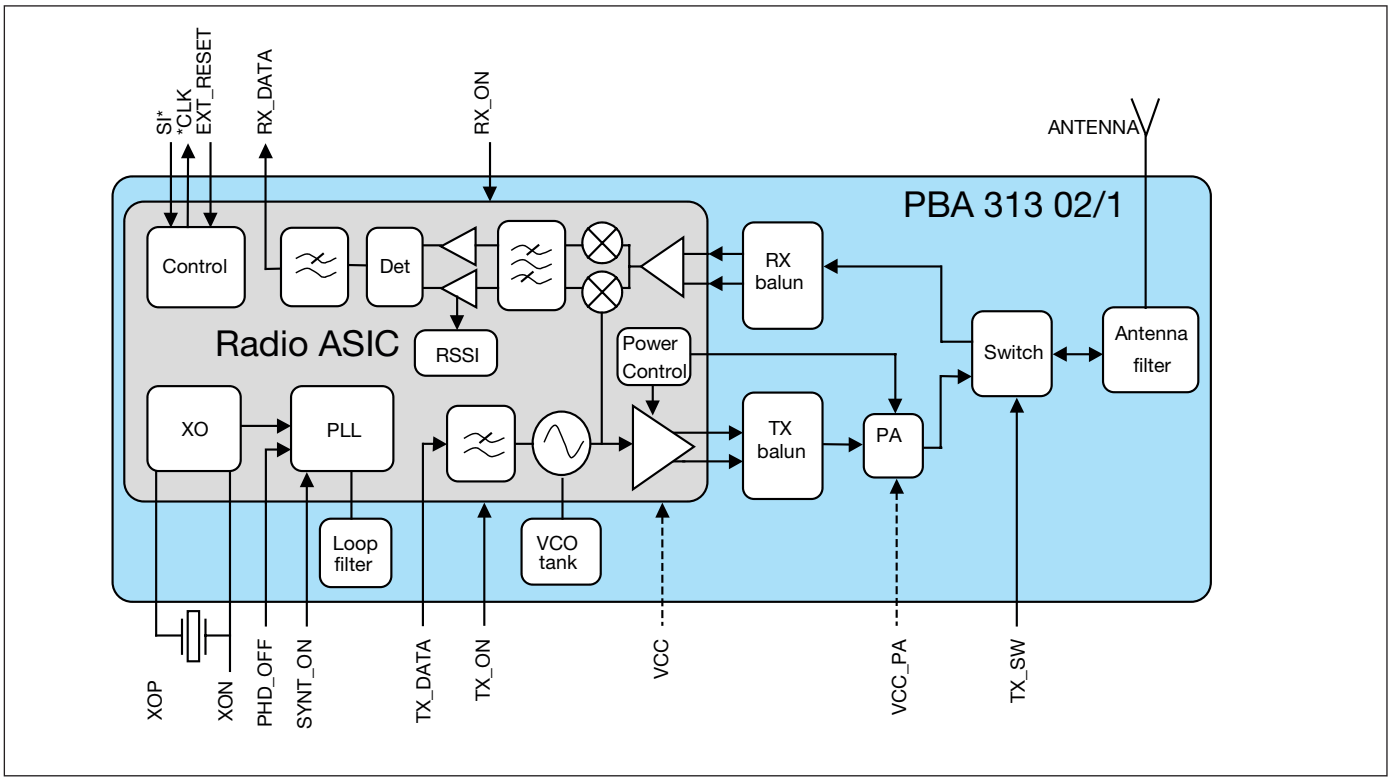


Figure 1. Block diagram

Limiting data

The absolute maximum ratings of the PBA 313 02 are summarised in Table 1.
Unless otherwise noted, whenever VCC is mentioned it also includes VCC_DIG.

Absolute maximum ratings

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Supply voltage		VCC[1]	2.65		3.0	V
PA Supply voltage		VCC_PA	2.7		5.5	V
Applied voltage to non supply pins			GND -0.3		Vcc +0.3	V
Input RF power	In-band				15	dBm
	Out-band				15	dBm
Storage temperature		T_{Stg}	-40		+90	°C
Max operating temperature			-30		+75	°C
Reference clock frequency		(f_{EXT_CLK})	10		20	MHz
Reference clock amplitude			0.3		1.0	Vpp
Max. load mismatch tolerant, stability					TBD	

Characteristic data

Unless otherwise noted, the specification applies forT_{Amb}=25°C, VCC =2.8V, f_{Ref} = 13MHz, ±10ppm, VSWR ≤ 2:1, VCC_PA =3.2V

Operating conditions

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Frequency range			2.402		2.480	GHz
Reference clock frequency	1)	f_{EXT_CLK}	12.99987		13.00013	MHz
Reference clock frequency tolerance		f_{EXT_CLK}			10	ppm
Reference clock amplitude			0.8			Vpp
Reference clock phase noice	Δf = 15 kHz				-110	dBc/Hz
Supply voltage VCC			2.7	2.775	3.0	V
Supply voltage VCC_PA				3.2	4.2	V
Crystal tolerance	2)				±20	ppm
Output matching of ANT pin		VSWR			2:1	
Antenna load				50		Ω
Logical input high		V_{IH}	0.9× VCC		VCC +0.3	V
Logical input low		V_{IL}	-0.3		+0.3	V
Rise/Fall time of all digital inputs			2		20	ns
Clock frequency of SI_CLK					4	MHz
Positive period of SI_CLK			76			ns
Operating temperature		T_{Amb}	-20	+25	+55	°C

1) If an external clock input is used then the XO_N crystal input can be used. The external clock should be AC coupled into the XO_N input and the XO_P input shall be left unconnected.

2) Crystal frequency can be trimmed by writing a 6-bit value to the XO_trim register in order to get ±10 ppm frequency tolerance.

DC and low frequency specifications

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Supply current	Transmit mode 3)			50		
	Receive mode			60		mA
	Idle mode 4)			20	50	µA
XO_N input capacitance				3		pF
XO_P input capacitance				3		pF
XO_N Trim capacitance each step	Max 63 steps (6bits)			0.4		pF
XO_P Trim capacitance each step	Max 63 steps (6bits)			0.4		pF
Capacitance of all digital inputs				3		pF
Input leakage current	0.5< V_{IN}<(VCC -0.5)			5		µA
Rise/Fall time of digital outputs 5)			2		20	ns
Rise/Fall time of RX Data	15kΩ+15pF			20		ns
Logical output high		V_{OH}	0.9×Vcc		VCC	V
Logical output low		V_{OL}	-0.3	0	+0.3	V
SYS_CLK frequency				f_{EXT_CLK}		MHz
TX_CLK frequency				1.0		MHz
LPO_CLK frequency				3.2		kHz
LPO_CLK frequency tolerance				250		ppm

3) See Table 2.

4) After at least 200 ms from shut down

5) Driving a 10 pF load.

Receiver performance

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Frequency Range		f_{Range}	2.402		2.480	GHz
Input and output impedance of ANT pin				50		Ω
Input matching of ANT pin (VSWR) [6]				2:1		
Sensitivity level [2]	BER = 0.1% Carrier offset = ±75 kHz Frequency dev = 160kHz		-83	-86		dBm
Max input level	BER = 0.1%			+14		dBm
RSSI value (See Table 1)						
Co-Channel interference, $C/I_{co\text{-}channel}$			11			dB
Adjacent (±1 MHz) interference, C/I_{1MHz}			0			dB
Adjacent (±2 MHz) interference, C/I_{2MHz}			-30			dB
Adjacent (±3 MHz) interference, $C/I_{\geq 3MHz}$			-40			dB
Image frequency interference, C/I_{image} [7]			-9			dB
Adjacent (1MHz) interference to in-band Image frequency, $C/I_{image+1MHz}$ [7]			-20			dB
Intermodulation rejection [7]			-39			dBm
LO leakage					-47	dBm
Spurious emission	30 MHz – 1 GHz		-47			dBm
	1 GHz – 12.75 GHz		-47			dBm
Out-of-band blocking [7]	30-880 MHz [10]			+11		dBm
	880-915 MHz [10]			+11		dBm
	915-1710 MHz [10]			+11		dBm
	1710-1785 MHz [10]			+11		dBm
	1785-1850 MHz [10]			+11		dBm
	1850-1980 MHz [10]			+11		dBm
	1980-2000 MHz [10]			+11		dBm
	2000-2100 MHz [10]			0		dBm
	2100-2200 MHz [10]			-10		dBm
	2200-2300 MHz [10]			-13	-27	dBm
	2300-3000 MHz [10]			-15	-27	dBm
	3000-12750 MHz [10,11]			-5	-10	dBm

[6] RX_ON must be high.

[7] PX_ON high and 0xBF written to the Enable register.

[8] Carrier signal level of –67 dBm, interferer Bluetooth modulated

[9] Carrier signal level of –60 dBm, interferer Bluetooth modulated

[10] Carrier signal level of –67 dBm, Continuous Wave (CW) interferer.

[11] Using two exemptions according to the BT specification

Table 1, RSSI performance

RSSI register value	Min	Typ	Max	Unit
0	-85	-85	-79	dBm
1	-83	-81	-78	dBm
2	-81	-80	-76	dBm
3	-80	-78	-75	dBm
4	-79	-77	-74	dBm
5	-78	-76	-73	dBm
6	-77	-75	-72	dBm
7	-76	-74	-70	dBm
8	-74	-72	-69	dBm
9	-72	-70	-66	dBm
10	-69	-68	-64	dBm
11	-67	-66	-62	dBm
12	-66	-64	-61	dBm
13	-65	-63	-60	dBm
14	-64	-62	-59	dBm
15	-63	-61	-59	dBm

RSSI register value	Min	Typ	Max	Unit
16	-62	-60	-57	dBm
17	-61	-59	-56	dBm
18	-60	-58	-54	dBm
19	-58	-56	-53	dBm
20	-57	-54	-52	dBm
21	-54	-53	-49	dBm
22	-53	-51	-48	dBm
23	-52	-50	-46	dBm
24	-51	-49	-46	dBm
25	-50	-48	-45	dBm
26	-50	-47	-44	dBm
27	-49	-46	-44	dBm
28	-48	-45	-43	dBm
29	-47	-44	-41	dBm
30	-45	-43	-40	dBm
31	-44	-41	-39	dBm

Transmitter performance

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Maximum TX power [15]			14	17	20	dBm
Minimum TX power [15]					+4	dBm
Output power step size			2		8	dBm
Frequency accuracy (excluding crystal accuracy)					25	kHz
Frequency deviation [12]						
0000111100001111 pattern			140		175	kHz
Minimum frequency deviation [12], 010101 pattern			115			kHz
TX carrier drift	1 slot [13] (366 µs)	f_{Drift1}			±25	kHz
	3 slots (1598 µs)	f_{Drift1}			±40	kHz
	5 slots (2862 µs)	f_{Drift1}			±40	kHz
Drift rate [14]					400	Hz/µs
20 dB bandwidth with peak det.					1	MHz
Adjacent channel power	±2 MHz				-20	dBm
	±3 MHz				-40	dBm
	±4 MHz				-40	dBm
Spurious emissions	Harmonics,				-30	dBm
	non-harmonics, <1 GHz,				-36	dBm
	non-harmonics, >1 GHz				-30	dBm
Broadband noise	30 MHz-1.91 GHz			-160		dB/Hz
	1.91 GHz- 2.3 GHz			-120		dB/Hz
	2.5 GHz- 3.0 GHz			-120		dB/Hz
	3.0 GHz- 12.75 GHz			-130		dB/Hz
Output impedance			50			Ω
Output	VSWR				2:1	

[12] Measured differentially.

[13] Measured in a 5-slot packet.

[14] Measured in a 5-slot packet using curve fitting to reduce noise influence.

[15] See Table 2.

Table 2, transmitter power levels [16]

T_{Amb}=25°C, VCC =2.7V, f_{Ref} = 13MHz, ±10ppm, VSWR ≤ 2:1, VCC_PA =3.2V

Register #16 setting (XXXX XXXX XXXX ABCD) [17]	Register #24 setting (00100ABC)	Pout				I_{Tot} (I_{Vcc}+I_{Vcc_pa})	
		Min	Typ	Max	Unit	Typ	Unit
ABCD = 1111	ABC = 111	14	16.5	20	dBm	175	mA
1100	101		12		dBm	120	mA
1001	101		8		dBm	90	mA
1001	011		4		dBm	75	mA
0111	100		0		dBm	63	mA
1000	001		-4		dBm	62	mA
0111	001		-8		dBm	54	mA
0110	010		-12		dBm	49	mA
0110	001		-16		dBm	48	mA
0110	000		-20		dBm	47	mA
0101	010		-24		dBm	46	mA
0101	000		-28		dBm	45	mA

[16] Power levels have typical 4dB steps. Power control flexibility enables customer to specify smaller or larger power steps.

[17] X= Don't care

Table 3, digital control registers

Register name	# bits	R or W	Address	Value at reset	Recommended Value
ext-PA-level	16	W	010000 = 16	00000000 00000000	See Table 2
VCO/mod. Test trim	8	W	010001 = 17	10001010	10001010
Chan	8	W	010010 = 18	00000010	
RSSI	5	R	010010 = 18	XXXUUUUU	
XO trim	7	W	010011 = 19	00000000	
ID	8	R	010011 = 19	0100VVVV	Set during application trimming
LPO-hi	1	W	010100 = 20	XXXXXXX0	Set during application trimming
LPO-lo	8	W	010101 = 21	00000000	Set during application trimming
Control	8	W	010110 = 22	01000010	01000010
CHP control	8	W	010111 = 23	00000000	00001000
Power Control	8	W	011000 = 24	00000000	See Table 2
Enable	8	W	011001 = 25	00000000	Initial value
Fref	21	W	011010 = 26	XXX10011 11010110 00100000	Initial value Initial value Initial value
MidTiming	8	W	011011 = 27	00000000	Initial value
ModInc	21	W	011100 = 28	XXX11111 11110101 00000010	Initial value Initial value Initial value
DsmIn	21	W	011101 = 29	XXX00000 00000000 00000000	Initial value Initial value Initial value
DsmOut	8	W	011110 = 30	00000000	Initial value
Mux	7	W	011111 = 31	00000000	Initial value

W=Writable, R=Readable, X=n.a., U=Undefined, V=Version number.

Table 4, short description of the PBA 313 02 pin-out.

(In the Type-column ”A” denotes Analog bipolar and ”D” Digital CMOS

Pin No.	Pin name	Type	Active	Description
A1	VCC	Power	-	Common power supply
A2	RX_ON	D in	High	Receiver power on
A3	VCC_DIG	Power	-	Digital power supply
A4	TX_ON	D in	High	Transmit power on
A5	PX_ON	D in	High	Packet on
A6	VCC_PA	Power	-	Power supply for external PA
B1	ANT	50 Ω	-	Antenna input/output
B2	GND	Ground	-	Common ground
B3	RX_DATA	D out	High	Received data output
B4	GND	Ground	-	Common ground
B5	TX_CLK	D out	-	1 MHz clock
B6	SYS_CLK_REQ	D in	High	System clock request
C1	GND	Ground	-	Common ground
C2	GND	Ground	-	Common ground
C3	GND	Ground	-	Common ground
C4	SI_CDI	D in	High	Serial data input
C5	LPO_CLK	D out	-	3.2 kHz clock
C6	GND	Ground	-	Common ground
C7	GND	Ground	-	Common ground
D1	NC	-	-	Not connected
D2	GND	Ground	-	Common ground

Pin No.	Pin name	Type	Active	Description
D3	SYS_CLK	D out	-	System clock (13 MHz)
D4	SI_CMS	D in	High	Serial data interface
D5	SI_CDO	D out	High	Serial data output
D6	GND	Ground	-	Common ground
D7	GND	Ground	-	Common ground
E1	GND	Ground	-	Common ground
E2	XO_P	A in	-	Crystal positive input
E3	XO_N	A in	-	Crystal negative input / external clock input
E4	PHD_OFF	D in	High	Open PLL
E5	TX_DATA	D in	High	Transmit data
E6	SI_CLK	D in	-	Serial interface clock (4MHz)
F1	TX_SW	D in	High	Controls the RX/TX switch
F2	NC	-	-	Not connected
F3	EXT_RESET	D in	Low	External reset
F4	POR	D out	High	Power on reset
F5	SYNT_ON	D in	High	Synthesiser power up
F6	NC	-	-	Not connected
G*	NC	-	-	Not connected & should not be grounded. (Only for mechanical support).

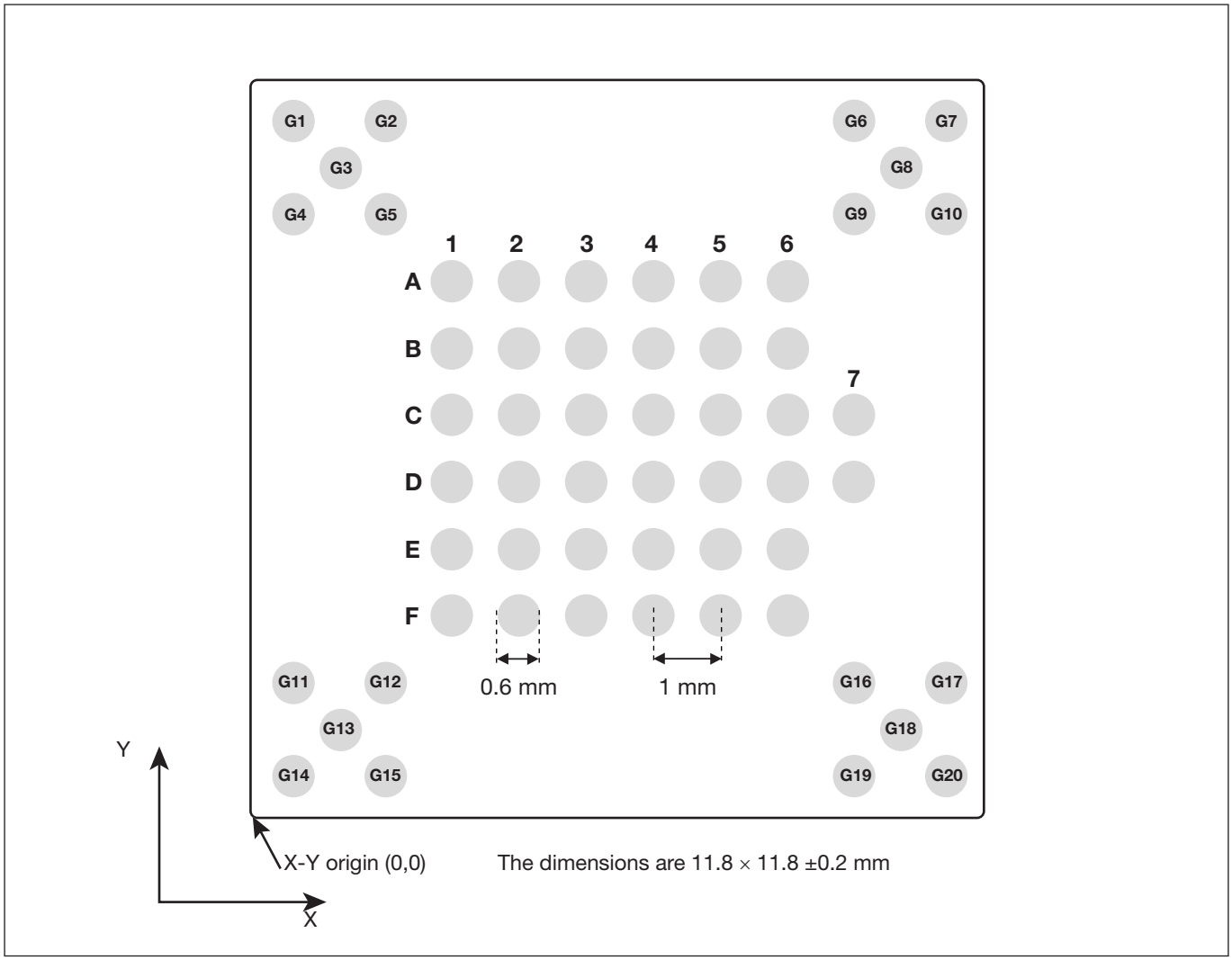


Figure 2. Mechanical dimensions of PBA 313 02. (Seen through the module from the component side)

Physical dimensions

Parameter	Min	Typ	Max	Unit
Length	11.6	11.8	12.0	mm
Width	11.6	11.8	12.0	mm
Thickness			1.6	mm
Coplanarity			0.1	mm

Table 5, Pad co-ordinates for module PBA 313 02

Reference point is down, left corner (0,0) and units are mm.

Pad	X	Y		Pad	X	Y		Pad	X	Y
A1	3,4	8,4		D1	3,4	5,4		G1	0,8	11,0
A2	4,4	8,4		D2	4,4	5,4		G2	2,4	11,0
A3	5,4	8,4		D3	5,4	5,4		G3	1,6	10,2
A4	6,4	8,4		D4	6,4	5,4		G4	0,8	9,4
A5	7,4	8,4		D5	7,4	5,4		G5	2,4	9,4
A6	8,4	8,4		D6	8,4	5,4		G6	9,4	11,0
B1	3,4	7,4		D7	9,4	5,4		G7	11,0	11,0
B2	4,4	7,4		E1	3,4	4,4		G8	10,2	10,2
B3	5,4	7,4		E2	4,4	4,4		G8	10,2	10,2
B4	6,4	7,4		E3	5,4	4,4		G9	9,4	9,4
B5	7,4	7,4		E4	6,4	4,4		G10	11,0	9,4
B6	8,4	7,4		E5	7,4	4,4		G11	0,8	2,4
C1	3,4	6,4		E6	8,4	4,4		G12	2,4	2,4
C2	4,4	6,4		F1	3,4	3,4		G13	1,6	1,6
C3	5,4	6,4		F2	4,4	3,4		G14	0,8	0,8
C4	6,4	6,4		F3	5,4	3,4		G15	2,4	0,8
C5	7,4	6,4		F4	6,4	3,4		G16	9,4	2,4
C6	8,4	6,4		F5	7,4	3,4		G17	11,0	2,4
C7	9,4	6,4		F6	8,4	3,4		G18	10,2	1,6
								G19	9,4	0.8
								G20	11.0	0,8

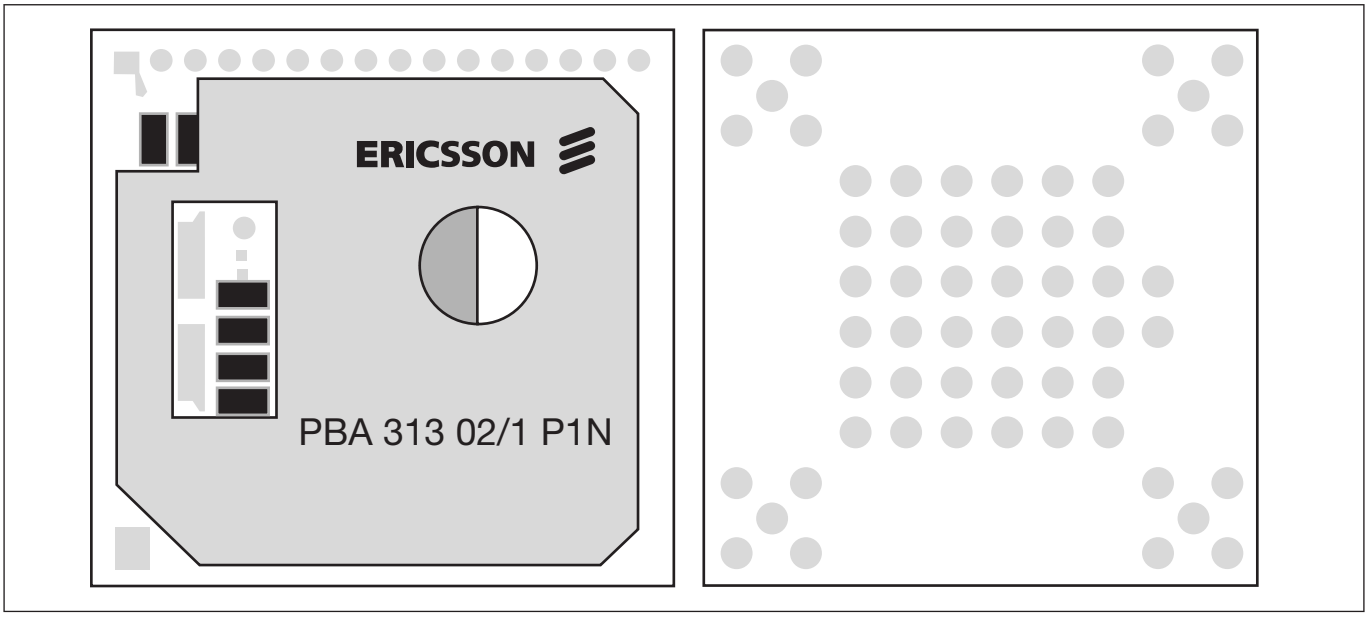


Figure 3. Orientation of PBA 313 02 (Top and bottom layers of the module shown in the same orientation).

Functional description

PBA 313 02 is a long-range transceiver module for Bluetooth applications. The transceiver operates in the globally available 2.4 – 2.5 GHz ISM band. The module is a class 1 Bluetooth device.
The transceiver module is based on a BiCMOS application specific integrated circuit (ASIC). The antenna filter, the RX and TX baluns, and the switch are all at least partially integrated into the ceramic substrate onto which the components of the module are mounted.
The maximum output power is +20 dBm and the sensitivity (0.1% bit error rate) is –86 dBm (typical), measured at the antenna pin.

Block diagram

PBA 313 02 is based on a single chip radio ASIC that utilises a heterodyne receiver architecture with low intermediate frequency. The transmitter utilises direct modulation of the voltage controlled oscillator. A fractional N synthesiser is used to enable different reference frequencies to be used. There are also a number of other circuit blocks including a crystal oscillator, a low power oscillator, power on reset and frequency divider. The chip is controlled by the serial interface.
The block diagram in figure 4 shows the simplified architecture of the radio ASIC and seven major supporting blocks on the module:

Radio ASIC

The receiver on the radio ASIC consists of a low noise amplifier, followed by an image reject down converter. The low IF signal of the mixer is fed to an on chip selectivity filter. This is followed by a limiter, which generates the RSSI and also maximises the signal before it is fed to the demodulator. This is followed by a post detection filter and a slicer, which outputs the data to a baseband.

The transmitter consists of a gaussian low pass filter to shape the data before it directly modulates the voltage controlled oscillator, which is run in open loop during transmit. The VCO is buffered before driving the PA on the module. The module output power is controlled by varying the buffer and PA gain

VCO-tank

Part of the phase locked loop. The modulation is performed directly on the VCO. To ensure high performance the VCO-tank is laser trimmed.

Loop filter

Generates the tuning voltage of the VCO-tank.

RX balun

Transformation from unbalanced (single-ended) to balanced (differential) transmission. The major part of the balun is integrated in the substrate.
TX balun Biasing of the output amplifier in the radio ASIC and transformation from balanced to unbalanced transmission. The major part of the balun is integrated in the substrate.

Antenna switch

Directs the power either from the antenna filter to the receive port or from the external PA output port to the antenna filter.

Antenna filter

Front end bandpass filter fully integrated in the ceramic substrate.

External PA

Two stage GaAs Power Amplifier that operates from a single supply and boosts the output power up to +20dBm, mounted on the module. The output power is controlled by an analogue signal from the ASIC.

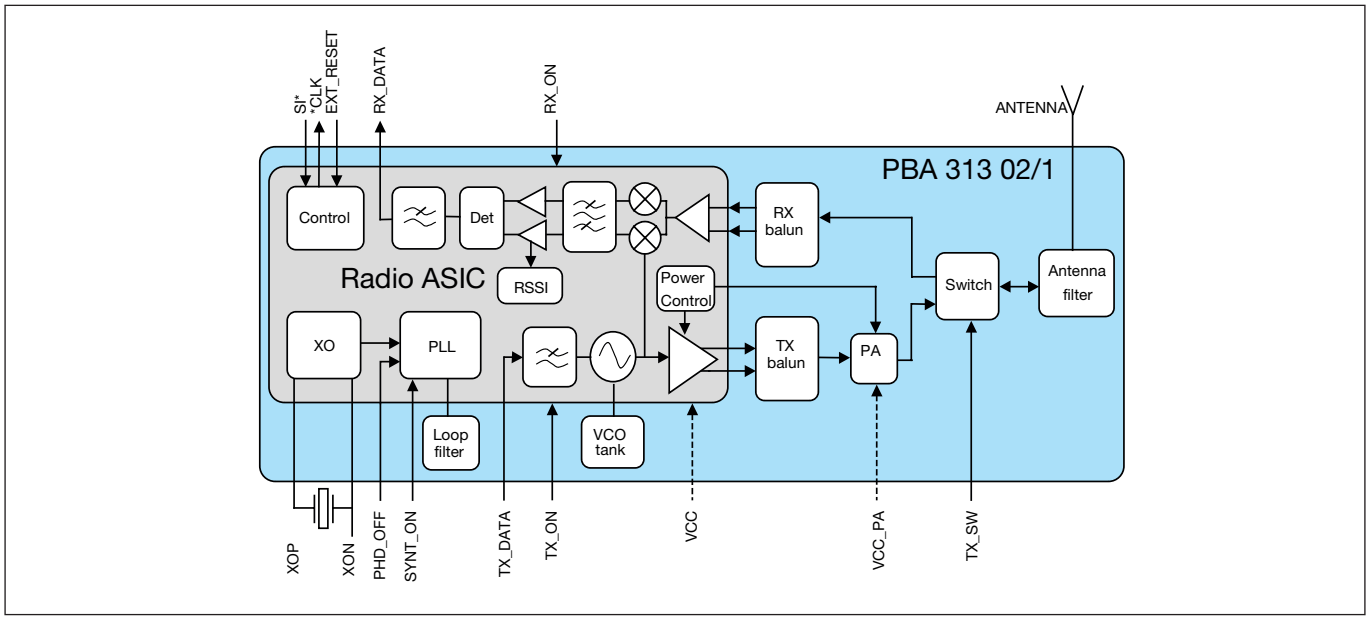


Figure 4. Block diagram.

I/O signal description

Power supply

There are three connections feeding the Bluetooth radio, VCC, VCC_DIG and VCC_PA. VCC supplies the sensitive RF circuitry. It's important that this supply is proper decoupled and free from noise and other disturbances. VCC_DIG feeds the digital circuitry of the module. The power amplifier is fed from the VCC_PA rail. To avoid AM modulation on the TX signal this pin should also be decoupled.

Oscillator or external clock input

XO_N and XO_P connects to the crystal's inputs. The load capacitance to the crystal can be trimmed using the XO-Trim register (Depending on crystal, no external load capacitors are required). If an external clock is used, it should be AC coupled into the XO_N input and the XO_P input shall be left unconnected.

Ground

Ground should be distributed with very low impedance as a ground plane. Connect all GND connections to the ground plane. It is critical to have a ground plane underneath the Bluetooth radio in order to shield the VCO tank from any electrical noise. The ground vias purpose is to connect the local ground plane to the main ground layer. Note: If a local ground plane cannot be directly placed underneath the radio, then no routing should be planned underneath the radio until a layer can be used as a local ground plane. The Bluetooth radio will be self-shielding and no additional shields should be necessary for normal operating conditions.

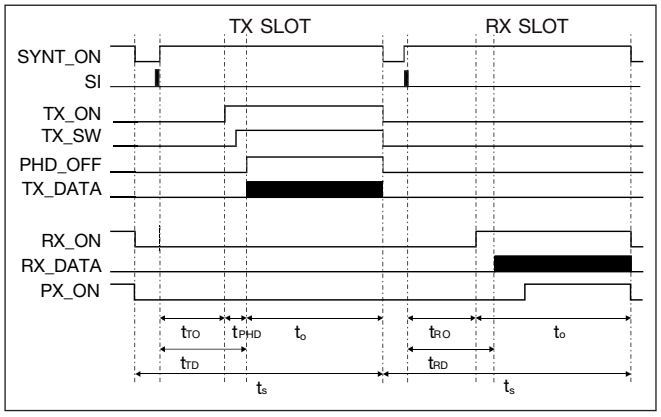


Figure 5. Timing sequence for data transmission.

Antenna

The ANT pin should be connected to a 50Ω antenna interface, thereby supporting the best signal strength performance. Ericsson Microelectronics partners can support application specific antennas.

Input control

There are five digital inputs available for the radio controlling features of the PBA 313 02. The Bluetooth timing requirements for these are described in table 6 and figure 5. In addition, there is a digital input signal for hardware reset of the radio, and a digital input signal for waking up the clock circuitry after a sleep mode period.

PX_ON

Packet switch on control is active 'high'. Activate this signal during reception of a Bluetooth payload.
PX_ON is used to control the Slicer of the receiver. Since the General Inquiry Access Code (GIAC), information in a Bluetooth packet header contains an equal number of one's (+FMOD) and zero's (-FMOD), the average frequency will always be centred on the carrier frequency. This provides the Slicer the reference for the fast tuning. If the fast mode is not used during the header then the first bits could be interpreted incorrectly.
The slow mode gives a more accurate FSK compensation of the thresholds for a one and a zero compared to the fast mode; therefore, the BER is less. The fast mode (time constant < 2µs) is used when PX_ON is deactivated and the slow mode (time constant < 50µs) when it is activated.

SYNT_ON

Synthesiser on control is active 'high'. Activate this signal to power up of the VCO section of the radio. SYNT_ON is used in both transmit and receive mode. This activates the PLL as well as the VCO.

RX_ON

Receive-on control is active 'high'. Activate this signal to enable reception of Bluetooth data on the RX_DATA pin. The transmit-on control (TX_ON) must be deactivated and the synthesiser (SYNT_ON) activated if data is to be received.

Symbol	Parameter	Min	Typical	Max	Unit
tS	One Slot time			625	µs
tS	Two Slot times			1875	µs
tS	Three Slot times			3125	µs
tTO	Transmitter On delay		102		µs
tTD	Delay before transmitting data	203	213	223	µs
tPHD	Phase Detector Off delay after tTO		104		µs
tD	Data sending period, one slot			366	µs
tD	Data sending period, two slots			1598	µs
tD	Data sending period, three slots			2862	µs
tRO	Receiver On delay		175	213	µs
tRD	Delay before receiving data		213		µs

Table 6. Timing requirements for data transmission.

TX_ON

Transmit-on control is active ‘high’. Activate this signal to enable radio signal output on the ANT pin. The actual transfer of data that exists on the TX_DATA input occurs when PHD_OFF goes ‘high’. The receive-on control, RX_ON, must also be ‘low’ and the transmit-switch, TX_SW, be held “high” if data is to be transmitted.

TX_SW

Transmit-switch is active ”high”. This switch controls which one of the TX_PA and the RX balun to be connected to the antenna. During TX mode it should be held ”high”, the rest of the time it should be ”low”. In system without a dedicated control pin this signal can be connected to the TX_ON signal.

PHD_OFF

Phase detector off control is active ‘high’. Activate this signal in transmit mode to open the phase locked loop (PLL) employed in the VCO section and enable modulation of the carrier using the TX_DATA digital input. PHD_OFF is activated after the initialisation of the SYNT_ON signal and the TX_ON signal.

POR_EXT

External power on reset is active ‘high’. An external power-on-reset digital input signal that will reset the radio controller and its registers. A reset will occur on the positive edge of POR_EXT signal. The signal should remain high during operation.

SYS_CLK_REQ

System clock request control is active ‘high’. Once the crystal oscillator bit (XOCTR, control register, bit #2) has been set, use this control to switch off (sleep mode) and wake up (idle and operating modes) the reference clock circuitry and corresponding 13 MHz and 1 MHz clock output ports of the module.

Output control

There are four digital output control signals available for controlling external baseband circuitry.

POR

Power-on-reset digital output is activated after the power has been applied to the Bluetooth radio or on a positive edge of the POR_EXT digital input. POR has a transition from ‘low’ to ‘high’ after four clock cycles have been delivered to the baseband chip, see figure 6.

SYS_CLK

13 MHz system clock digital output available for the baseband circuitry when the POR_EXT and SYS_CLK_REQ are both ‘high’. SYS_CLK will also be available during start-up, independent on the value of SYS_CLK_REQ.

TX_CLK

1 MHz transmit clock digital output available for the baseband circuitry when the POR_EXT and SYS_CLK_REQ (see above) are both ‘high’. TX_CLK changes value on rising edges of SYS_CLK.

LPO_CLK

3.2 kHz low power oscillator clock digital output that is adjustable by setting the internal LPOHI and LPOLO registers (see figure 6).The clock output is available as soon as the power supply is applied and POR_EXT is ‘high’. The LPO is necessary for wake-up timing in the baseband circuitry, if the Ericsson baseband is used.

Data interface

Two digital signals are used for data flow over the air interface.

TX_DATA

Transmit data digital control is active ‘high’[18]. The radio module feeds Bluetooth data (1 Mbit/s) directly[19] to the radio frequency modulator when PHD_OFF is activated. The total delay from the TX_DATA pin to the ANT pin is typically 0.5 µs.

[18] The TX_polarity bit of Enable register should be set to ’1’ (positive polarity) for normal operation.
A logic ’high’ value will then result in a positive frequency deviation output on the ANT pin.

[19] Data on the TX_DATA pin is digitally buffered before it is fed to the radio frequency modulator.

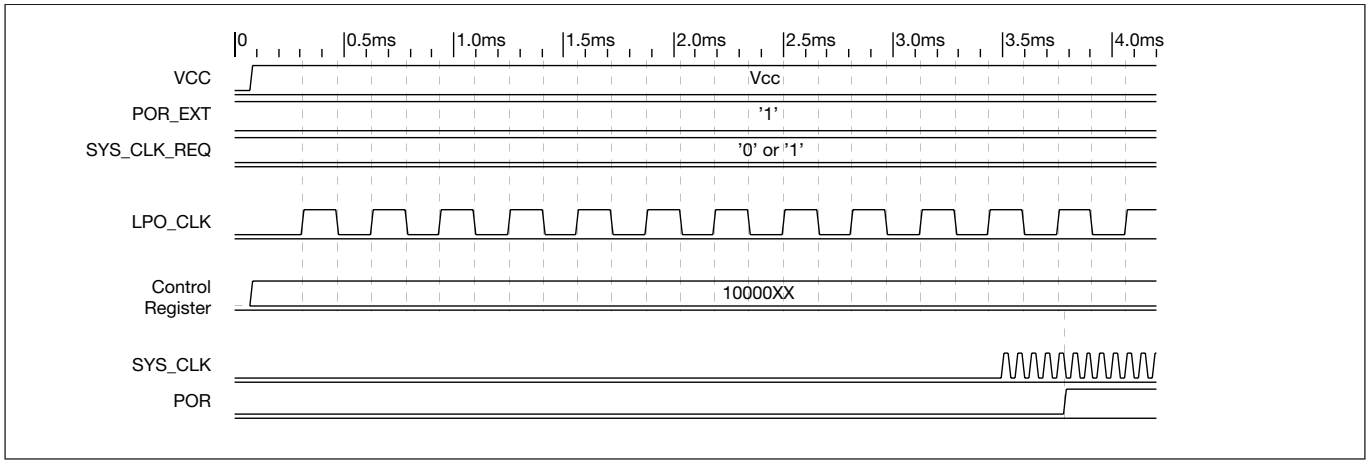


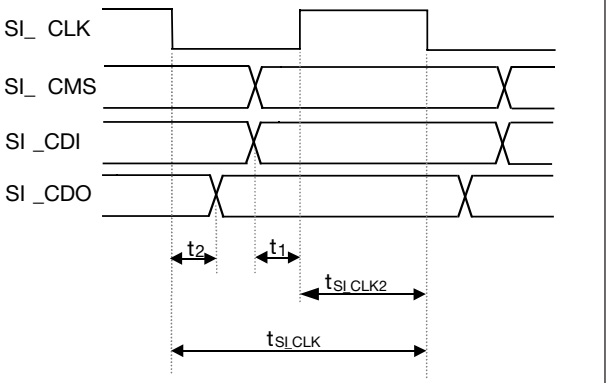
Figure 6. Powering up the module.

RX_DATA

Receive data digital output is active 'high'. The radio module latches out Bluetooth data (1 Mbit/s) on the RX_DATA pin on falling edges of SYS_CLK when RX_ON is activated. The total delay from the ANT pin to the RX_DATA pin is typically 2.5 µs.

Serial interface

The serial control interface is a JTAG Boundary-Scan Architecture (IEEE Std 1149.1). Interconnection between the serial interface and the external controller (baseband circuit) consists of four 1-bit digital signals; control data input (SI_CDI), control mode select (SI_CMS), control clock (SI_CLK) and control data output (SI_CDO). The timing of these signals are defined in figure 7.
(Footnotes)



	Min	Typ	Max	Unit
t_{SI_CLK}	200	250		ns
t_{SI_CLK2}	76	76		ns
t_1	20			ns
t_2			20	ns

Figure 7. Timing diagram of the serial interface.

Assembly guidelines

Solder paste

The PBA 313 02 module is made for surface mounting with land grid array (LGA) gold solder joints. To assemble the module, solder paste (eutectic Tin/Lead) must be printed at the target surface. Preferred solder paste height is 100-127µm (4-5 mil).

Soldering profile

It must be noted that the module should not be allowed to be hanging upside down in the reflow operation. This means that the module has to be assembled on the side of the PCB that is soldered last. The reflow process should be a regular surface mount soldering profile (full convection strongly preferred), the ramp-up should not be more than 3°C/s and with a peak temperature of 210-225°C during 10-20 seconds. Max sloping rate should not exceed 4°C/s.

Pad size

It is recommended that the pads on the PCB should have a diameter of 0.5-0.7mm. The surface finish on the PCB pads should be Nickel/Gold or a flat Tin/Lead surface or OSP (Organic Surface Protection).

Placement

The recommended pickup co-ordinates for the PBA 313 02 shield is based on a nozzle with inner diameter 2 mm and outer diameter 3.17 mm. The centre of the shield is the origin of co-ordinates, (0,0) for (x,y), giving the pickup co-ordinates (5.9mm, 5.9mm) for (x,y).

Storage

Keep the component in its dry pack when not yet using the reel. After removal from the dry pack ensure that the modules are soldered onto the PCB within 48 hours.

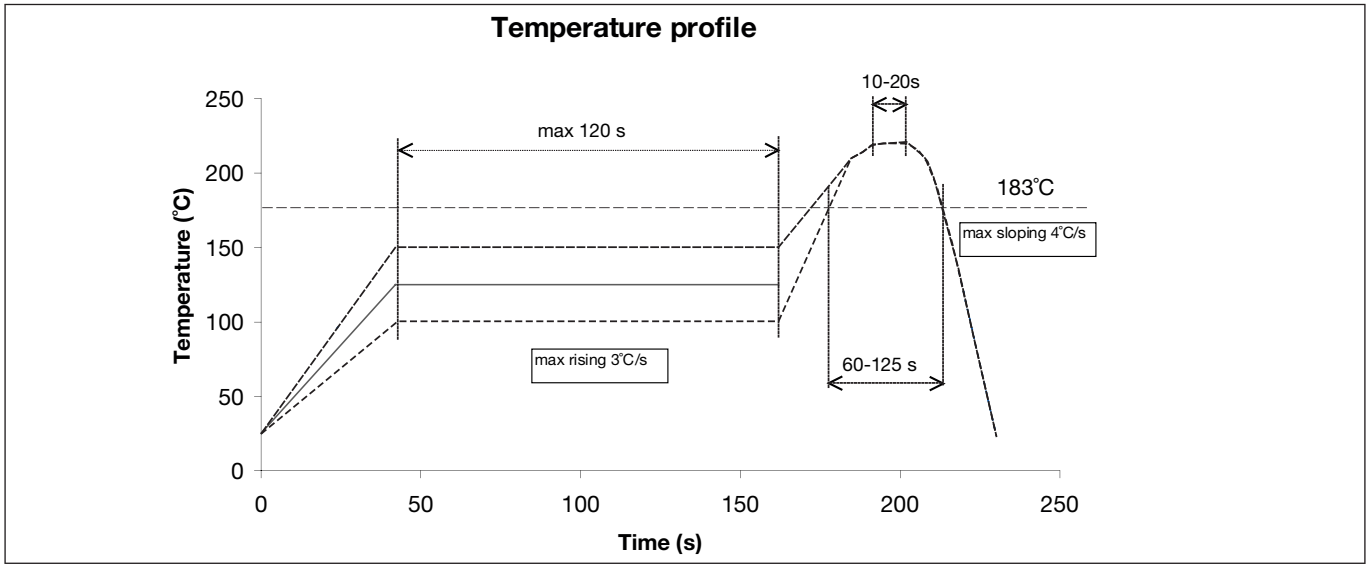


Figure 8. Temperature profile.

Module marking

Each module is marked on the shield with the following information:

- Ericsson logotype
- Product No with index
- Revision state
- Manufacturing unit code
- Production year and week
- Bluetooth trademark
- FCC product code
- CE marking

Reel marking

The reel, reel box and dry pack has a label with the following information:

- Ericsson product number with revision
- Customer product number with revision
- Quantity
- Reel-ID. (Batch No)
- Factory code
- Manufacturing date
- Country of origin
- Ericsson logotype

1-6 above is also printed in BAR-code format

Contacting Ericsson Microelectronics

For further information regarding Bluetooth technology, components and development tools,
please contact Ericsson Microelectronics:

Ericsson Microelectronics
SE-164 81 Kista, Sweden
Telephone: +46 8 757 50 00
Internet: www.ericsson.com/microelectronics

For local sales contacts, please refer to our website
or call: Int + 46 8 757 47 00, Fax: +46 8 757 47 76

The latest and most complete information can be found on our website!

Preliminary Data Sheet

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