

DATA SHEET

74F776

Pi-bus transceiver

Product specification

1990 Dec 19

IC15 Data Handbook

Pi-bus transceiver

74F776

FEATURES

- Octal latched transceiver
- Drives heavily loaded backplanes with equivalent load impedances down to 10 ohms
- High drive (100mA) open collector drivers on B port
- Reduced voltage swing (1 volt) produces less noise and reduces power consumption
- High speed operation enhances performance of backplane buses and facilitates incident wave switching
- Compatible with Pi-bus and IEEE 896 Futurebus standards
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Controlled output ramp and multiple GND pins minimize ground bounce
- Glitch-free power up/power down operation
- Multiple package options
- Industrial temperature range available (-40°C to $+85^{\circ}\text{C}$)

DESCRIPTION

The 74F776 is an octal bidirectional latched transceiver and is intended to provide the electrical interface to a high performance wired-OR bus. The B port inverting drivers are low-capacitance open collector with controlled ramp and are designed to sink 100mA from 2 volts. The B port inverting receivers have a 100 mV threshold region and a 4ns glitch filter.

The 74F776 B port interfaces to 'Backplane Transceiver Logic' (BTL). BTL features a reduced (1V to 2V) voltage swing for lower power

consumption and a series diode on the drivers to reduce capacitive loading. Incident wave switching is employed, therefore BTL propagation delays are short. Although the voltage swing is less for BTL, so is its receiver threshold, therefore noise margins are excellent.

BTL offers low power consumption, low ground bounce, EMI and crosstalk, low capacitive loading, superior noise margin and low propagation delays. This results in a high bandwidth, reliable backplane.

The 74F776 A port has TTL 3-state drivers and TTL receivers with a latch function. A separate high-level control voltage input (V_X) is provided to limit the A side output level to a given voltage level (such as 3.3V). For 5.0V systems, V_X is simply tied to V_{CC} .

The 74F776 has a designed feature to control the B output transitions during power sequencing. There are two possible sequencing, They are as follows:

1. When $\overline{\text{LE}} = \text{low}$ and $\overline{\text{OEBn}} = \text{low}$ then the B outputs are disabled until the $\overline{\text{LE}}$ circuitry takes control. Then the B outputs will follow the A inputs, making a maximum of one transition during power-up (or down).
2. If $\overline{\text{LE}} = \text{high}$ or $\overline{\text{OEBn}} = \text{high}$ then the B outputs will be disabled during power-up (or down).

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT(TOTAL)
74F776	6.5ns	80mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	INDUSTRIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	
28-pin plastic DIP (600 mil)	N74F776N	I74F776N	SOT117-2
28-pin PLCC	N74F776A	I74F776A	SOT261-2

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A7	PNP latched inputs	3.5/0.117	70 μA /70 μA
B0 – B7	Data inputs with threshold circuitry	5.0/0.167	100 μA /100 μA
OEA	A output enable input (active high)	1.0/0.033	20 μA /20 μA
$\overline{\text{OEB0}}$, $\overline{\text{OEB1}}$	B output enable inputs (active low)	1.0/0.033	20 μA /20 μA
$\overline{\text{LE}}$	Latch enable input (active low)	1.0/0.033	20 μA /20 μA
A0 – A7	3-state outputs	150/40	3mA/24mA
B0 – B7	Open collector outputs	OC/166.7	OC/100mA

Notes to input and output loading and fan out table

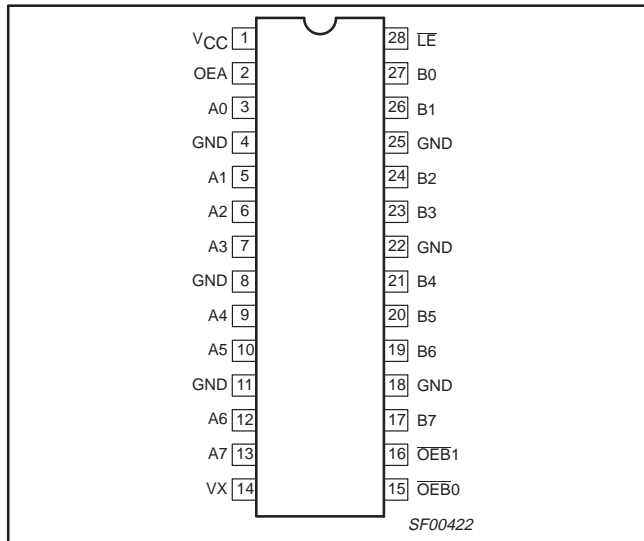
One (1.0) FAST unit load is defined as: 20 μA in the high state and 0.6mA in the low state.

OC = Open collector.

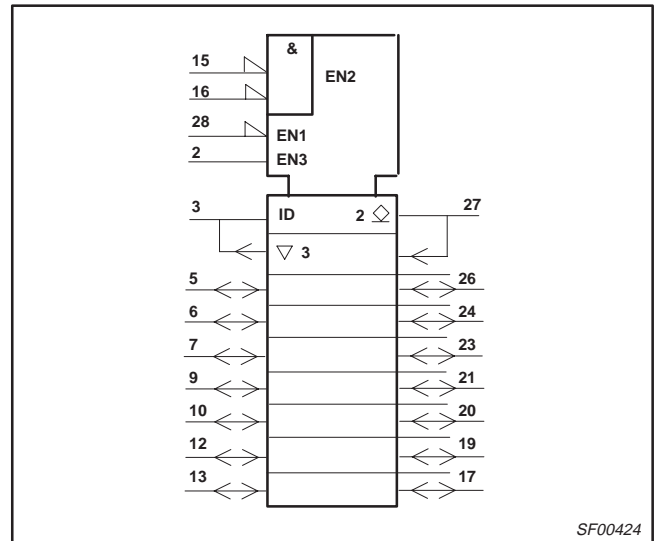
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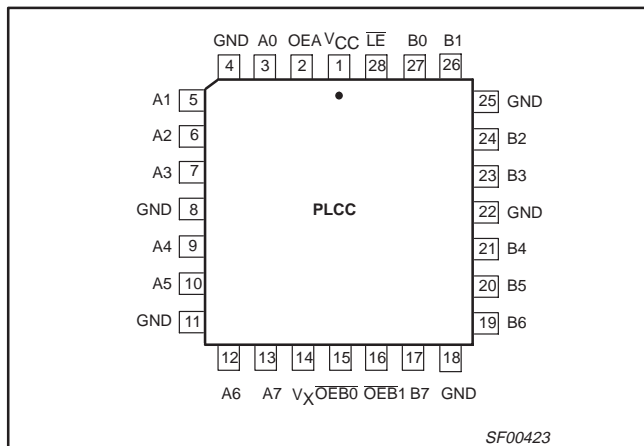
PIN CONFIGURATION



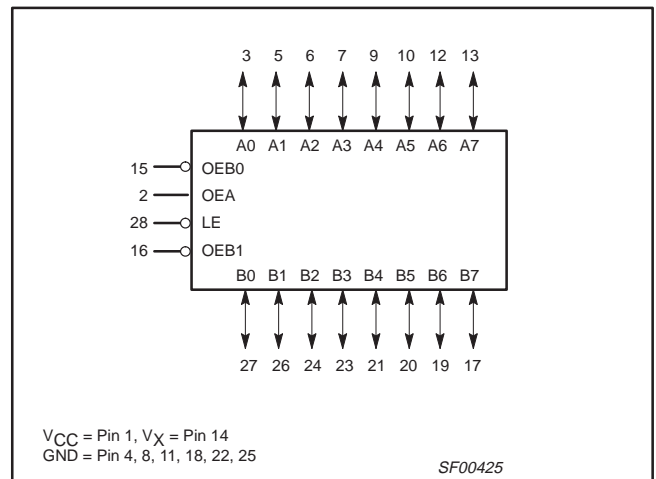
IEC/IEEE SYMBOL



PIN CONFIGURATION PLCC



LOGIC SYMBOL



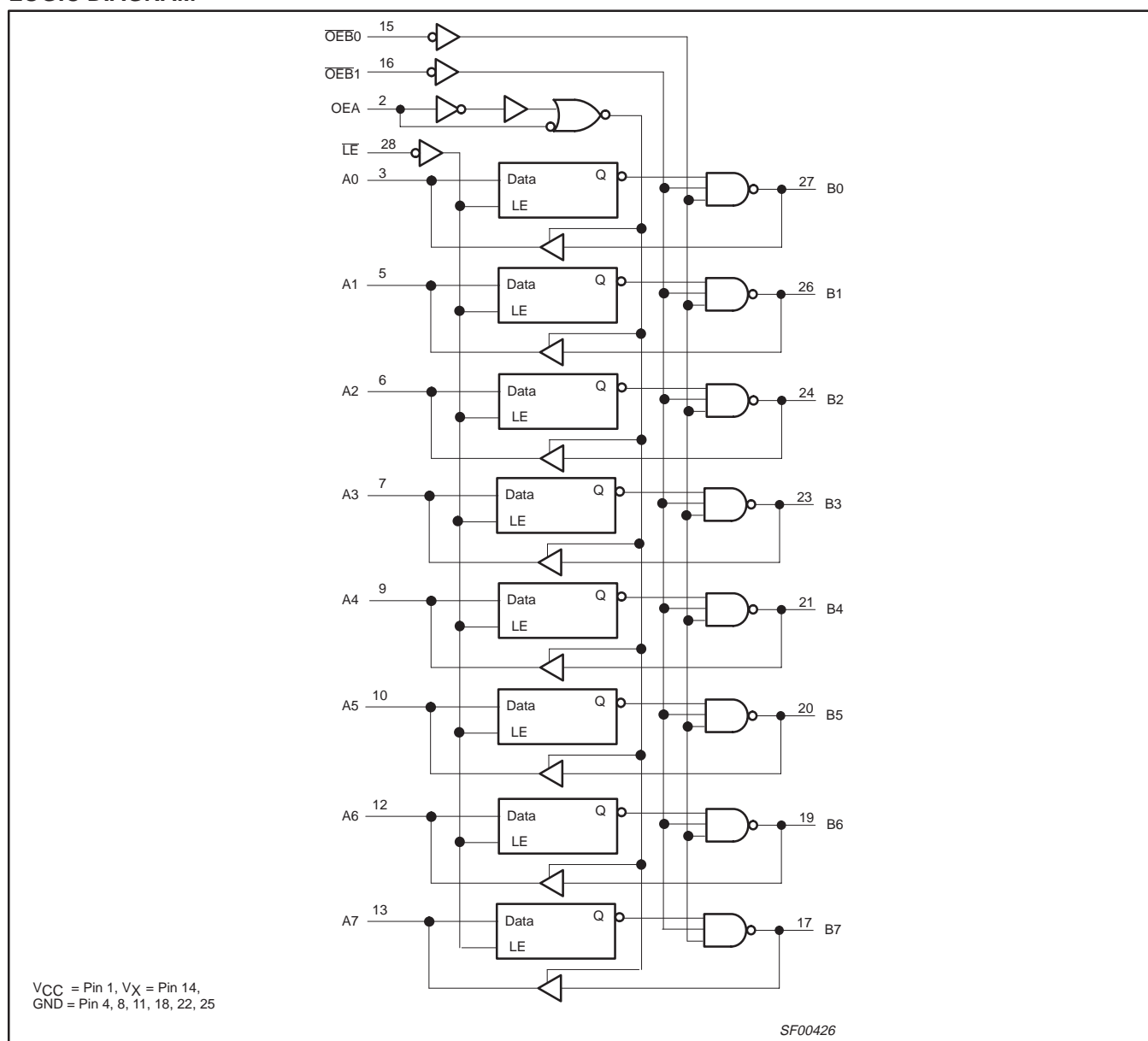
PIN DESCRIPTION

SYMBOL	PINS	TYPE	NAME AND FUNCTION
A0 – A7	3, 5, 6, 7, 9, 10, 12, 13	I/O	PNP latched input/3–state output (with V _X control option)
B0 – B7	27, 26, 24, 23, 21, 20, 19, 17	I/O	Data input with special threshold circuitry to reject noise/ open collector output, high current drive
$\overline{\text{OEB0}}$	15	Input	Enables the B outputs when both pins are low
$\overline{\text{OEB1}}$	16	Input	
OEA	2	Input	Enables the A outputs when high
$\overline{\text{LE}}$	28	Input	Latched when high (a special feature is built in for proper enabling times)
V _X	14	Input	Clamping voltage keeping V _{OH} from rising above V _X (V _X = V _{CC} for normal use)

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LOGIC DIAGRAM



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FUNCTION TABLE

INPUTS						LATCH STATE	OUTPUTS		OPERATING MODE
An	Bn*	LE	OEA	OEB0	OEB1		An	Bn	
H	X	L	L	L	L	H	Z	Z	A 3-state, data from A to B
L	X	L	L	L	L	L	Z	L	
X	X	H	L	L	L	Qn	Z	Qn	A 3-state, latched data to B
-	-	L	H	L	L	(1)	(1)	(1)	Feedback: A to B, B to A
-	H	H	H	L	L	H (2)	H	Z(2)	Preconditioned latch enabling data transfer from B to A
-	L	H	H	L	L	H (2)	L	Z(2)	
-	-	H	H	L	L	Qn	Qn	Qn	Latch state to A and B
H	X	L	L	H	X	H	Z	Z	B and A 3-state
L	X	L	L	H	X	L	Z	Z	
X	X	H	L	H	X	Qn	Z	Z	
-	H	L	H	H	X	H	H	Z	B 3-state, data from B to A
-	L	L	H	H	X	L	L	Z	
-	H	H	H	H	X	Qn	H	Z	
-	L	H	H	H	X	Qn	L	Z	
H	X	L	L	X	H	H	Z	Z	B and A 3-state
L	X	L	L	X	H	L	Z	Z	
X	X	H	L	X	H	Qn	Z	Z	
-	H	L	H	X	H	H	H	Z	B 3-state, data from B to A
-	L	L	H	X	H	L	L	Z	
-	H	H	H	X	H	Qn	H	Z	
-	L	H	H	X	H	Qn	L	Z	

Notes to function table

- H = High voltage level
- L = Low voltage level
- X = Don't care

- = Input not externally driven
- Z = High impedance "off" state

Qn = High or Low voltage level one setup time prior to the low-to-high LE transition.

(1) = Condition will cause a feedback loop path: A to B and B to A.

(2) = The latch must be preconditioned such that B inputs may assume a high or low level while OEB0 and OEB1 are low and LE is high.

B* = Precaution should be taken to insure the B inputs do not float. If they do they are equal to low state.

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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V _{CC}	Supply voltage		-0.5 to +7.0	V
V _X	Threshold control		-0.5 to +7.0	V
V _{IN}	Input voltage	OEB _n , OEA, LE	-0.5 to +7.0	V
		A0 – A7, B0 – B7	-0.5 to +5.5	V
I _{IN}	Input current		-40 to +5	mA
V _{OUT}	Voltage applied to output in high output state		-0.5 to V _{CC}	V
I _{OUT}	Current applied to output in low output state	A0 – A7	48	mA
		B0 – B7	200	mA
T _{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	-40 to +85	°C
T _{stg}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5.0	5.5	V
V _{IH}	High-level input voltage	Except B0 – B7	2.0			V
		B0 – B7	1.6			V
V _{IL}	Low-level input voltage	Except B0 – B7			0.8	V
		B0 – B7			1.45	V
I _{Ik}	Input clamp current	Except A0 – A7			-18	mA
		A0 – A7			-40	mA
I _{OH}	High-level output current	A0 – A7			-3	mA
I _{OL}	Low-level output current	A0 – A7			24	mA
		B0 – B7			100	mA
T _{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	-40		+85	°C

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DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹	LIMITS			UNIT	
				MIN	TYP ²	MAX		
I_{OH}	High-level output current	B0 – B7	$V_{CC} = \text{MAX}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, V_{OH} = 2.1\text{V}$			100	μA	
I_{OFF}	Power-off output current	B0 – B7	$V_{CC} = 0.0\text{V}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, V_{OH} = 2.1\text{V}$			100	μA	
V_{OH}	High-level output voltage	A0 – A7 ⁴	$V_{CC} = \text{MIN},$ $V_{IL} = \text{MAX}, V_{IH} = \text{MIN}$	$I_{OH} = -3\text{mA}, V_X = V_{CC}$	2.5		V_{CC}	V
				$I_{OH} = -4\text{mA},$ $V_X = 3.13\text{V and } 3.47\text{V}$	2.5			V
V_{OL}	Low-level output voltage	A0 – A7 ⁴	$V_{CC} = \text{MIN},$ $V_{IL} = \text{MAX}$	$I_{OL} = 20\text{mA}, V_X = V_{CC}$			0.50	V
		B0 – B7	$V_{IH} = \text{MIN}$	$I_{OL} = 100\text{mA}$			1.15	V
					$I_{OL} = 4\text{mA}$	0.40		
V_{IK}	Input clamp voltage	A0 – A7	$V_{CC} = \text{MIN}, I_I = I_{IK}$				-0.5	V
		Except A0 – A7	$V_{CC} = \text{MIN}, I_I = I_{IK}$				-1.2	V
I_I	Input current at maximum input voltage	$\overline{OE}B_n, OEA, \overline{LE}$	$V_{CC} = 0.0\text{V}, V_I = 7.0\text{V}$				100	μA
		A0 – A7, B0 – B7	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$				1	mA
I_{IH}	High-level input current	$\overline{OE}B_n, OEA, \overline{LE}$	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}, B_n - A_n = 0\text{V}$				20	μA
		B0 – B7	$V_{CC} = \text{MAX}, V_I = 2.1\text{V}$				100	μA
I_{IL}	Low-level input current	$\overline{OE}B_n, OEA, \overline{LE}$	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$				-20	μA
		B0 – B7	$V_{CC} = \text{MAX}, V_I = 0.3\text{V}$				-100	μA
$I_{OZH} + I_{IH}$	Off state output current, high level voltage applied	A0 – A7	$V_{CC} = \text{MAX}, V_O = 2.7\text{V}$				70	μA
$I_{OZL} + I_{IL}$	Off state output current, low level voltage applied	A0 – A7	$V_{CC} = \text{MAX}, V_O = 0.5\text{V}$				-70	μA
I_X	High-level control current		$V_{CC} = \text{MAX}, V_X = V_{CC}, \overline{LE} = OEA = \overline{OE}B_n = 2.7\text{V}, A0 - A7 = 2.7\text{V}, B0 - B7 = 2.0\text{V},$	-100			100	μA
			$V_{CC} = \text{MAX}, V_X = 3.13 \& 3.47\text{V}, \overline{LE} = OEA = 2.7\text{V}, \overline{OE}B_n = A0 - A7 = 2.7\text{V}, B0 - B7 = 2.0\text{V},$	-10			10	μA
I_{OS}	Short circuit output current ³	A0 – A7 only	$V_{CC} = \text{MAX}, B_n = 1.8\text{V}, OEA = 2.0\text{V}, \overline{OE}B_n = 2.7\text{V}$	-60			-150	mA
I_{CC}	Supply current (total)	I_{CCH}	$V_{CC} = \text{MAX}$		65	100	mA	
		I_{CCL}	$V_{CC} = \text{MAX}, V_{IL} = 0.5\text{V}$		100	145	mA	
		I_{CCZ}			75	100	mA	

Notes to DC electrical characteristics

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type. Unless otherwise specified, $V_X = V_{CC}$ for all test conditions.
- All typical values are at $V_{CC} = 5\text{V}, T_{\text{amb}} = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- Due to test equipment limitations, actual test conditions are for $V_{IH} = 1.8\text{V}$ and $V_{IL} = 1.3\text{V}$.

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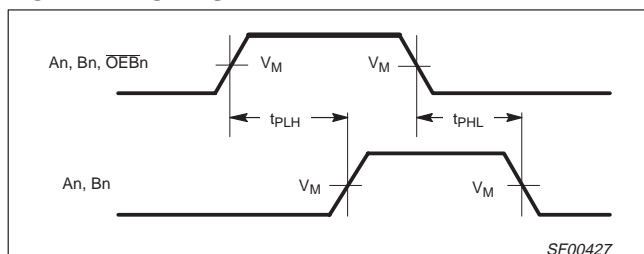
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS						UNIT	
			T _{amb} = +25°C			T _{amb} = 0°C to +70°C		T _{amb} = -40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
t _{PLH} t _{PHL}	Propagation delay Bn to An	Waveform 1	V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		ns
t _{PZH} t _{PZL}	Output enable time to high or low, OEA to An	Waveform 3, 4	5.5	8.0	12.0	5.5	12.0	5.5	12.0	ns
t _{PHZ} t _{PLZ}	Output disable time from high or low, OEA to An	Waveform 3, 4	4.5	6.0	9.0	4.5	9.0	4.5	9.0	ns
t _{PHZ} t _{PLZ}	Output disable time from high or low, OEA to An	Waveform 3, 4	8.0	10.5	13.5	7.5	15.0	7.5	15.5	ns
t _{PHZ} t _{PLZ}	Output disable time from high or low, OEA to An	Waveform 3, 4	2.0	3.5	6.0	1.5	6.5	1.5	6.5	ns
t _{PHZ} t _{PLZ}	Output disable time from high or low, OEA to An	Waveform 3, 4	2.0	4.5	7.0	2.0	7.5	2.0	7.5	ns
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS						UNIT	
			T _{amb} = +25°C			T _{amb} = 0°C to +70°C		T _{amb} = -40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
t _{PLH} t _{PHL}	Propagation delay An to Bn	Waveform 1	V _{CC} = +5.0V C _D = 30pF, R _U = 9Ω			V _{CC} = +5.0V ± 10% C _D = 30pF, R _U = 9Ω		V _{CC} = +5.0V ± 10% C _D = 30pF, R _U = 9Ω		ns
t _{PLH} t _{PHL}	Propagation delay LE to Bn	Waveform 1	3.0	5.0	7.0	2.5	8.0	2.0	9.0	ns
t _{PLH} t _{PHL}	Propagation delay LE to Bn	Waveform 1	3.0	4.5	7.5	2.5	8.5	2.5	8.5	ns
t _{PLH} t _{PHL}	Enable/disable time OEBn to An	Waveform 1	3.5	5.0	8.0	3.0	9.0	2.5	9.5	ns
t _{PLH} t _{PHL}	Enable/disable time OEBn to An	Waveform 1	3.5	5.0	8.0	2.5	9.0	2.5	9.5	ns
t _{PLH} t _{PHL}	Enable/disable time OEBn to An	Waveform 1	3.0	4.5	7.0	2.5	8.0	2.5	8.5	ns
t _{PLH} t _{PHL}	Enable/disable time OEBn to An	Waveform 1	3.5	5.5	9.0	3.5	10.0	3.5	10.5	ns
t _{TLH} t _{THL}	Transition time, B port 1.3V to 1.7V, 1.7V to 1.3V	Test Circuit and Waveforms	0.5	2.0	4.5	0.5	5.0	0.5	5.0	ns
t _{TLH} t _{THL}	Transition time, B port 1.3V to 1.7V, 1.7V to 1.3V	Test Circuit and Waveforms	0.5	2.0	4.5	0.5	5.0	0.5	5.0	ns

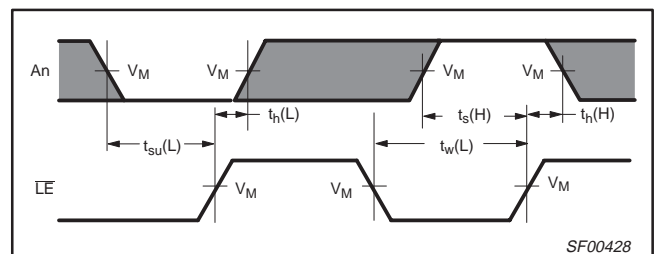
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT	
			T _{amb} = +25°C			T _{amb} = 0°C to +70°C		T _{amb} = -40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
t _{SU} (H) t _{SU} (L)	Setup time, high or low An to LE	Waveform 2	V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		ns
t _{SU} (H) t _{SU} (L)	Setup time, high or low An to LE	Waveform 2	3.5			4.5		4.5		ns
t _H (H) t _H (L)	Hold time, high or low An to LE	Waveform 2	4.5			5.0		5.0		ns
t _H (H) t _H (L)	Hold time, high or low An to LE	Waveform 2	0.0			0.0		0.0		ns
t _H (H) t _H (L)	Hold time, high or low An to LE	Waveform 2	0.0			0.0		0.0		ns
t _w (L)	LE pulse width, low	Waveform 2	4.0			5.0		5.0		ns

AC WAVEFORMS



Waveform 1. Propagation delay for data to output

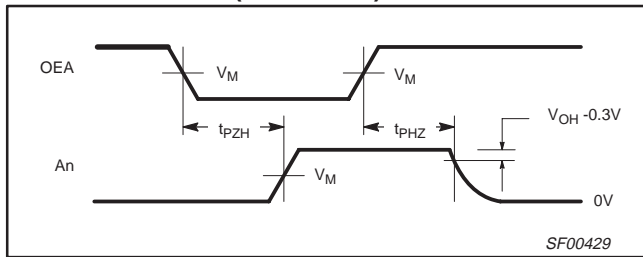


Waveform 2. Data setup and hold times and LE pulse width

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AC WAVEFORMS (Continued)

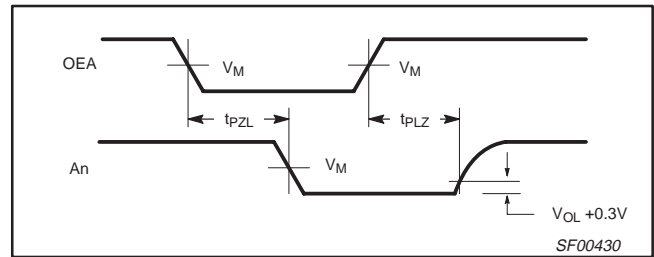


Waveform 3. 3-state output enable time to high level and output disable time from high level

Notes to AC waveforms

For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 4. 3-state output enable time to low level and output disable time from low level

TEST CIRCUIT AND WAVEFORMS

SWITCH POSITION	
TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

Test circuit for 3-State outputs on A port

Test circuit for outputs on B port

Input pulse definition

family	INPUT PULSE REQUIREMENTS						
	amplitude	Low V	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
A port	3.0V	0.0V	1.5V	1MHz	500ns	2.5ns	2.5ns
B port	2.0V	1.0V	1.0V	1MHz	500ns	4.0ns	4.0ns

DEFINITIONS:
 R_L = Load resistor; see AC electrical characteristics for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
 R_U = Pull up resistor; see AC electrical characteristics for value.
 C_D = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

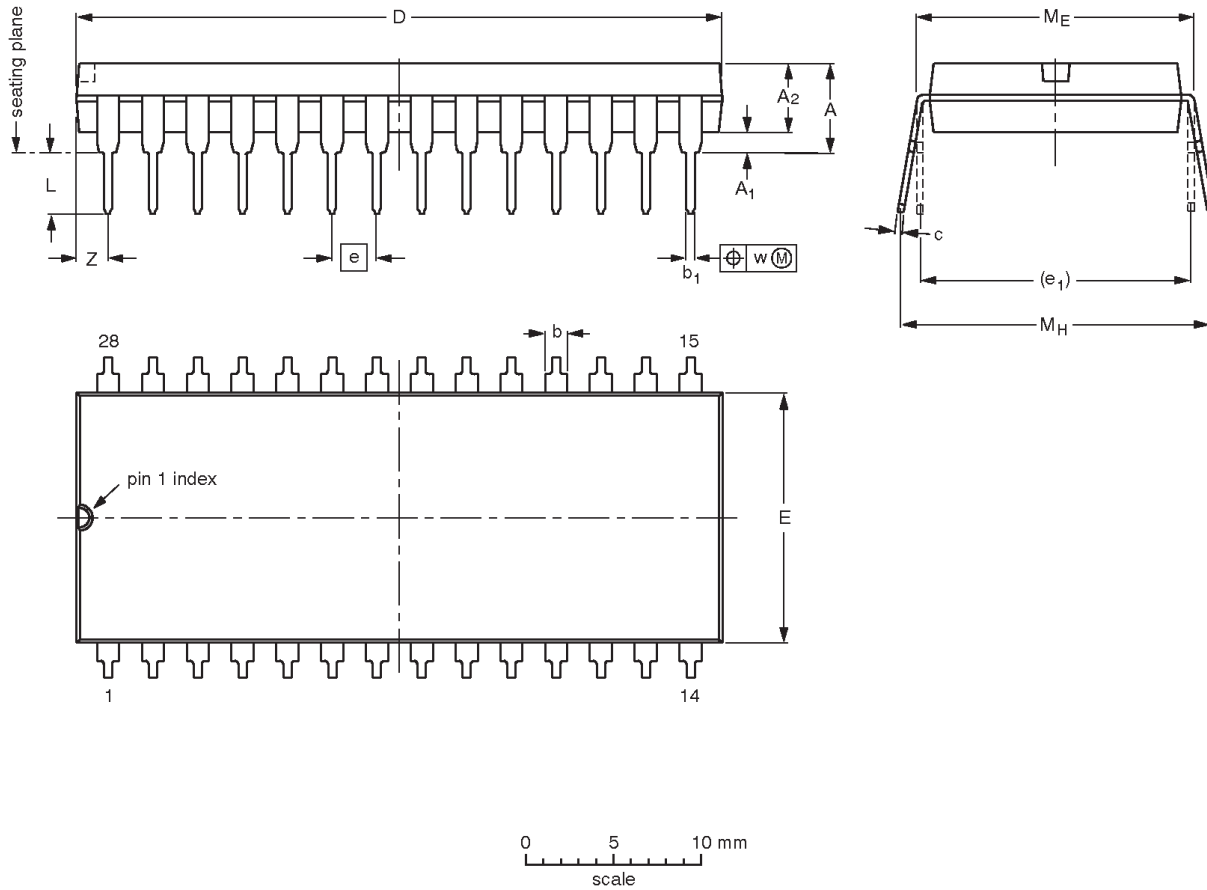
SF00431

Pi-bus transceiver

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DIP28: plastic dual in-line package; 28 leads (600 mil); long body

SOT117-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	5.08	0.51	3.94	1.63 1.14	0.56 0.43	0.38 0.25	37.08 35.94	14.22 13.84	2.54	15.24	3.51 3.05	15.75 15.24	17.65 15.24	0.25	2.10
inches	0.200	0.020	0.155	0.064 0.045	0.022 0.017	0.015 0.010	1.460 1.415	0.560 0.545	0.100	0.600	0.138 0.120	0.62 0.60	0.695 0.600	0.01	0.083

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

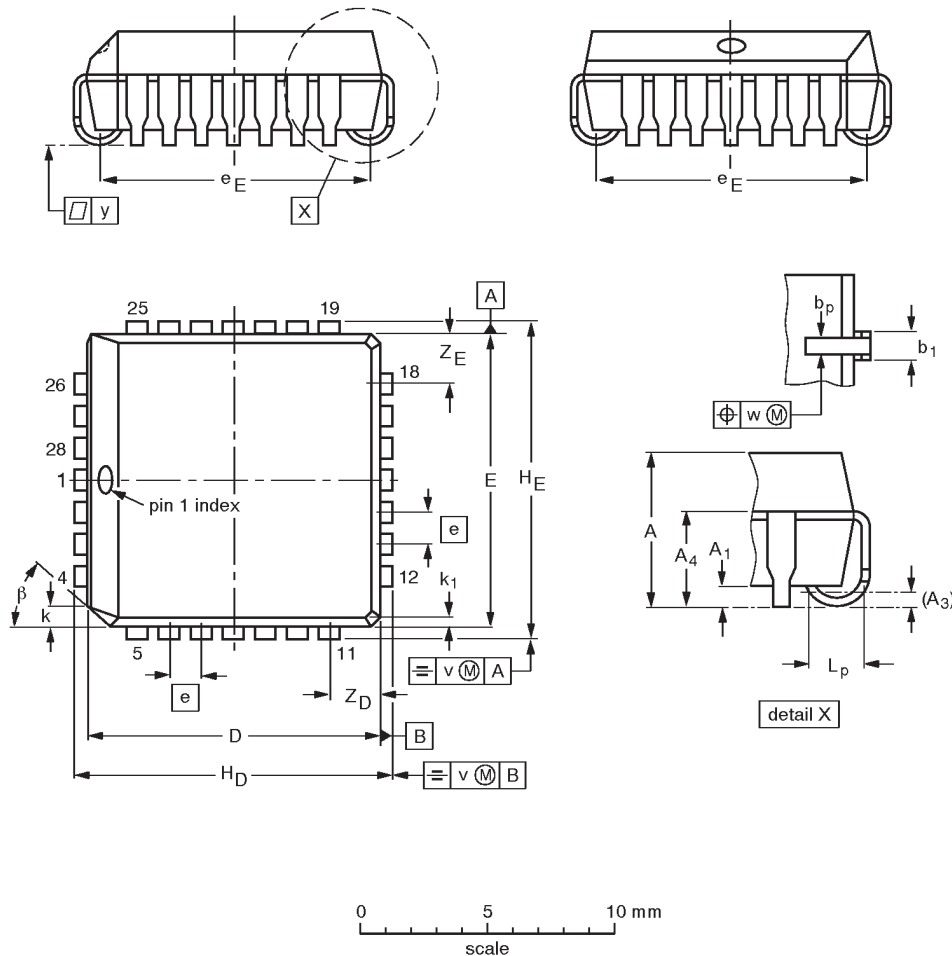
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-2		MS-011AB				95-03-11

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PLCC28: plastic leaded chip carrier; 28 leads

SOT261-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A ₁ min.	A ₃	A ₄ max.	b _p	b ₁	D ⁽¹⁾	E ⁽¹⁾	e	e _D	e _E	H _D	H _E	k	k ₁ max.	L _p	v	w	y	Z _D ⁽¹⁾ max.	Z _E ⁽¹⁾ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.430 0.390	0.430 0.390	0.495 0.485	0.495 0.485	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT261-2					92-11-17 95-02-25

Pi-bus transceiver

74F776

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088-3409
Telephone 800-234-7381

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