Oki Semiconductor

MSM7712

Wireless LAN Baseband Controller

DESCRIPTION

The MSM7712 is the first release in a series of wireless LAN baseband controllers, designated .XI (a suffix of the IEEE P802.11 protocol). The MSM7712 integrates the baseband physical layer and the lower MAC layers into a single IC that supports specific draft standards of the P802.11 specification. The architecture targets optimum integration with maximum user flexibility, providing a migration path to low-cost module handsets and access points. In accordance with all three P802.11 media, the MSM7712 directly supports frequency hopping (FH), spread spectrum, direct-sequence spread spectrum, and infrared protocols., A board-level system contains the MSM7712, a radio, a 16-bit processor, and buffer memory ICs.

The MSM7712 provides a seamless interface to the radio, hoist, processor, and memory subsystems. The device directly interfaces with the PCMCIA R2.1 and ISA bus, with support for 16-bit data transfers. The device can control antenna select, synthesizer programming, and power-save modes. The MSM7712 provides FH PLPC framing, with the FH modem on-board. A bypass mode allows support for other standards. MSM7712 firmware is available from Oki Semiconductor.

Portable handheld systems inherently require minimal current dissipation during operation and standby modes. The MSM7712 offers low power consumption via its implementation of a 3-V core. Either 3-V or 5-V I/O are available for optimal RF and host-interface design.

The MSM7712 wireless LAN baseband controller is manufactured in Oki's advanced Si-gate 0.5µm CMOS process for the best possible low-power performance.

FEATURES

- Support for specific IEEE P802.11 wireless LAN draft standards
- Suitable for low-cost stations and access points
- PCMCIA compliant (version 2.1) interface supporting 16-bit data transfers
- On-chip radio modem for high-throughput data transfers
- Interface to radio providing antenna select, power control, synthesizer programming
- Processor interface support for 80C86, 80C186, V33, and V53A
- On-chip multi-port memory controller on chip for local shared memory and simplified design construction
- E^2PROM interface to download host interface configuration data and provide non-volatile card parameter storage
- Low-power mode to minimize power dissipation in batter applications.
- 5-V external and 3.3-V core operation
- 144-pin LQFP package, suitable for PCMCIA Type II Cards (LQFP144-P-2020-0.50-K)

BLOCK DIAGRAM

Figure 1 shows a typical WLAN card. The MSM7712 provides a direct connection to a host interface, processor, radio, shared memory, and configuration E^2PROM. Optional additions are a RAM for processor code.

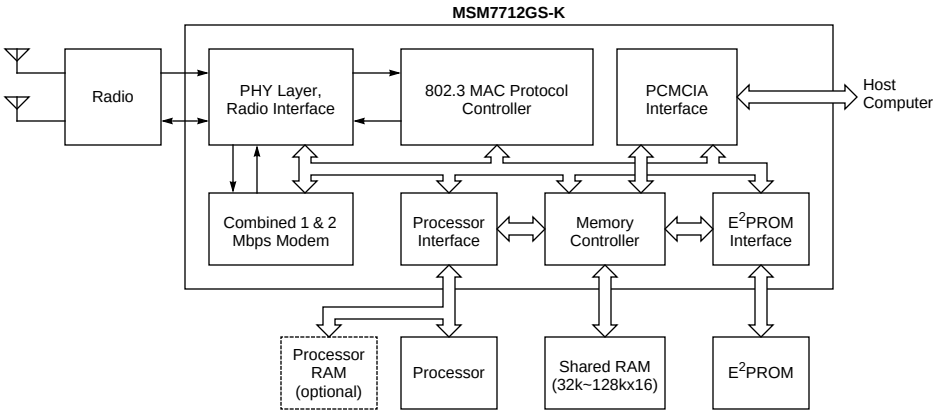
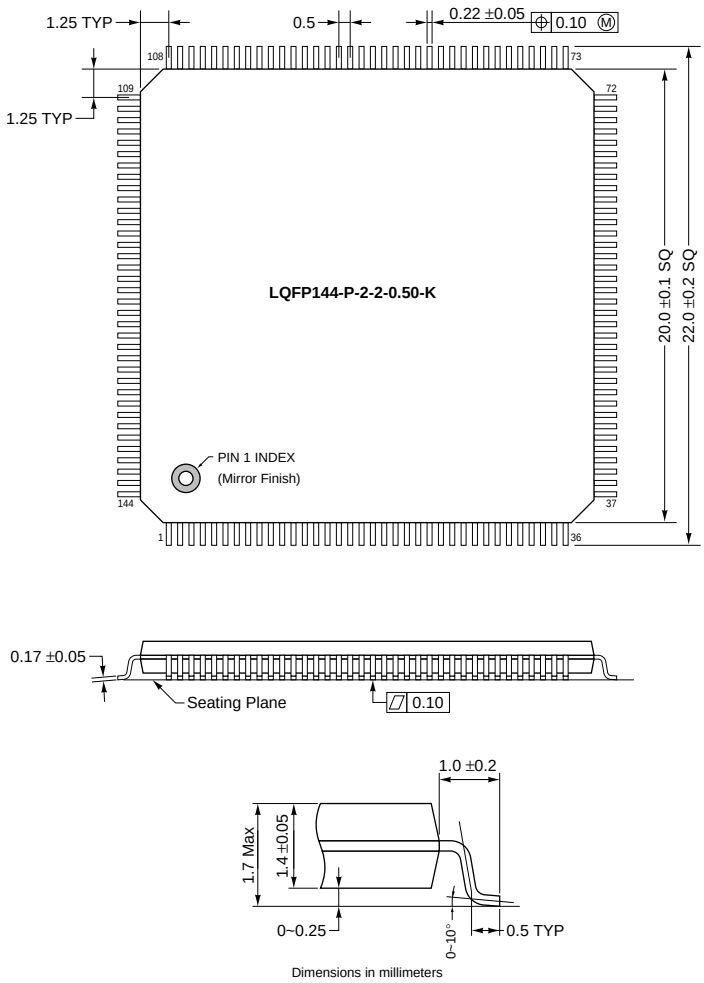


Figure 1. MSM7712 Block Diagram & Typical WLAN Card

PACKAGE DRAWING



Dimensions in millimeters

PIN CONFIGURATION

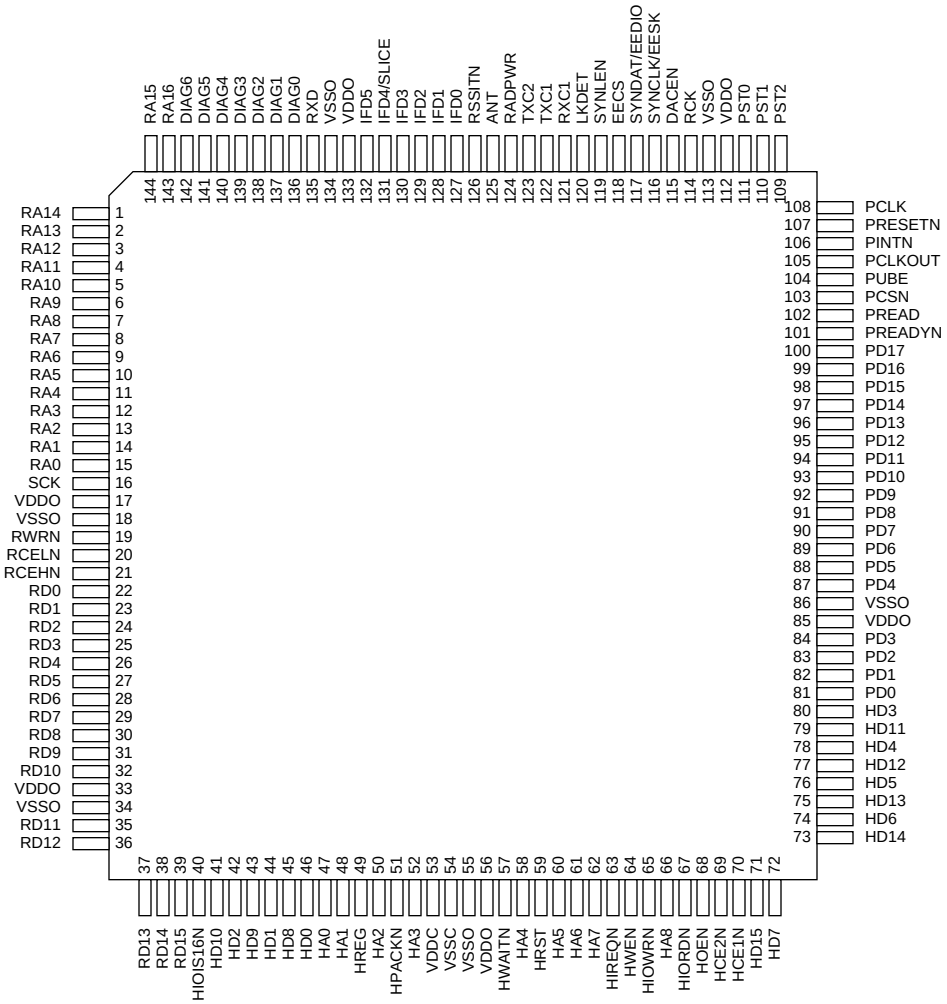


Figure 2. 144-Pin Plastic TQFP Pin Assignment

INTERFACE DESCRIPTIONS

Processor Interface

Most applications (e.g. PC add-in cards) require a local processor to handle the higher layers of the IEEE 802.11 protocol. The host computer typically runs a NDIS or ODI driver that communicates to the local processor via shared memory and interrupts. The local processor performs the higher layers of the IEEE 802.11 MAC protocol while the MSM7712GS-K performs the lower layers of MAC and the PHY under control of the local processor.

The MSM7712 can be configured to operate with 80C80 (V30) and 80C186 processor types. The processor configuration P_CONF is determined from the level of the PD lines during the MSM7712 reset. Designers should consult the appropriate processor datasheets and this section to understand how the processor interface works.

No external circuitry is required between the processor and the MSM7712. Table 1 specifies the connection of various processor signals to the MSM7712.

Processor Options

MSM7712GS-K	80C86, V30 (Max mode)	80C186
P_CONF	1	2
PA[17:16]	A[17:16]	AD[17:16]
PD[15:0]	AD[15:0]	AD[15:0]
PST2	BS2	S2
PST1	BS1	S1
PST0	BS0	S0
PREAD	-	-
PUBE	UBE	BHE
PCLKOUT	-	CLKOUT
PREADYN	READY	SRDY
PINTN	INT	INT0
PRESETN	RESET	RES
PCLK	CLK	X1

The output signal PREADYN, PINTN, PRESETN are active low or high to suit the different processor requirements

P_CONF option 1 provides an interface to the 80C86 or V30 processor. The processor must be set to maximum mode and a device with a 50% mark/space clock ratio at 16MHz and must be used (assuming a CSCK of 32 MHz).

P_CONF option 2 provides an interface to the 80C186 processor family with a 32 Mhz oscillator input.

All other values of P_CONF are reserved and should not be used.

Processor Interface Signal Descriptions

Pin Name	Direction	Description
PA[17:16]	Input	Provides the high address pins to the MSM7712. The usage depends on the shared memory size. The address space usage of the MSM7712 is 256 kbytes comprising MSM7712 registers and shared RAM.
PCSN	Input	Provides a processor chip select to the MSM7712. From reset, this pin is ignored and all processor accesses use the MSM7712. The pin can then be configured by software to be active high or active low.
PD[15:0]	Bidirectional	Provides the data bus and low addresses. The 80C86 and 80C186 processors have a multiplexed address/ data bus and are connected directly to PD [15:0]. The MSM7712 configuration is provided on these pins during reset. During reset (HRST asserted), the processor is reset and these pins are configured as input pins. The configuration is set by weak pull-up and pull-down resistors on PD [7:0]. Following reset and when the processor is not reset, the bus operates normally. See the Configuration Section for detailed options.
PST[2:0]	Input	Provides Processor Status to the MSM7712. Typically this differentiates between memory and I/O reads and writes.
PREAD		This pin is reserved for future product enhancements.
PUBE	Input	In conjunction with PD[0], this signal provides a decode of even byte, odd byte, or word accesses by the processor. The MSM7712 registers are accessed as words and the processor and shared RAMs can be accessed as bytes or words.
PCLKOUT	Input	Within a 80C186 processor-based system, CLKOUT should be connected to PCLKOUT pin. This is required such that PREADYN timing requirements relative to CLKOUT are met.
PREADYN	Input	This pin signals the processor that the bus cycle is complete. The only accesses that potentially require wait states are those to the shared RAM. The shared RAM is accessed by the MSM7712 host (via PCMCIA) and processor on a priority basis. This means the shared RAM may be busy when the processor requests an access and hence wait states are inserted until the shared RAM is available.
PINTN	Output	One interrupt is provided from the MSM7712 to the processor. A fixed interrupt vector is provided on the data bus for interrupt acknowledge cycles. Although described as active low (by the xxxN convention), the pin state is active high or low depending on the processor selected.
PRESETN	Output	The processor is reset via the host computer with this signal. From card reset, the processor is typically held in reset until the program code is downloaded from the host. Although described as active low (by the xxxN convention) the pin state is active high or low depending on the processor selected.
PCLK	Output	The processor clock is provided by the MSM7712. From power up PCLK is set at SCK divided by 8. A register programs PCLK to be from SCK to SCK divided by 8. The PCLK frequency selection allows a processor to operate at either low power or maximum performance. Within a 80C186 system, the processor is synchronized to the MSM7712 by monitoring the processor CLKOUT signal and skipping PCLK periods if necessary. All processor types must use this clock. The MSM7712 expects the processor bus interface timing to be synchronized with this clock signal. Note: SCLK is typically 16 MHz or 32 MHz depending on which modem and processor is being used.

Shared RAM Interface

Local memory is provided for packet buffer and processor code and data. Memory size is flexible from 32K words to 128K words to support a range of applications (e.g. low-cost stations to high performance access points).

Memory is word-sized to allow maximum performance in packet transfer rate. The design allows the use of word-wide RAMs or a pair of byte-wide RAMs. The MSM7712 and host computer access shared RAM in words only. The processor can access the RAM as odd or even bytes in addition to words.

For minimal cost applications local processor code may reside in shared memory. This may affect the processor speed because accesses to shared memory may have wait states inserted.

The RAM access time is (1.5 clock cycles less 18 ns). Hence, with a MSM7712 clock (RCLK) of 16MHz, the RAM requires an access time better than 75 ns.

Shared RAM Interface Signal Descriptions

Pin Name	Direction	Description
RA[16:0]	Output	The RAM address is provided by these pins. A maximum address size of 128K words is supported.
RD[15:0]	Bidirectional	The RAM data is provided on these pins. Word or byte operations are supported. When the shared memory is not in use the data bus is output to prevent a floating data bus consuming power.
RCELN	Output	When asserted, a low byte (or word) shared RAM cycle is active.
RCEHN	Output	When asserted, a high byte (or word) shared RAM cycle is active.
RWRN	Output	When asserted, a write cycle is required. When deasserted a read cycle is required. This signal remains valid before and while RCELN and RCEHN are asserted.

E²PROM Interface

E²PROM support is provided to allow for non-volatile storage of the host interface configuration (e.g. PCMCIA CIS table) and wireless LAN parameters (e.g. local IEEE address, radio parameters). The design supports a 64, 128 or 256 byte E²PROM (e.g. 93C46,93C56, or 93C66 types).

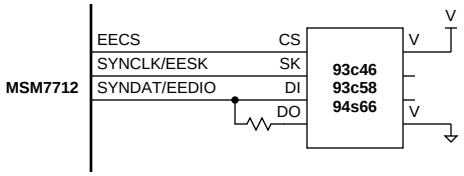


Figure 3. E²PROM Connections to MSM7712GS-K

The local processor can access the E²PROM for reads, writes and control functions. This is used to initialize the E²PROM and provide card parameter storage.

Following a reset by the host processor, the 64 or 128 bytes of E²PROM contents are automatically read to shared RAM to provide the configuration information for the host interface.

E²PROM Interface Signal Descriptions

Pin Name	Direction	Description
EEDIO	Bidirectional	This is a bidirectional data signal for the E²PROM. It is connected directly to DI of the E²PROM, and to DO via a resistor (see E²PROM application notes and *Figure 3*).
EECS	Output	This signal is connected to CS of the E²PROM to provide the chip select.
EESK	Output	This signal is connected to SK of the E²PROM to provide the clock. The clock rate is RCK divided by 64 (250 kHz with RCK at 16 MHz).

Host Interface (Between Adapter Card and Computer or Laptop)

The 16-bit PCMCIA interface is fully supported by the MSM7712 with no additional logic. Access to attribute memory (the CIS configuration data) and I/O memory (host registers) are provided.

In normal operation, access to the baseband controller registers and shared buffer memory is via a small number of I/O addresses. This requires minimum support in memory and input/output from the host computer.

The signals are defined in the PCMCIA standard. Note that the PCMCIA bus timing is independent of the system clock timing.

PCMCIA Interface

MSM7712GS-K	Pin Type	PCMCIA
H_CONF		0
HA[8:0]	Input	A[8:0]
HD[15:0]	Bidirectional	D[15:0]
HWEN	Input	WEN
HOEN	Input	OEN
HIORDN	Input	IORDN

PCMCIA Interface (Continued)

MSM7712GS-K	Pin Type	PCMCIA
HIOWRN	Input	IOWRN
HCE1N	Bidirectional	CE1N
HCE2N	Bidirectional	CE2N
HREG	Input	Reg
HWAITN	Output	WAITN
HIOIS16N	Output	IOIS16N
HPACKN	Output	PACKN
HRST	Input	RST
HIREQN	Output	IREQN

Host Interface Signal Descriptions

Pin Name	Direction	Description
HA[8:0]	Input	An attribute address range of 512 even bytes accesses is supported. An I/O space of 4 words is used (i.e. HA[2:0] is used and HA[8:0] is not used).
HD[15:0]	Bidirectional	Attribute memory is standardized to even byte accesses only. Input/Output memory is defined as word accesses only (to maximize packet transfer rates).
HOEN, HWEN, HIORDN,HIOWRN, HCE1N, HCE2N, HREG	Input	These signals provide the chip selects, read strobes, write strobes as defined in the PCMCIA standard
HPACKN, HIOIS16N	Output	These signals provide the chip selects, read strobes, write strobes as defined in the PCMCIA standard
HRST	Input	The card reset is provided by HRST. HRST must be asserted for a period of time from power up to allow the oscillator to settle. The MSM7712 is set to a default state while HRST is asserted and SCK is available. From HRST being deasserted the MSM7712 must download the CIS table from the E^2PROM to SRAM before the reset procedure is considered complete.
HIREQN	Output	HIREQN operates as the RDY/BSY line until the card is configured and hence remains low until the reset process is complete (as defined in the PCMCIA standard). Once reset is complete, HIREQN functions as a level-sensitive interrupt to the host.
HWAITN	Input	Wait states are potentially required when the host accesses the shared memory (to transfer packet data). Internal registers require no wait states.

Radio Interface

The radio interface supports simple, flexible control of the radio and its synthesizer. The control signal timing is programmable by the processor. *Figure 4* shows the connection to a typical radio architecture.

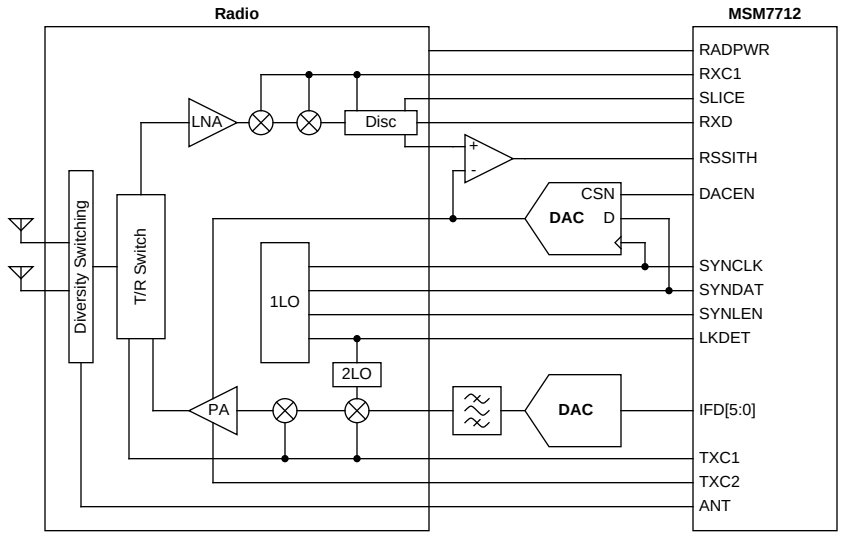


Figure 4. Typical FH Radio Interface

Radio Interface Signal Descriptions

Pin Name	Direction	Description
RXC1	Open-collector/drain Output	When asserted reception is enabled. RXC1 is always asserted during reception. This signal is programmable to be open-collector (active low) or open-drain (active high).
TXC, TXC2	Open-collector/drain Output	When asserted transmission is enabled. Both signals are programmable to be open-collector (active low) or open-drain (active high). Transmit is only activated following a receive (where Clear Channel Assessment is performed). The timing of TXC1 and TXC2 at the start of a transmit is programmable from the deassertion of RXC1. RXC2 is typically used for TX Power Amplifier switching, and its assertion depends on the power control mode selected in the MSM7712.
RADPWR	Open-collector/drain output	This pin is asserted to power up the radio circuitry (i.e. local oscillators) for reception. The pin is programmable to be open-collector (active low) or open-drain (active high).
ANT	Open-collector output	This pin selects one of two antennas for transmission or reception.
SLICE	Open-collector/drain output	This control pin determines the response time constant of an analog data slicer when using the internal modem with an analog data slicer circuit (options MSEL-0 or 1). This pin is programmable to be open-collector (active low) or open-drain (active high). The pin is asserted when CCA has determined a valid IEEE 802.11 GH signal (preamble is detected).

Radio Interface Signal Descriptions (Continued)

Pin Name	Direction	Description
SYNCLK, SYNDAT, SYNLEN	Open collector	These signals provide the interface to the radio synthesizer to select the transmit/receive carrier. Many synthesizers are supported by a flexible architecture. The data is output on SYNDAT ready for the rising edge of SYNCLK. SYNLEN is asserted during the programming, and the data is latched on the rising edge of SYNCLEN. SYNCLK is clocked at RCK divided by 2. SYNCLK and SYNDAT are also used to program a serial DAC used for TX power control, CCA threshold and RSSI measurement (see below). The synthesizer is programmed when the radio is idle. The RSSI and CCA threshold DAC is used at the start of receiving a packet. The TX power DAC is programmed at the start of transmitting packet. The radio provides indication of being in lock with LKDET. This input is active high or low (programmable), pulse sensitive, and latched so that both pulsed and steady out-of-lock signals are recognized. Glitches shorter than 2 RCK periods are ignored. Transmission is prevented when the synthesizer is out-of-lock
LKDET	Input	
DACEN	Open-collector	For TX power control, CCA threshold and RSSI measurement, data is also clocked into a serial DAC (10/12 bit type e.g. MAX515/MAX539) using the SYNCLK and SYNDAT lines as described above, except that DACEN is asserted during the programming, and the data is latched on the rising edge of DACEN. RSSITH is an input from a threshold comparison of the analog RSSI signal from the radio with the DAC output. It is high when the received signal exceeds the programmed threshold. This performs two purposes: • A minimum threshold of RSSI can be set before enabling the demodulator for CCA to reduce power. • Once a valid receive signal is determined (CCA invalid) the RSSI can be measured with the external comparator/DAC and a SAR within the MSM7712. The RSSI measurement is performed for internal and external modem options when CCA is determined. The same DAC can be used for both TX power control, RSSI threshold and RSSI measurement
RSSITH	Input	
RCK	Output	A clock to the radio is provided on this pin. The clock is derived from SCK when RADPWR is asserted, with fixed division ratio of one or two (selected by post-reset configuration SCK_CONF). RCK is typically 16MHz for the radio synthesizer reference.

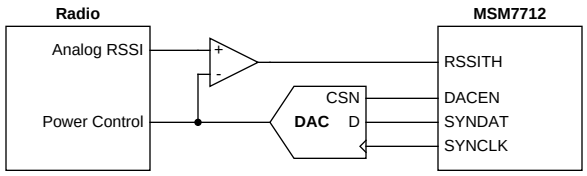


Figure 5. Connection of Serial DAC for Power Control and RSSI

MODEM Interface

The MSM7712 provides FH PLPC framing and the FH modem as defined by the IEEE 802.11 specification.The radio synthesizer control pins are used for all modem options. A diagnostic port is provided when the internal modem is used. Several options are provided by the internal FH modem selected by the PHY_VER[MSEL] register bits. The following table shows the pin usage for various modem options.

Modem Options and Pin Connections [1]

Modem Interface	FH Mbps (Low Cost)	FH 1/2 Mbps (Normal ADC)	FH 1/2 Mbps (Delta ADC)
MSEL	1	2	3
IFD[]	IFD[5:0] to TXIF DAC IFD[4] carries SLICE on RX	IFD[5:0] to TXIF DAC and IFD[3:0] from RXADC	IFD[5:0] to TXIF DAC (also used for Delta ADC)
RXD	Baseband RX data from radio	Recovered data (Debug out)	Input from Delta ADC comparator

1. All modem signals are synchronized to RCK.

Modem Interface Signal Descriptions

Pin Name	Direction	Description
IFD[5:0]	Bidirectional	If MSEL=1 (low cost for 1Mbps modem), IFD[5:0] are used to drive a 6-bit DAC at 32 MHz to provide the modulated transmit IF signal at 24 MHz. They are set to the DAC mid-value during receive. It is anticipated that a resistor ladder DAC will be used. If MSEL=2,3, (1/2 Mbps modem), IFD[5:0] are used to drive a 6-bit DAC at 32 MHz to provide the modulated transmit IF signal at 24 MHz. If MSEL=2 (1/2 Mbps modem, normal ADC) a 4-bit ADC (e.g. CA3304 type) provides digitized demodulated data at 16 MHz as input to the baseband controller on pins IFD[3:0] during receive. The ADC outputs must only be enabled during receive (e.g. by connecting RXC1 to the ADC output enable pin). If MSEL=3 (1/2 Mbps modem, delta ADC), a comparator is used to compare the value of the transmit IF DAC output to the receive demodulated signal, performing a tracing delta ADC function. The same 6-bit DAC (but at 16 MHz) is used on IFD[5:0] as during transmit, and the comparator input is connected to the RXD pin
RIFD[5:0]	Bidirectional	With MSEL=2 (1/2 Mbps modem, normal ADC) a 4-bit ADC (e.g. CA 3304 type) provides digitized demodulated data at 16 MHz as input to the baseband controller on pins IFD (3:0) during receive. The ADC outputs must only be enabled during receive (e.g. by connecting RXC) to the ADC output enable pin.
RXD	Input	When MSEL=1 (low-cost 1 Mbps modem), the RXD pin is used for baseband data input from a radio which has a built-in analog data slicer. The MSM7712 has a clock recovery circuitry to synchronize to the incoming data. The recovered clock is output on a diagnostic pin for test purposes. When MSEL=3 (1/2 Mbps modem, delta ADC), the delta comparator is input on this pin. The recovered clock from the demodulator is output on a diagnostic pin for test purposes.
DIAG[6:0]	Output	Various signals are provided on these pins as diagnostic aids. The registers PHY_CTL[DIAG] and DEM_CTL0[DTST] select what signals are provided on these pins.

General Signals

General Signal Descriptions

Pin Name	Direction	Description
SCK	Input	The system clock to the MSM7712 is provided by this pin. The clock must always be active (i.e. when reset is asserted). The WLAN card operates synchronously to this clock. The MSM7712 and radio operate at SCK/2. The internal modem operates at SCK (32 MHz). The processor operates from a division of SCK (divide by 1 to divide by 8) depending on a register (GLOB_CTL, see Programmers Reference) in the MSM7712. This signal is output as PCK.
VCSS, VPSS	Power	These pins serve as ground for the core logic and I/O pads.
VCDD	Power	This pin serves as power to the core at 3-V nominal.
VPDD	Power	These pins serve as power to I/O pads and can either be 3-V or 5-V nominal.

Test

TEST mode is activated when HRST and PST2 are both active low (an illegal state) in normal operation.

The MSM7712 operates normally when TEST is not asserted. When asserted, the following test modes are selected using processor data pins PD[1:0].

Test Select Options

PD[1]	PD[0]	Test	Description
0	0	Scan	Internal manufacturing scan test providing greater than 95% fault coverage. The scan select pin is PST0.
0	1	Hi-Z	All output pins are set to high impedance. This test allows external tester to drive MSM7712GS-K pins.
1	0	PinConn	All bidirectional, 3-state (except processor) and output pins are set to output and input pins determine state of output pins. This test ensures connectivity of the MSM7712G-K to the PCB
1	1	Reserved	

MODEM SPECIFICATION

The following two subsections describe modulator and demodulator specifications.

Modulator

The MSM7712 features an internal digital 24 MHz IF CP-FSK modulator. There are two modes of modulator operation:

- 1 Mbit/s, 2-ary CP-FSK
- 2 Mbit/s, 4-ary CP-FSK

Deviations can be set independently for both modes. Modes switch phase continuously in a single clock cycle.

- 1 Mbit deviation: 1MDEV = N x 32^6 /4096 Hz
- 2 Mbit deviation: 2MDEV = N x 3 x 32^6/4096 Hz

where N=0.63.

Digital on/off ramping from 0 ~ 24 µs of the modulator output power may be added under register control

Modulator radio requirements are:

- 6-bit DAC, clock at 32 MHz (offset binary).
- Anti-alias filtering to extract the 24-MHz alias
  (24 MHz IF will be -10 dB on 8 MHz fundamental from DAC output)
- Gaussian filtering, to translate CP-FSK into G-FSK, in accordance with the IEEE 802.11 specification
  (SAW filter at 240 MHz IF recommended)

Demodulator

The MSM7712 features a digital baseband demodulator, requiring an external discriminator. The MSM7712 supports two modes:

- 1Mbit/s 2-ary FSK
- 2 Mbit/s 4-ary FSK.

Both modes require a 1-Mbit preamble of 80 bits of reversals and 16 bits UW for acquisition of carrier and timing. The modem can then be switched to 2 Mbit/s if following headers require. Features of the demodulator include:

- Diversity switching control for two antennas.
- RSSI threshold wake-up of demodulator

The demodulator offers three possible interfaces to a limiter/discriminator radio. The supported interfaces are:

- Analog data slicer (1Mbit/s only)
- Post discriminator 4-bit ADC (offset binary)
- Post discriminator 1-bit ADC (provisional)

The demodulator's radio requirements are:

- 1 Mbit: 20 dB S/N from discriminator 10^{-5} BER (802.11 specifies sensitivity of 10^{-5} for 80 dBm)
- 2 Mbit: 30 dB S/N from discriminator 10^{-5} BER (802.11specifies sensitivity of 10^{-5} for 75 dBm)
- Discriminator linearity of ±5% required for specified 2 Mbit/s operation.
- 4-bit discriminator-to-ADC ranging, to cover approximately ±360 KHz.
- Carrier acquisition for analog slicer option within 4 µs, yielding a duty cycle better than 60:40 for a square wave (demodulation provides signal for carrier lock switch once preamble detected.
- RSSI threshold decision within 4 µs of antenna switching.
- 3-state ADC output during transmit (bus is shared with TxDAC).

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings [1]

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage Core	V_{CDD}	T_J = 25 °C V_{SS} = 0V	-0.3 to 4.6	V
Power Supply Voltage Pad	V_{PDD}		-0.3 ~ 7	
Input Voltage	V_I		-0.3 ~ V_{DD}+0.3	
Output Voltage	V_O		-0.3 ~ V_{DD}+0.3	
Input Current per Pad	I_I		-10 ~ +10	mA
Output Current per Pad	I_O		-10 ~+10	mA
Storage Temperature	T_{STG}		-65 ~ 150	˚C

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Range V_{SS} = 0 V

Parameter	Symbol	Range	Unit
Power Supply Voltage Core	V_{CDD}	2.7 ~ 3.6	V
Power Supply Voltage Pad	V_{PDD}	4.5 ~ 5.5	V
Ambient Temperature	Ta	-40 ~ +85	˚C
Oscillator Frequency	SCK	40	MHz

DC Characteristics V_{PDD} = 4.5 ~ 5.5 V, V_{PSS} = 0 V, T_J= -40 ~ +85 ˚C

Parameter	Symbol	Condition [1]	Min	Typ	Max	Unit
“H” level Input Voltage	V_{IH}	TTL Input	2.0	-	V_{PDD}+0.3	V
“L” Level Input Voltage	V_{IL}	TTL Input	-0.3	-	0.8	V
“H” Level Output Voltage	V_{OH}	I_{OH} = 100 µA	V_{PDD} – 0.2 2.4	-	-	V
“L” Level Output Voltage	V_{OH}		-	-	0.2 0.4	V
Standby Current (Core)	I_{CORE}	V_{DD} = 3 V, RST asserted, SCK active	-	56.5	-	mA
Standby Current (Pad)	I_{PAD}	V_{DD} = 5 V, RST asserted, SCK active	-	9.3	-	mA
Normal Current (Core)	I_{CORE}	V_{DD} = 3 V, RST asserted, SCK active	-	58.4	-	mA
Normal Current (Pad)	I_{PAD}	V_{DD} = 5 V, RST asserted, SCK active	-	30.2	-	mA

1. All inputs are CMOS thresholds. All outputs, 3-states, open-drains, open-collectors are rated at 2 mA drive. All bidirectional pins are rated at 4 mA drive.

AC Characteristics

Processor Interface

The MSM7712 is designed to operate with the V80C86, V33, V53A, and 80C186 processors. Refer to the appropriate processor data sheets for detailed information.

Host Interface

The MSM7712 meets the timing requirements of the PCMCIA interface. Wait states are used to provide the access times to the shared RAM when required.

Shared Memory Interface

Shared Memory Timing [1]

Parameter	Description	Min.	Typ.	Max.	Unit
$t_{S(RCE)}$	Setup time of address, WR strobe and data output to RCE asserted	20	-	-	ns
$t_{H(RCE)}$	Hold time of address, WR strobe and data output to RCE deasserted	10	-	-	
t_{RCE}	RCE low period (with 16/32 MHz SCK)	85	-	-	
$t_{S(D-CE)}$	Setup time of read data to RCE deasserted	10	-	-	
t_{ACC}	RAM access time Tce -Ts (d-rce)	75	-	-	
$t_{H(RCE-D)}$	Hold time of read data to RCE deasserted	0	-	-	
$t_{H(CYC)}$	Hold time before data bus driven low	50	-	70	

1. RCK at 16 MHz.

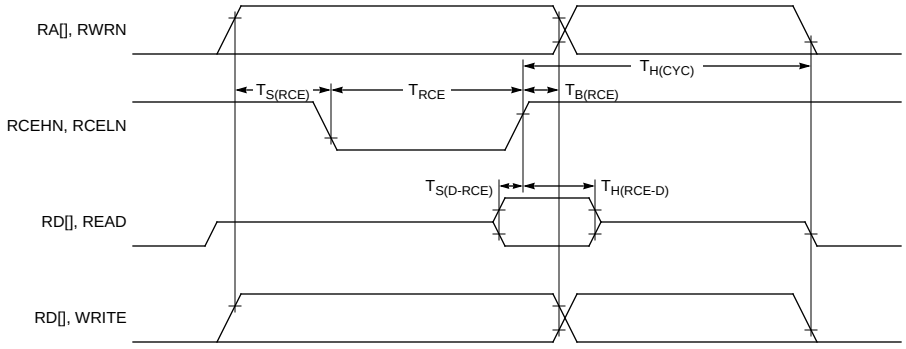


Figure 6. Shared Memory Timing

The shared memory cycle time is 2 RCK clock periods. When the memory interface is not active the data bus RD[15:0] is output (low). This ensures the shared memory data bus does not float and consume power.

E²PROM Interface

E²PROM Timing [1]

Parameter	Description	Min.	Typ.	Max.	Symbol
t_{SKL}	Clock low time	-	2000	-	
t_{SKH}	Clock high time	-	2000	-	
t_{SU}	CS,DI setup time to rising clock	-	2000-125	-	ns
$t_{S(DO-SK)}$	Setup time of read data to rising clock	10	-	-	
$t_{H(SK-DO)}$	Hold time of read data to rising clock	0	-	-	

1. RCK at 16 MHz.

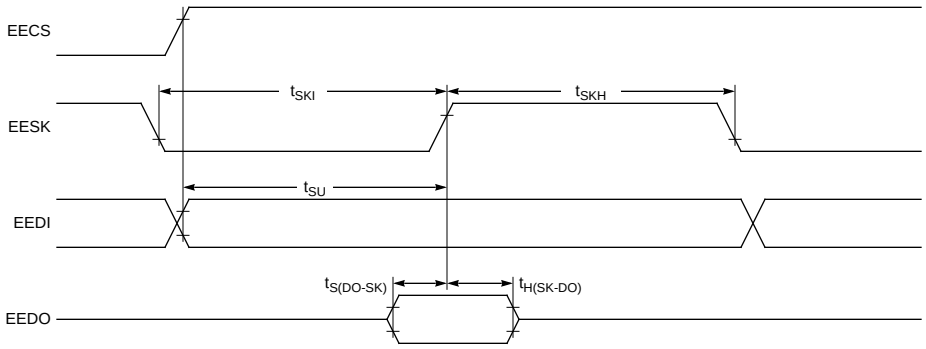


Figure 7. E²PROM Timing

Radio Control Timing

The following diagram shows a typical receive-transmit-receive sequence. RXPHE is asserted for receive. When CSENSE is detected(1) a packet is received. When CSENSE is inactive a transmit is requested by TXPHYE asserted. Delays between the receive control pins RXCx and transmit control pins TXCx are programmable to suit different radio designs. The packet is transmitted and when no further information is to be transmitted TXPHYE is deasserted. The modem holds CSENSE (2) until the ramp down is complete when the transmit control pins are deasserted and receive control pins are asserted. Note: RXPHYE, TXPHYE and CSENSE are internal signals.

Radio Control Timing [1]

Parameter	Description	Min.	Typ.	Max.	Symbol
t_{ONRT1}	RXC1 deasserted to TXC1 asserted	0	3000	7000	
t_{ONTIT2}	TXC1 asserted to TXC2 asserted	0	2000	7000	
t_{ONT1IF}	TXC2 asserted to IF data output	0	2000	15000	ns
$t_{OFFCST2}$	CSENSE deasserted to TXC2 deasserted	0	5	20	
$t_{OFFT2T1}$	TXC2 deasserted to TXC1 deasserted	0	4000	7000	
t_{OFFT1R}	TXC1 deasserted to RXC1 asserted	0	1000	7000	

1. RCK at 16 MHz

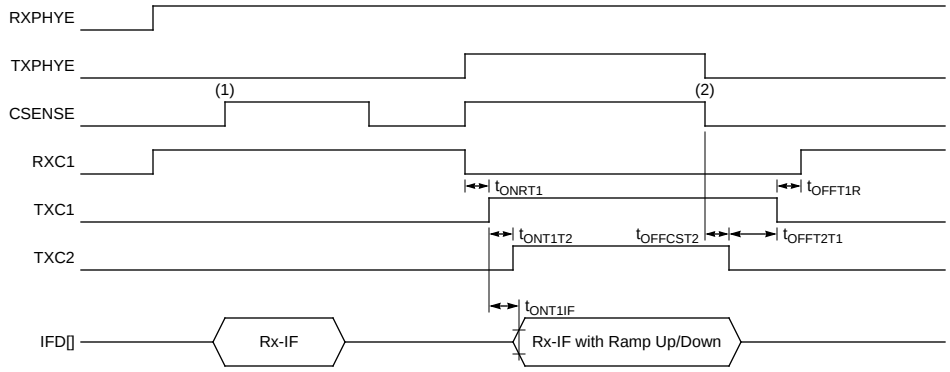


Figure 8. Radio Control Timing

Synthesizer and DAC Programming

Synthesizer Programming Timing [1]

Parameter	Description	Min.	Typ.	Max.	Symbol
t_{CKL}	Clock low time, 8 MHz	60	62.5	65	ns
t_{CKH}	Clock high time, 8 MHz	60	62.5	65	
$t_{D(DAT-CK)}$	Delay time of data from falling clock	10	-	-	
$t_{S(DAT-CK)}$	Setup time of data before rising edge	-	-	T_{CKL}-$T_{D(DAT-CK)}$	
$t_{D(CK-LE)}$	Delay time of latch enable from clock	-	-	T_{CKL}-$T_{D(DAT-CK)}$	

1. RCK at 16 MHz.

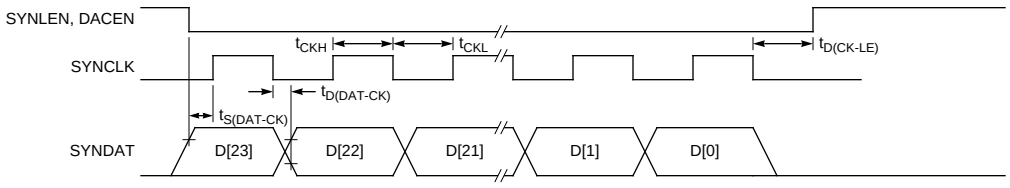


Figure 9. Synthesizer Programming Timing and DAC Timing

Modem Interface

IFD[5:0] Bus Timing (MSEL=1..3, Transmitting)

Parameter	Description	Min.	Typ.	Max.	Symbol
Td (ifd-rk)	Delay time of IFD[] data from rising SCK	10	–	–	ns

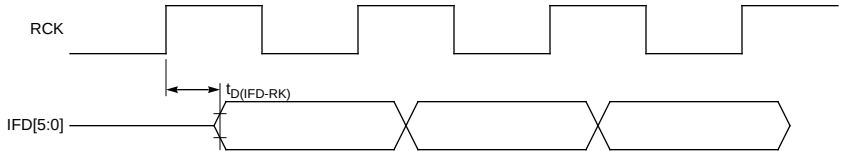


Figure 10. IFD[5:0] Bus Timing (MSEL = 1…3, Transmitting)

IFD[3:0] Bus Timing (MSEL=2, Receiving)

Symbol	Min.	Typ.	Max.	Notes (RCK at 16 MHz)
Ts (rk-ifd)	10	-	-	Setup time of IFD[] data to rising clock
Th (ifd-rk)	0	-	-	Hold time of IFD[] data after rising clock

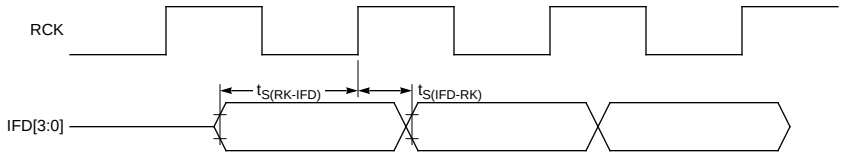
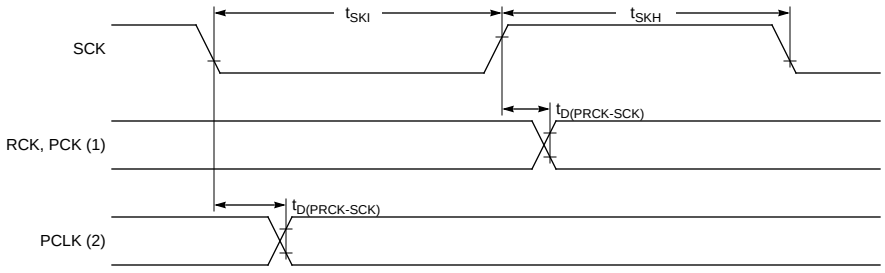


Figure 11. IFD[3:0] Bus Timing (MSEL = 2, Receiving)

SCK, RCK, PCLK Timing

SCK, RCK, PCLK Timing

Symbol	Min.	Typ.	Max.	Notes (RCK at 16 MHz
Tskl	12.5	16.625	-	System Clock low time
Tskh	12.5	16.625	-	System Clock high time
Td (prck-sck)	0	10	20	Delay time from SCK rising edge to PCLK and SCK changing state



Note: PCLK (1) when PCLK_DIV = 2, 4, or 8.
PCLK (2) when PCLK_DIV = 1.

Figure 12. SCK, RCK, PCK Timing