FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12529-1E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89950 Series

MB89951/953/P955/PV950

■ OUTLINE

The MB89950 series of single-chip compact microcontroller using the F²MC*-8L family core which can operate at high-speeds and low voltages. They contain peripherals such as timers, UART, serial interfaces, external interrupts and a 168-pixel LCD controller/driver. It is best suited for use in LCD panels.

*: F²MC stands for FUJITSU Flexible Microcontroller.

■ FEATURES

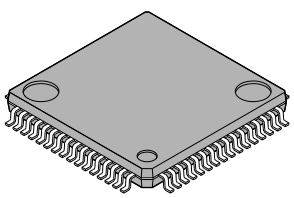
- Minimum instruction execution time: 0.8 µs at 5 MHz
- F²MC-8L family CPU core

Instruction system most suited to controllers
- Multiplication and division instructions
- 16-bit arithmetic operation
- Instruction test and branch instruction
- Bit manipulation instruction, etc.

(Continued)

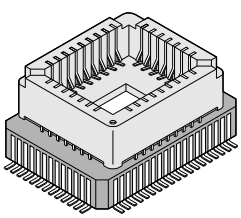
■ PACKAGE

64-pin Plastic QFP



(FPT-64P-M09)

64-pin Ceramic MQFP



(MQP-64C-P01)

MB89950 Series

(Continued)

- LCD controller/driver
  Maximum 42 segment outputs x 4 common outputs
  Build-in LCD driver split resistor
- Three-channel timer unit
  8-bit PWM timer: (usable as both reload timer and PWM timer)
  8-bit pulse width counter timer: (usable as both reload timer)
  20-bit timebased counter
- Two serial interfaces
  8-bit synchronous serial interface
  UART (5, 7, and 8-bit transfers possible)
- External-interrupt input: 2 channels
  2 channels can be used to clear the low-power consumption modes
  An edge detection function is provided for each channel
- Low-power consumption modes
  Stop mode (Oscillation stops to minimize the current consumption)
  Sleep mode (CPU stops to reduce current consumption to about 30%)
- Package: QFP-64 (0.65mm pitch)

■ PRODUCT LINEUP

Part number / Item	MB89951	MB89953	MB89P955	MB89PV950
Classification	Mass-produced products (Mask ROM product)		One-time PROM products	Piggyback/ evaluation and development ptoduct
ROM size	4 K × 8 bits (internal mask ROM)	8 K × 8 bits (internal mask ROM)	16 K × 8 bits (internal PROM, to be programmed with general-purpose EPROM programmer)	32 K × 8 bits (external ROM)
RAM size	128 × 8 bits	256 × 8 bits	512 × 8 bits	1024 × 8 bits
CPU functions	The number of basic instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits Minimum imstruction execution time: 0.8 µs at 5 MHz (V_{CC} =5.0 V) Interrupt processing time: 7.2 µs at 5 MHz (V_{CC} =5.0 V)			
Ports	I/O port (N-ch open-drain): 22 (also used as segment pin)*1 I/O port (N-ch open-drain): 4 (two of them are also used as LCD bias pins) I/O port (CMOS): 7 (6 used as peripheral) Total: 33 (max.)			
8-bit PWM timer	8-bit reload timer operation (toggle output possible) 8-bit resolution PWM operation Operation clock (pulse-width count timer output: 0.8 µs, 12.8 µs, 51.2 µs/5 MHz)			
8-bit pulse-width counter timer	8-bit reload timer operation 8-bit pulse width measurement (continuous measurement, High- and Low-width measurement, and one-cycle measurement) Operation clock (0.8 µs, 3.2 ms, 25.6 µs/5 MHz)			
8-bit serial I/O	8-bit length, selectable from least significant bit (LSB) first or most significant bit (MSB) first, transfer clock (external, 1.6 µs, 6.4 ms, 25.6 µs/5 MHz)			
UART	5-, 7-, 8-bit transfers possible, internal baud-rate generator (Max. 78125 bps/5 MHz)			
LCD controller/ driver	Common output: 4 Segment output: 42 (max.) Operation mode: 1/2 bias and 1/2 duty, 1/3 bias and 1/3 duty, 1/3 bias and 1/4 duty LCD controller display RAM capacity: 42 × 4 bits LCD driver split resistor: built-in (external resistor selectable)			
External interrupt	2 (edge selectable: one serving as pulse-width count timer input)			
Standby mode	Sleep mode, stop mode			
Power supply voltage*2	2.2 V to 6.0 V		2.7 V to 6.0 V	
EPROM	—			MBM27C256A-20TV (LCC package)

*1: Mask Option.
*2: Varies with conditions such as the operating frequency. (See "■ Electrical Characteristics".)

MB89950 Series

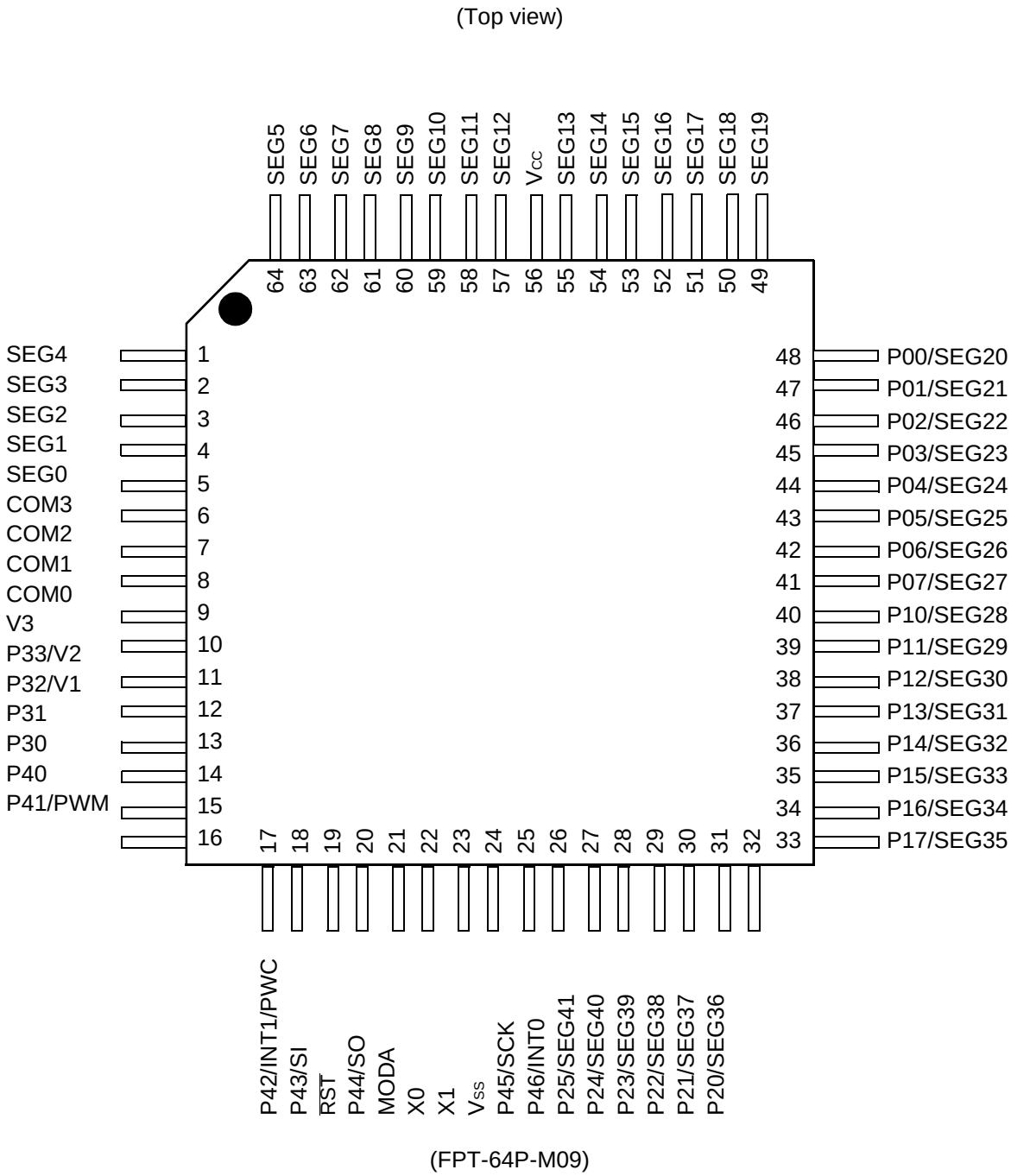
■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89951	MB89953	MB89P955	MB89PV950
FPT-64P-M09	○	○	○	×
MQP-64C-P01	×	×	×	○

○ : Available × : Not available

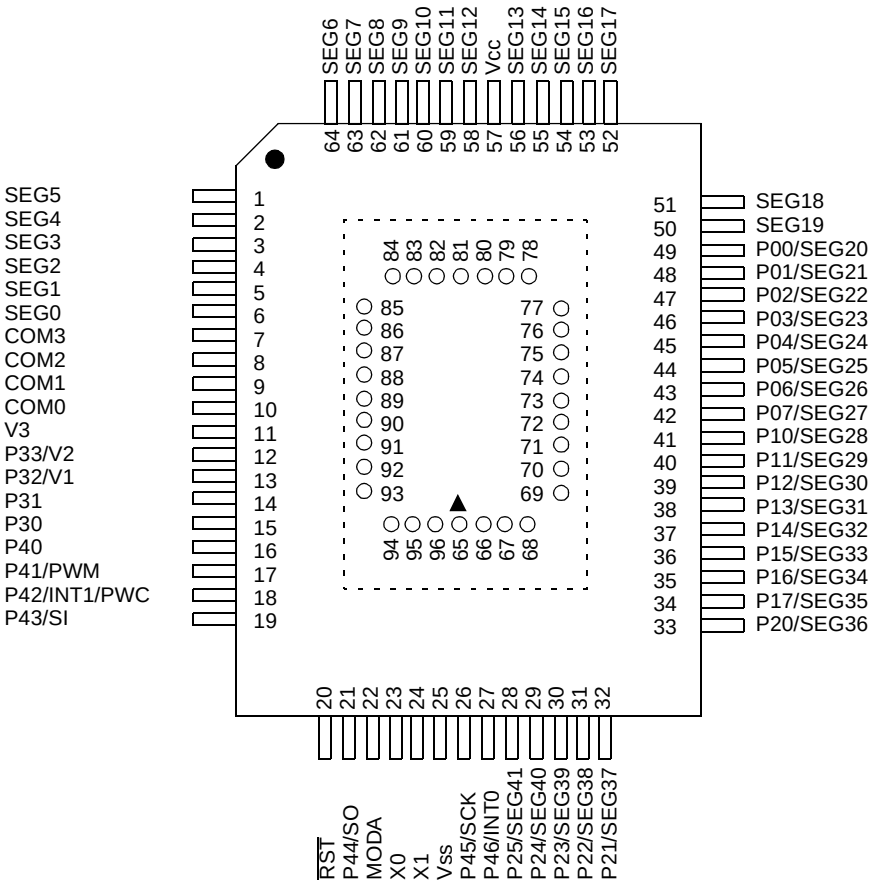
Note: For more information about each package, see section “■ Package Dimensions.”

■ PIN ASSIGNMENT



MB89950 Series

(Top view)



(MQP-64C-P01)

- **Pin assignment on package top (MB89PV950 only)**

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
65	N.C.	73	A2	81	N.C.	89	$\overline{OE}$
66	V_{PP}	74	A1	82	O4	90	N.C.
67	A12	75	A0	83	O5	91	A11
68	A7	76	N.C.	84	O6	92	A9
69	A6	77	O1	85	O7	93	A8
70	A5	78	O2	86	O8	94	A13
71	A4	79	O3	87	$\overline{CE}$	95	A14
72	A3	80	V_{SS}	88	A10	96	V_{CC}

N.C.:Internally connected. Do not use.

■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Function
QFP*1	MQFP*2			
22	23	X0	A	Clock oscillator pins
23	24	X1		
21	22	MODA	B	Operation-mode select pin This pin is connected directly to V_{SS} with pull down resistor.
19	20	$\overline{RST}$	C	Reset I/O pin This pin consists of an N-ch open-drain output with a pull-up resistor and hysteresis input. A Low level is put out from this pin. A “LOW” voltage on this port generates a RESET condition
48 to 41	49 to 42	P00/SEG20 to P07/SEG27	D	N-channel open-drain type general-purpose I/O ports Also serve as LCDC controller segment outputs. Switching between port output and segment output is performed by the mask option every 8 bits.
40 to 33	41 to 34	P10/SEG28 to P17/SEG35	D	N-channel open-drain type general-purpose I/O ports Also serve as LCDC controller segment outputs. Switching between port output and segment output is performed by the mask option.
32 to 27	33 to 28	P20/SEG36 to P25/SEG41	D	N-channel open-drain type general-purpose I/O ports Also serve as LCDC controller segment outputs. Switching between port output and segment output is performed by the mask option.
14 to 11	15 to 12	P30 to P31	F	N-channel open-drain type general-purpose I/O ports
12 to 11	13 to 12	P32/V1 to P33/V2	D	N-channel open-drain type general-purpose I/O ports Also serve as LCDC controller power supply.
15	16	P40	E	General-purpose I/O port A pull-up resistor option is provided.
16	17	P41/PWM	E	General-purpose I/O port Serves as PWM timer toggle output (PWM). A pull-up resistor option is provided.
17	18	P42/PWC/INT1	E	General-purpose I/O port Also serves as pulse-width count timer input (PWC) and external interrupt input (INT1) The PWC and INT1 inputs are of a hysteresis type. A pull-up resistor option is provided.
18	19	P43/SI	E	General-purpose I/O port Also serves as serial I/O and UART data input (SI) The SI input is of a hysteresis type. A pull-up resistor option is provided.
20	21	P44/SO	E	General-purpose I/O port Also serves as serial I/O and UART data output (SO). A pull-up resistor option is provided.

*1: FPT-64P-M09
*2: MQP-64C-P01

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Pin no.		Pin name	Circuit type	Function
QFP*1	MQFP*2			
25	26	P45/SCK	E	General-purpose I/O port Also serves as serial I/O and UART clock input/output (SCK). The SCK input is of a hysteresis type. A pull-up resistor option is provided.
26	27	P46/INT0	E	General-purpose input port Also serves as external-interrupt input (INT0). The input is of a hysteresis type. A pull-up resistor option is provided.
5 to 1, 64 to 57, 55 to 49	6 to 1, 64 to 58, 56 to 50	SEG0 to SEG4, SEG5 to SEG12, SEG13 to SEG19	G	For LCDC controller segment ouput
9 to 6	7 to 10	COM0 to COM3	G	For LCDC controller common output
10	11	V3	—	For LCD driver power supply
56	57	V_{CC}	—	Power supply Pin
24	25	V_{SS}	—	Power supply (GND) Pin

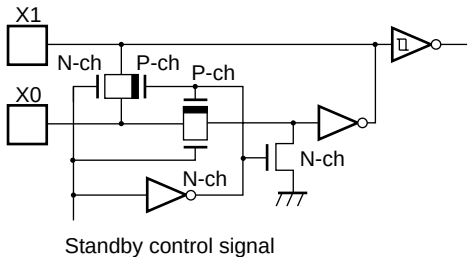
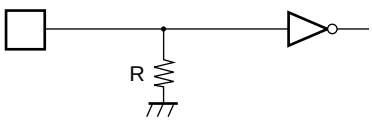
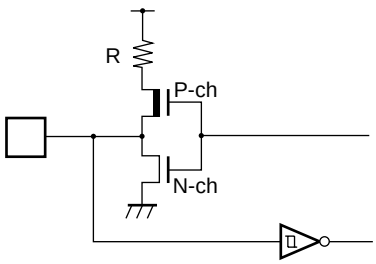
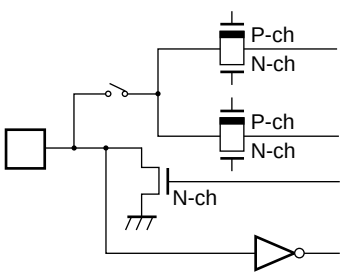
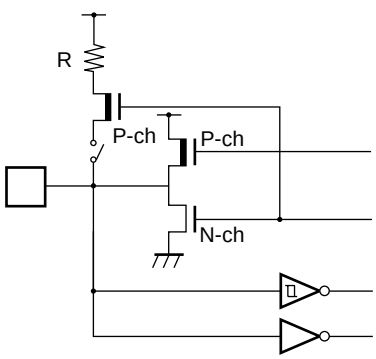
*1: FPT-64P-M09
*2: MQP-64C-P01

- **External EPROM pins (MB89PV950 only)**

Pin no.	Pin name	I/O	Function
66	V_{PP}	O	“H” level output pin
67 68 69 70 71 72 73 74 75	A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins
77 78 79	O1 O2 O3	I	Data input pins
80	V_{SS}	O	Power supply (GND) pins
82 83 84 85 86	O4 O5 O6 O7 O8	I	Data input pins
87	CE	O	ROM chip enable pin Outputs “H” during standby.
88	A10	O	Address output pin
89	OE	O	ROM output enable pin Outputs “L” at all times.
91 92 93 94 95	A11 A9 A8 A13 A14	O	Address output pins
96	V_{CC}	O	EPROM power supply pin
65 76 81 90	N.C.	—	Internally connected pins Be sure to leave them open.

MB89950 Series

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Crystal oscillator • Feedback resistor: Approx. 1 MΩ/5.0 V (1 to 5 MHz)
B		• CMOS input • Pull-down resistor (N-ch)
C		• Output pull-up resistor (P-ch): Approx. 50 kΩ (5.0 V) • Hysteresis input
D		• N-ch open-drain output • CMOS input • The segment output is optional.
E		• CMOS output • CMOS input • Hysteresis input (peripheral input) • The pull-up resistor is optional.

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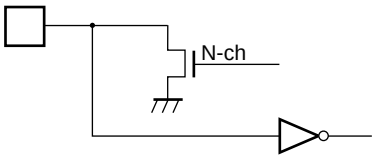
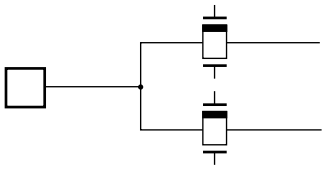
Type	Circuit	Remarks
F		• N-ch open-drain output • CMOS input
G		• LCDC output

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ Electrical Characteristics” is applied between V_{CC} and V_{SS}.

When latchup occurs, supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to pull-up or pull-down resistor.

3. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

4. Power Supply Voltage Fluctuations

Although operation is assured within the rated, rapid of V_{CC} power supply voltage, a rapid fluctuation of the voltage cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} rippli fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

5. Precautions when Using an External Clock

When an external clock is used, oscillation stabilization time is required even for power-on reset (optional) and wake-up from stop mode.

■ PROGRAMMING TO THE EPROM ON THE MB89P955

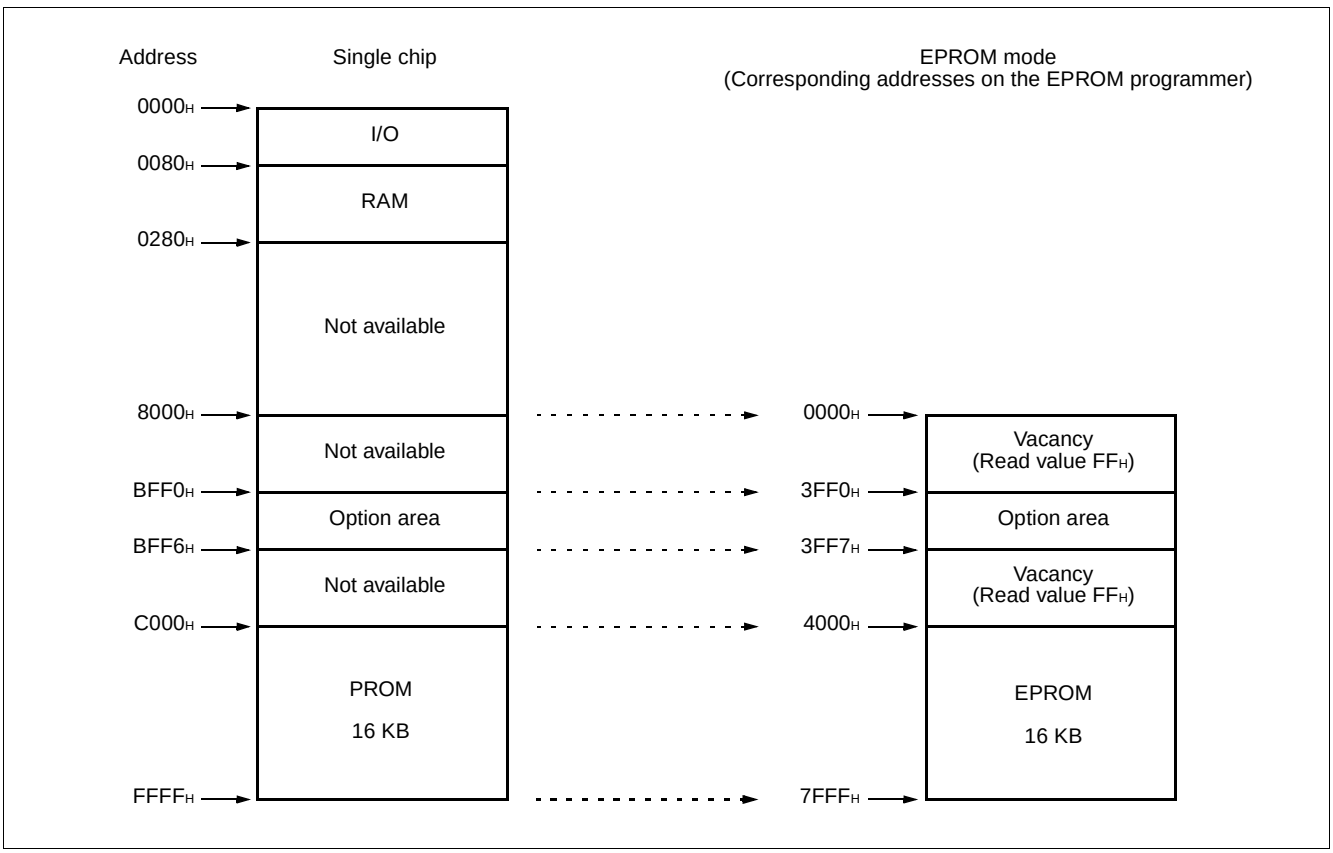
The MB89P955 is an OTPROM version of the MB89950 series.

1. Features

- 16-Kbyte PROM on chip
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in EPROM mode is diagrammed below.



3. Programming to the EPPROM

Functions equivalent to the MBM27C256A can be used in the MB89P955 EPROM mode. Accordingly, the user can write data with a general-purpose EPROM writer by using a dedicated adapter. Note that the electrical signature mode is not supported.

- Programming procedure

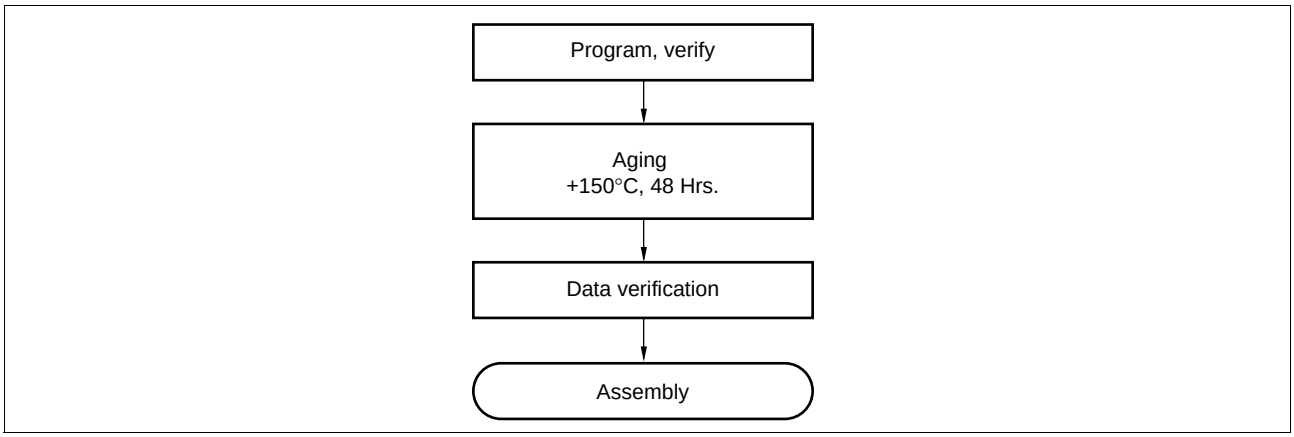
(1) Set the EPROM writer for the MBM27C256A.

(2) Load program data from 4000H to 7FFFH of the EPROM writer (Note that 0C000H to 0FFFFH in the operation mode are equivalent to 4000H to 7FFFH in the EPROM mode).
Load option data from 3FF0H to 3FF6H of the EPROM writer (See Bit Map on the next page for the correspondence to each option).

(3) Write the data with the EPROM writer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



5. Programming Yield

Due to its nature, bit programming test can't be conducted as Fujitsu delivery test. For this reason, a programming yield of 100% cannot be assured at all times.

6. EPROM Programmer Socket Adapter

Part number	MB89P955PFM
Package	QFP-64
Compatible socket adapter **Sun Hayato Co., Ltd.**	ROM-64QF2-28DP-8L3

Inquiry: Sun Hayato Co., Ltd.: TEL : (81)-3-3986-0403
FAX : (81)-3-5396-9106

7. Setting OTPROM Options

The programming procedure is the same as that for the PROM. Options can be set by programming values at the addresses shown on the memory map. The relationship between bits and options is shown on the following bit map:

- **OTPROM option bit map**

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3FF0H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Oscillation stabilization time 1: $2^{18}/f_C$ 0: $2^{14}/f_C$	Reset pin ouput 1: Yes 0: No	Power-on reset 1: Yes 0: No	Vacancy Readable and writable	Vacancy Readable and writable
3FF1H	Vacancy Readable and writable	P46 Pull-up 1: Yes 0: No	P45 Pull-up 1: Yes 0: No	P44 Pull-up 1: Yes 0: No	P43 Pull-up 1: Yes 0: No	P42 Pull-up 1: Yes 0: No	P41 Pull-up 1: Yes 0: No	P40 Pull-up 1: Yes 0: No
3FF2H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable
3FF3H	Vacancy Readable and Writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable
3FF4H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable
3FF5H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable
3FF6H	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable	Vacancy Readable and writable

Note: Each bit is set to ‘1’ as the initialized value, therefore the pull-up option is not selected.

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C256A-20TV

2. Programming Socket Adapter

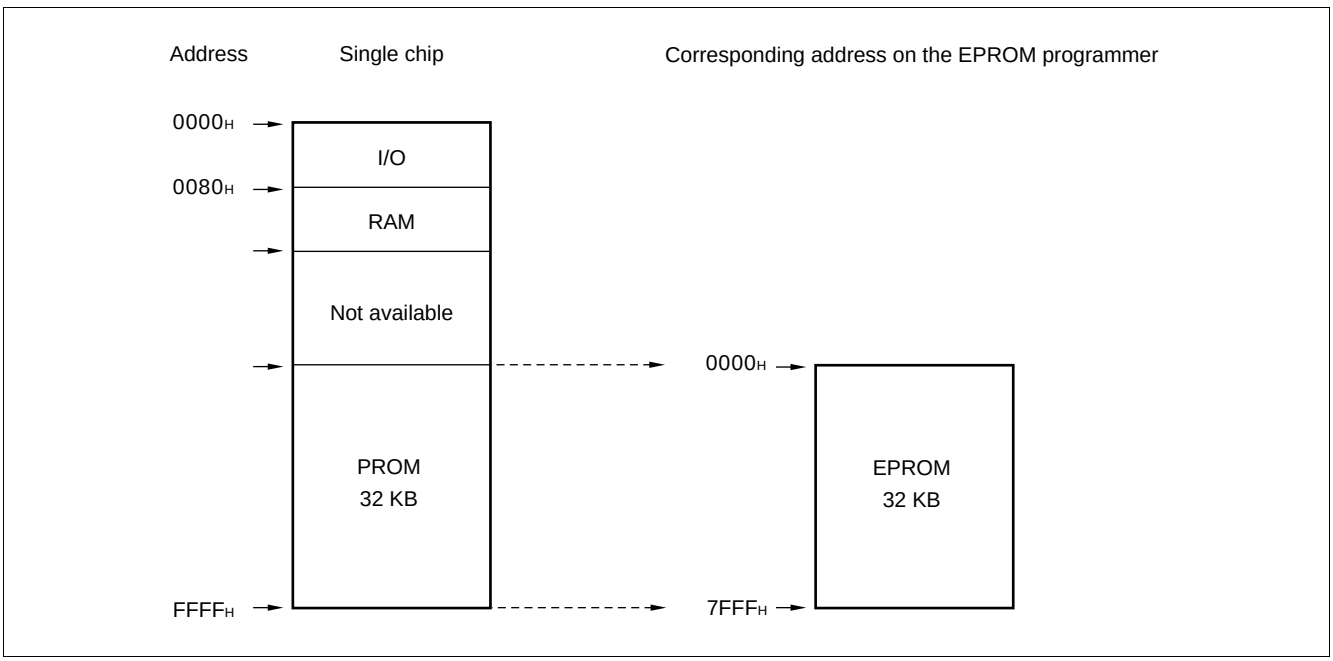
To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below:

Package	Adapter socket part number
LCC-32 (Rectangle)	ROM-32LC-28DP-YG

Inquiry: Sun Hayato Co., Ltd.: TEL: (81)-3-3986-0403
FAX : (81)-3-5396-9106

3. Memory Space

Memory space in each mode such as 32-Kbyte PROM, is diagrammed below.



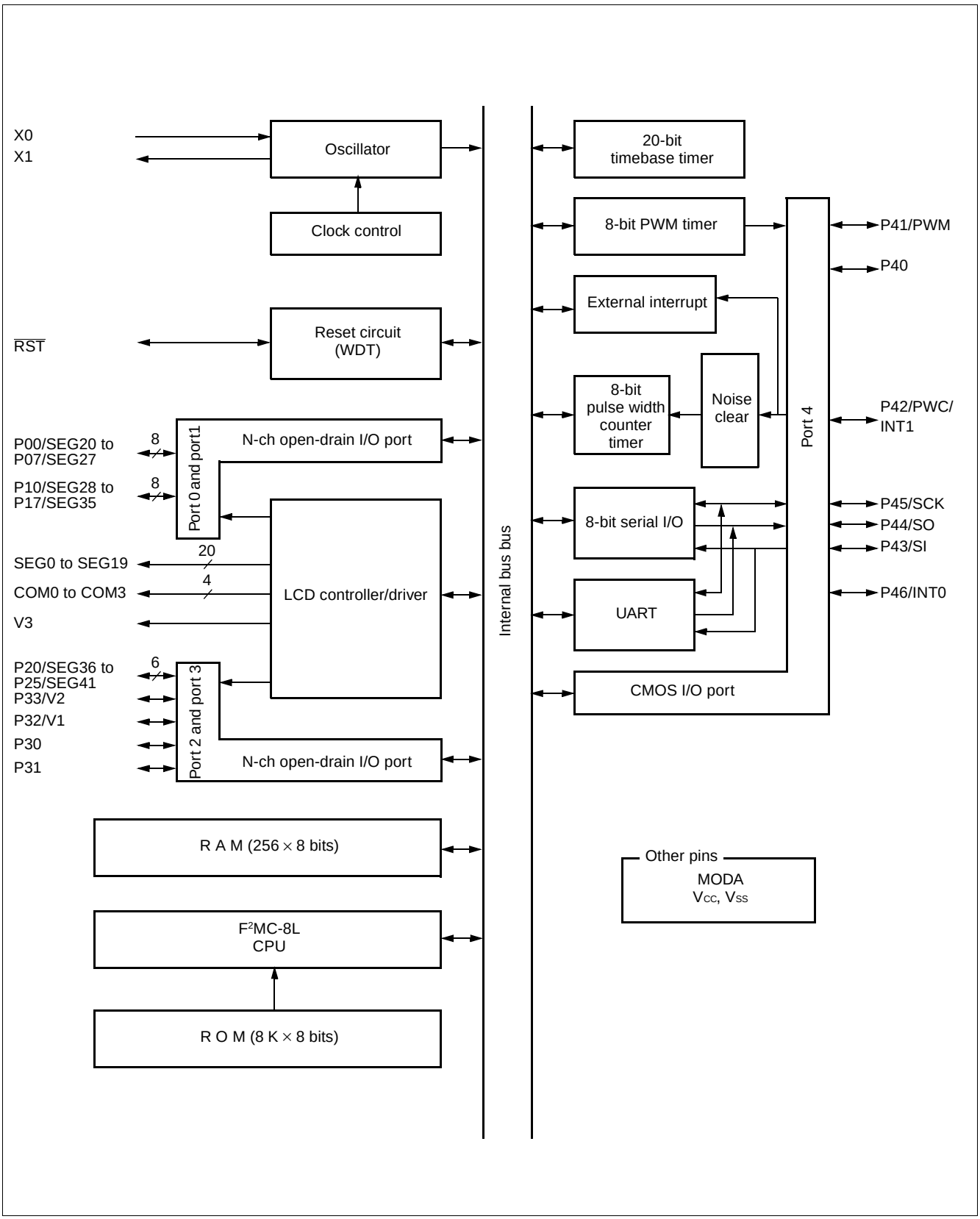
4. Programming to the EPROM

(1) Set the EPROM programmer for the MBM27C256A.

(2) Load program data into the EPROM programmer at 0007H to 7FFFH.

(3) Program with the EPROM programmer.

■ BLOCK DIAGRAM

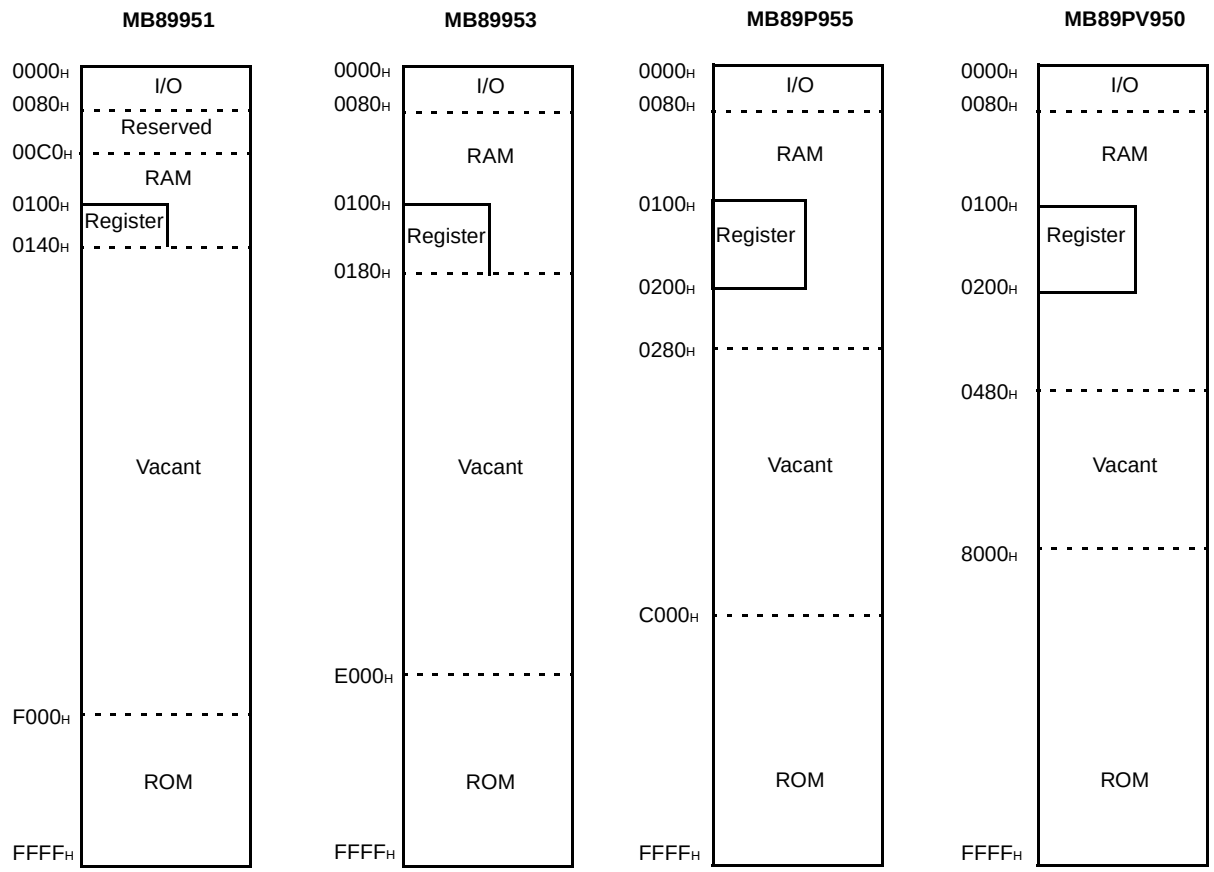


■ CPU CORE

1. Memory Space

F²MC-8L CPU has 64 Kbytes of memory. All I/O, data program areas are located in this space. The I/O area is near the lowest address and the data area is immediately above it. The data area can be divided into register, stack, and direct-address areas according to the applications. The program area is located near the highest address, and the tables of interrupt and reset vectors and vector-call instructions are at the highest address in this area. The following figure shows the structure of the memory space for the MB89950 series of microcontrollers.

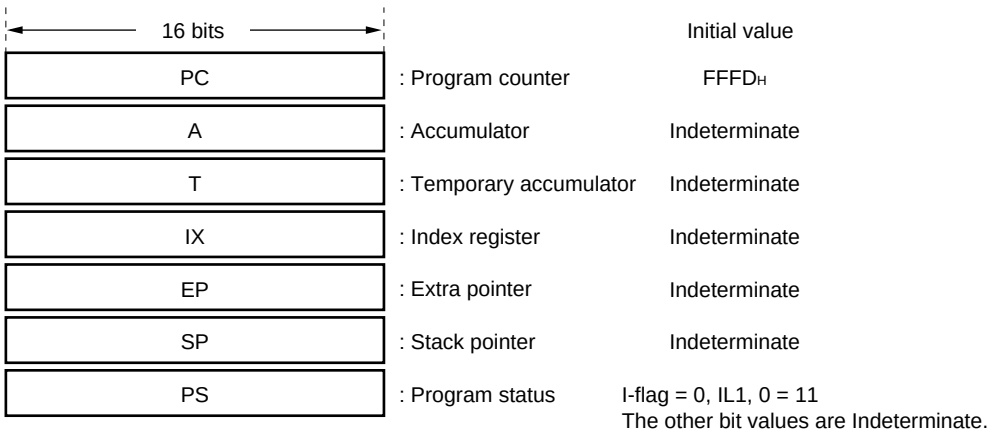
• **Memory Space**



2. Registers

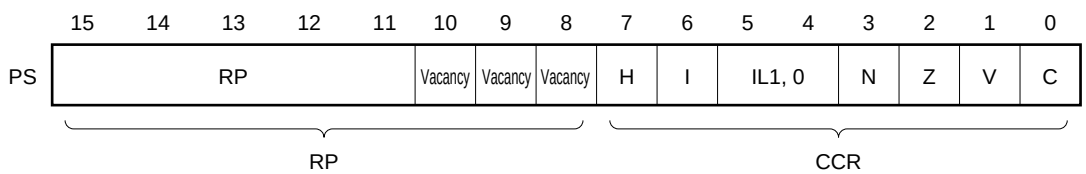
The F²MC-8L family has two types of registers; dedicated hardware registers in the CPU and general-purpose memory registers. The following registers are provided:

Program counter (PC):	A 16-bit register for indicating the instruction storage positions.
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit register which is used for arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit register for index modification
Extra pointer (EP):	A 16-bit pointer for indicating a memory address
Stack pointer (SP):	A 16-bit pointer for indicating a stack area
Program status (PS):	A 16-bit register for storing a register pointer, a condition code



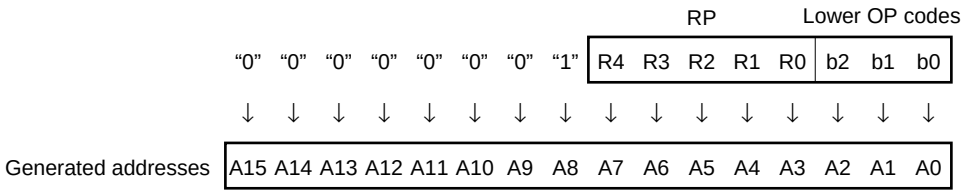
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

• Structure of the Program Status Register



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

- **Rule for Conversion of Actual Addresses of the General-purpose Register Area**



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data, and bits for control of CPU operations at the time of an interrupt.

H-flag: Set to '1' when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to '0' otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is enabled when this flag is set to '1'. Interrupt is disabled when the flag is cleared to '0'. Cleared to '0' at the reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low

N-flag: Set to '1' if the MSB becomes '1' as the result of an arithmetic operation. Cleared to '0' when the bit is cleared to '0'.

Z-flag: Set to '1' when an arithmetic operation results in '0'. Cleared to '0' otherwise.

V-flag: Set to '1' if the complement on '2' overflows as a result of an arithmetic operation. Cleared to '0' if the overflow does not occur.

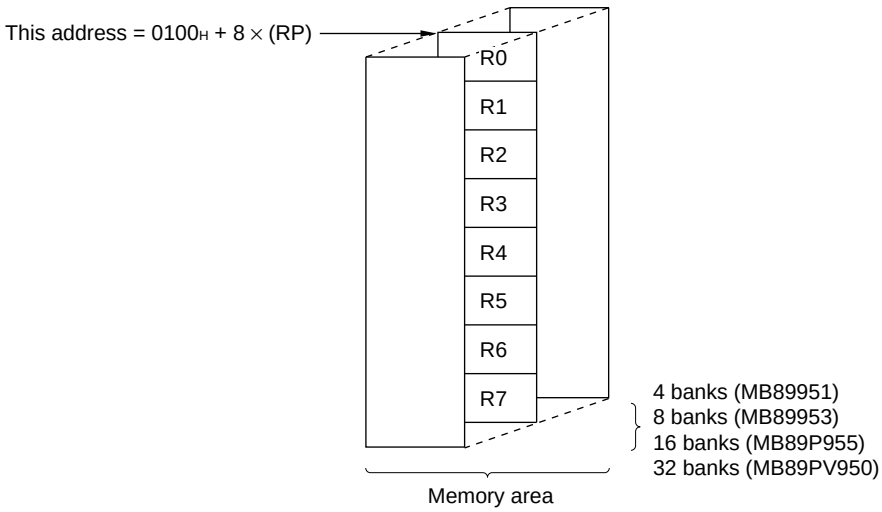
C-flag: Set to '1' when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to '0' otherwise.
Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: An 8-bit resister for storing data

The general-purpose registers are of 8 bits and located in the register banks of the memory. One bank contains eight registers. Up to a total of 4 banks can be used on the MB89951 and a total of 8 banks can be used on the MB89953 and a total of 16 banks can be used on the MB89P955 and a total of 32 banks can be used on the MB89PV950. The bank currently in use is indicated by the register bank pointer (RP).

• **Register Bank Configuration**



■ I/O MAP

Address	Read/write	Register name	Register description
00H	(R/W)	PDR0	Port 0 data register
01H	Vacancy		
02H	(R/W)	PDR1	Port 1 data register
03H	Vacancy		
04H	(R/W)	PDR2	Port 2 data register
05H to 07H	Vacancy		
08H	(R/W)	STBC	Standby control register
09H	(R/W)	WDTC	Watchdog timer control register
0AH	(R/W)	TBCR	Timebase timer control register
0BH	Vacancy		
0CH	(R/W)	PDR3	Port 3 data register
0DH	Vacancy		
0EH	(R/W)	PDR4	Port 4 data register
0FH	(W)	DDR4	Port 4 data direction register
10H	Vacancy		
11H			
12H	(R/W)	CNTR	PWM control register
13H	(W)	COMR	PWM compare register
14H	(R/W)	PCR1	PWC pulse width control register 1
15H	(R/W)	PCR2	PWC pulse width control register 2
16H	(R/W)	RLBR	PWC reload buffer register
17H	(R/W)	NCCR	PWC noise reduction control register
18H to 1BH	Vacancy		
1CH	(R/W)	SMR	Serial mode register
1DH	(R/W)	SDR	Serial data register
1EH	Vacancy		
1FH			
20H	(R/W)	SMC1	UART serial mode control register 1
21H	(R/W)	SRC	UART serial rate control register
22H	(R/W)	SSD	UART serial status/data register
23H	(R/W)	SIDR/SODR	UART serial data register
24H	(R/W)	SMC2	UART serial mode control register 2

(Continued)

(Continued)

Address	Read/write	Register name	Register description
25_H to $2F_H$	Vacancy		
30_H	(R/W)	EIC1	External interrupt 1 control register 1
31_H to 63_H	Vacancy		
64_H to 78_H	(R/W)	VRAM	Display data RAM
79_H	(R/W)	LCDR	LCD control register
$7A_H$	(R/W)	SEGR	Segment output select register
$7B_H$	Vacancy		
$7C_H$	(W)	ILR1	Interrupt level setting register 1
$7D_H$	(W)	ILR2	Interrupt level setting register 2
$7E_H$	(W)	ILR3	Interrupt level setting register 3
$7F_H$	—	ITR	Interrupt test register

Note: Do not use vacancies.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	
LCD power supply voltage	V3	V_{SS} – 0.3	V_{SS} + 7.0	V	
Input voltage	V_{I1}	V_{SS} – 0.3	V_{CC} + 0.3	V	All the pins must not exceed VSS + 7.0 V, excluding P00 to P07, P10 to P17, P20 to P25,P32 to P33 in MB89P955/PV950
	V_{I2}	V_{SS} – 0.3	V_{SS} + 7.0	V	Applicable to P00 to P07, P10 to P17, P20 to P25 (port select) in MB89951/953
	V_{I3}	V_{SS} – 0.3	V3	V	*P00 to P07, P10 to P17, P20 to P25, P32 to P33
Output voltage	V_{O1}	V_{SS} – 0.3	V_{CC} + 0.3	V	All the pins must not exceed Vss + 7.0 V, excluding P00 to P07, P10 to P17, P20 to P25, P32 to P33 in MB89P955/PV950
	V_{O2}	V_{SS} – 0.3	V_{SS} + 7.0	V	Applicable to P00 to P07, P10 to P17, P20 to P25 (port select) in MB89951/953
	V_{O3}	V_{SS} – 0.3	V3	V	P00 to P07, P10 to P17, P20 to P25, P32 to P33*
“L” level output current	I_{OL}	—	10	mA	Applicable to all pins except power supply pin.
“L” level average output current	I_{OLAV}	—	4	mA	Applicable to all pins excluding power supply pin. Specified as the average value in 1 hour.
“L” level total output current	$\sum I_{OL}$	—	40	mA	
“H” level output current	I_{OH}	—	–5	mA	Applicable to all pins excluding power supply pin.
“H” level average output current	I_{OHAV}	—	–2	mA	Applicable to all pins excluding power supply pin. Specified as the average value in 1 hour.
“H” level total output maximum current	$\sum I_{OH}$	—	–10	mA	
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

* : It is only suitable to MB89P955/PV950.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

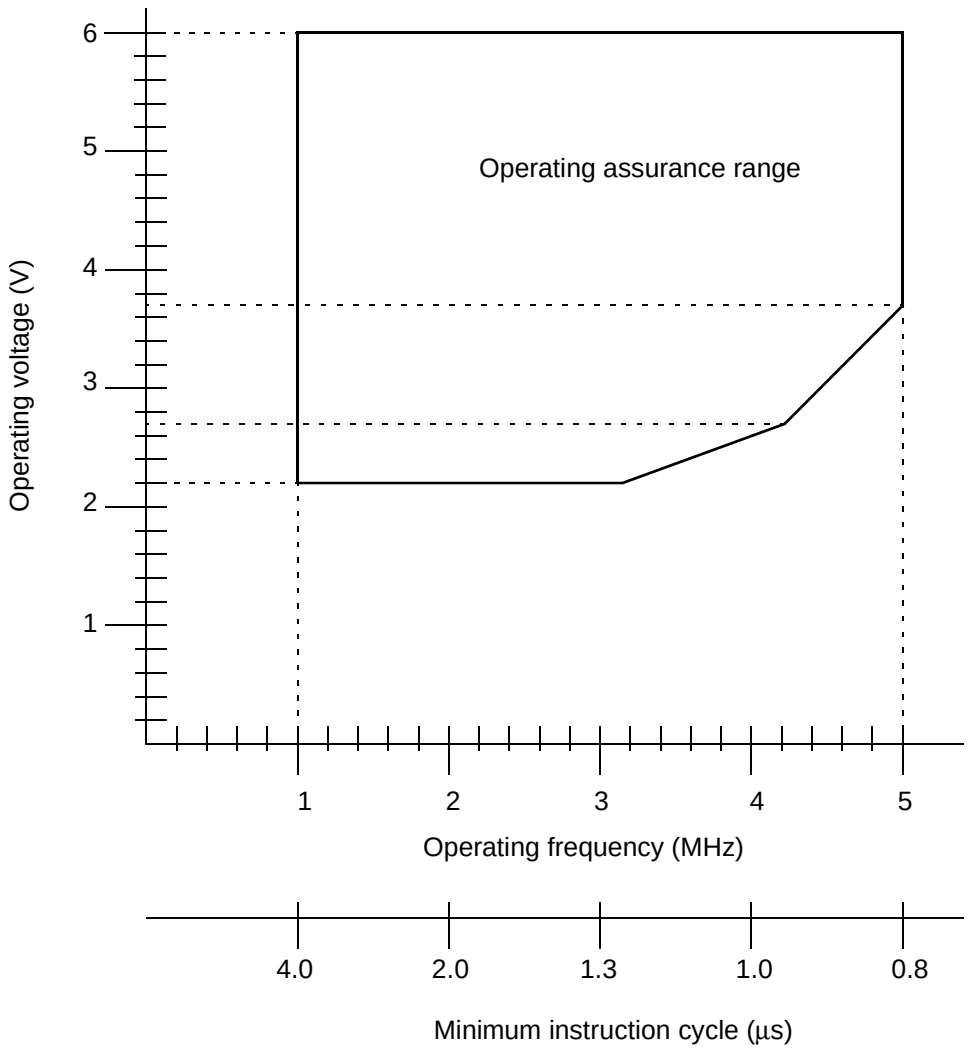
2. Recommended Operating Conditions

(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	2.2*	6.0	V	Usual operation guarantee range
		1.5	6.0	V	RAM-data-holding guarantee range at stop mode
LCD power supply voltage	V3	V_{SS}	6.0	V	V3 pins for MB89953 The voltage range supplied to LCD and its optimum value depend on the LCD
Operating temperature	T_A	–40	+85	°C	

* : This value varies with the operating frequency and analog assurance range. See Figure 1.

• Figure 1 Operating Voltage vs. Main Clock Operating Frequency (MHz)



WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

3. DC Characteristics

(V_{CC} = V3 = +5.0 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17, P20 to P25, P30 to P31, P40 to P46	—	0.7 V_{CC} *1	—	0.3 V_{CC} *1	V	
		P32,P33	—	0.7 V_{CC} *1	—	V3	V	
	V_{IHS}	$\overline{RST}$, INT0, SCK, SI, PWC/INT1	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17, P20 to P25, P30 to P33, P40 to P46	—	V_{SS} – 0.3	—	0.3 V_{CC} *1	V	
	V_{ILS}	$\overline{RST}$, MODA, INT0, SCK, SI, PWC/INT1	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
Open-drain output pin Applied voltage	V_D	P30 to P31, P20 to P25, P10 to P17, P00 to P07	—	V_{SS} – 0.3	—	V_{SS} + 6.0	V	P00 to P07, P10 to P17, P20 to P25 (port select) in MB89951/953
		P32, P33	—	V_{SS} – 0.3	—	V3	V	P32 to P33 (port select)
"H" level Output voltage	V_{OH}	P40 to P46	I_{OH} = –2.0 mA	4.0	—	—	V	
"L" level Output voltage	V_{OL1}	P00 to P07, P10 to P17, P20 to P25, P30 to P33	I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	$\overline{RST}$, P40 to P46	I_{OL} = 4.0 mA	—	—	0.4	V	
Input leakage current (Hi-z output leak current)	I_{LI1}	MODA, P30, P31, P40 to P46	0.45 V < VI < V_{CC}	—	—	±5	µA	When pull-up option is not selected
		P00 to P07, P10 to P17, P20 to P25, P32, P33		—	—	±5	µA	When pull-up option is not selected
Pull-up resistance	R_{PULL}	$\overline{RST}$, P40 to P46	V_I = 0.0 V	25	50	100	kΩ	When pull-up option is selected
Common Output impedance	R_{VCOM}	COM0 to COM3	V1 to V3 = +5.0 V	—	—	2.5	kΩ	

(Continued)

(Continued)

(V_{CC} = V3 = +5.0 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Segment Output impedance	R_{VSEG}	SEG0 to SEG41	V1 to V3 = +5.0 V	—	—	15	kΩ	
LCD divided resistance	R_{LCD}	—	V1 to V3	30	60	120	kΩ	
LCD leak current	I_{LCDL}	V1 to V3, COM0 to COM3, SEG0 to SEG41	—	—	—	±10	µA	
Pull-down resistance	—	MODA	—	TBD	TBD	TBD	kΩ	
Power Supply voltage	I_{CC}	V_{CC}	F_C = 5 MHz t_{inst}*3 = 0.8µs	—	3.5	5.0	mA	Main RUN mode
	I_{CCS}	V_{CC}	FC = 5 MHz t_{inst}*3 = 0.8µs	—	1.1	1.7	mA	Main SLEEP mode
	I_{CCH}	V_{CC}	T_A = +25°C	—	0.1	1	µA	STOP mode
Input capacitance	C_{IN}	Except V_{CC} and V_{SS}	f = 1 MHz	—	10	—	pF	

*1: Port input voltage is smaller than V3 for MB89P955/PV950.

*2: TBD = To be determined

*3: For information on t_{inst}, see “(4) Instruction Cycle” in “4.AC Characteristics.”

Note: For pins for selection of segments (SEG8 to SEG31) and ports (P10 to P17, P40 to P47, P50 to P57), see the limits values of ports when port output is selected and those for segments when segment output is selected.

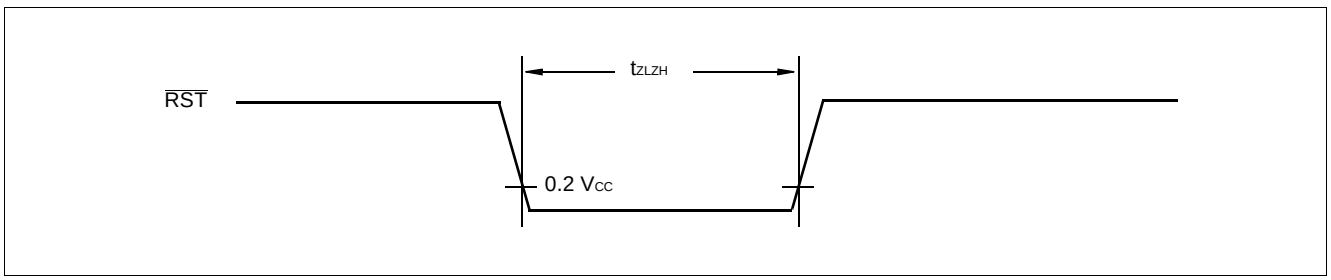
4. AC Characteristics

(1) Reset Timing

(V_{CC} = 5.0 V ±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	48 t_{XCYL}*	—	ns	

* : t_{XCYL} is the oscillation cycle (1/F_C) to input to the XO pin.

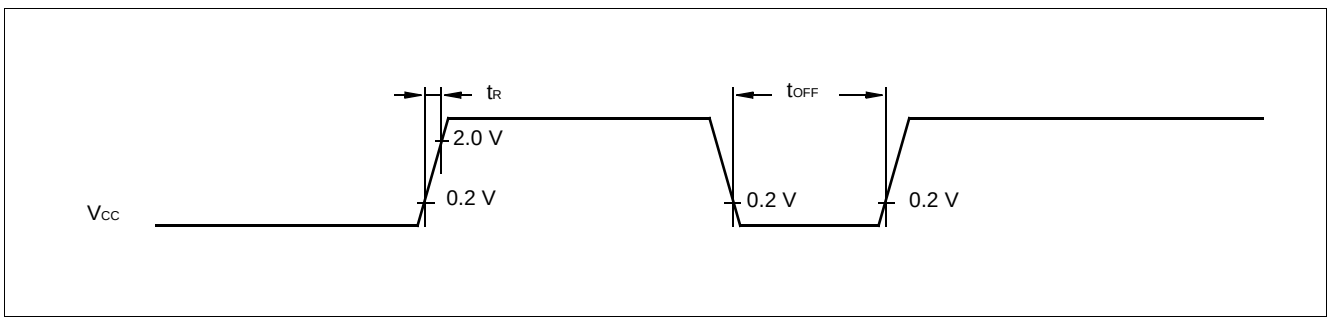


(2) Specifications for Power-on Reset

(V_{CC} = 5.0 V ±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}		1	—	ms	Min. interval time to the next power-on reset

Note: If power-on reset provided is selected, an abrupt change in the power supply voltage could cause a power-on reset. When changing the power supply voltage during operation, voltage fluctuations should be two or less times for smooth start-up.



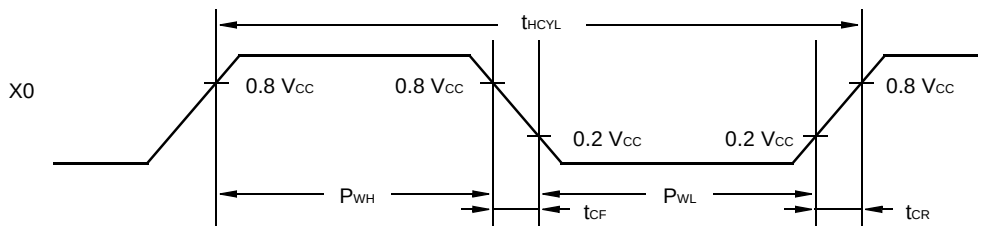
(3) Clock Timing

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

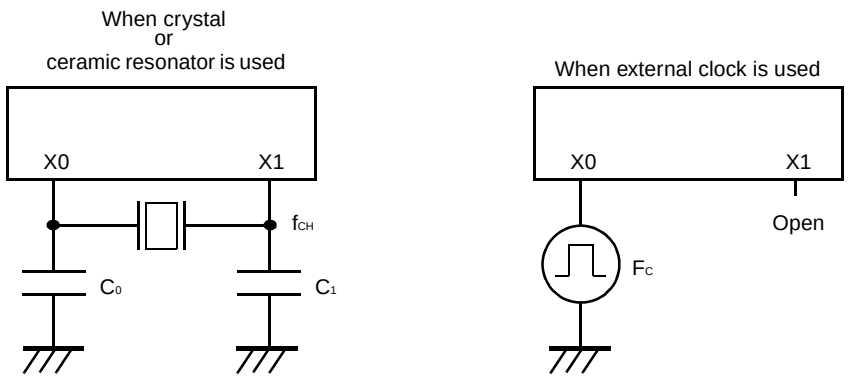
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min.	Typ.	Max.		
Clock frequency	F_C	X0, X1	1	—	5	MHz	
Clock cycle time	t_{HCYL}	X0, X1	400	—	2000	ns	
Input clock duty ratio*	duty	X0	30	—	70	%	crystal & ceramic
Input clock rising/falling time	t_{CR} t_{CF}	X0	—	—	10	ns	Applied when external clock used

* : duty = P_{WH}/t_{HCYL}

• Timing Conditions



• Clock Configurations



(4) Instruction Cycle

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Value	Unit	Remarks
Instruction cycle (Minimum instruction executing time)	t_{inst}	4/F_C to 64/F_C	µs	t_{inst} = 0.8 µs when operating at F_C = 5 MHz

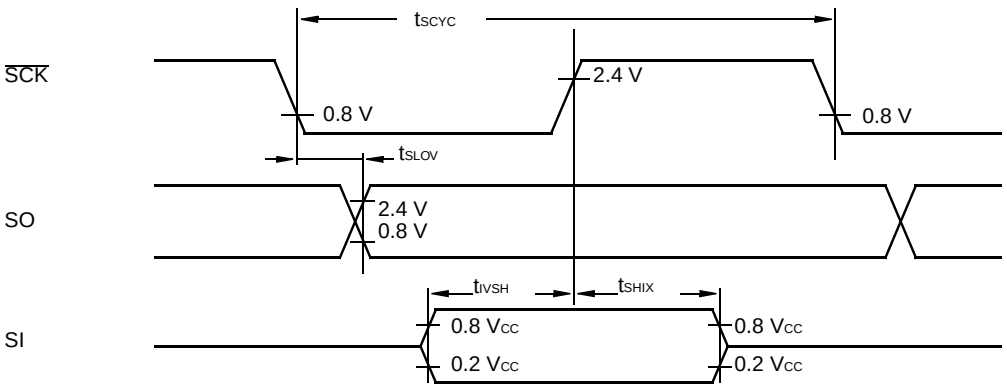
(5) Serial I/O & UART timing

(V_{CC} = 5.0 V ±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

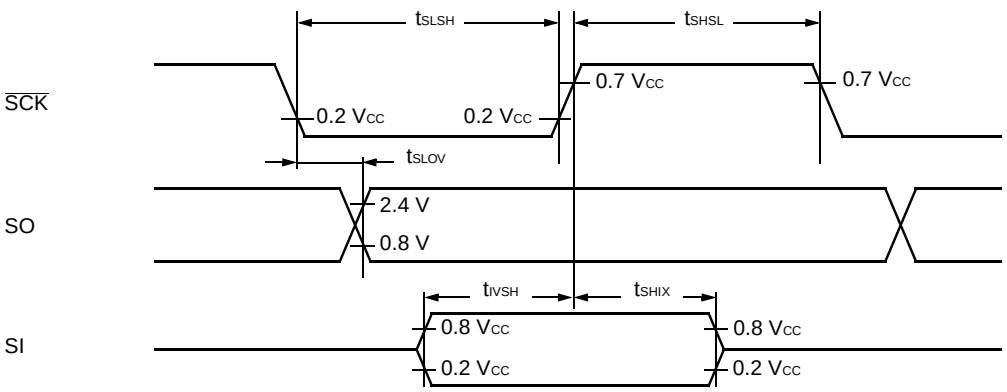
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation	2 t_{inst}*	—	µs	
SCK1 ↓ → SO time	t_{SLOV}	SCK, SO		200	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		0.5 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		0.5 t_{inst}*	—	µs	
Serial clock “H” pulse width	t_{SHSL}	SCK	External clock operation	1 t_{inst}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}	SCK		1 t_{inst}	—	µs	
SCK1 ↓ → SO time	t_{SLOV}	SCK, SO		0	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		0.5 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		0.5 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

• **Internal Shift Clock Mode**



• **External Shift Clock Mode**

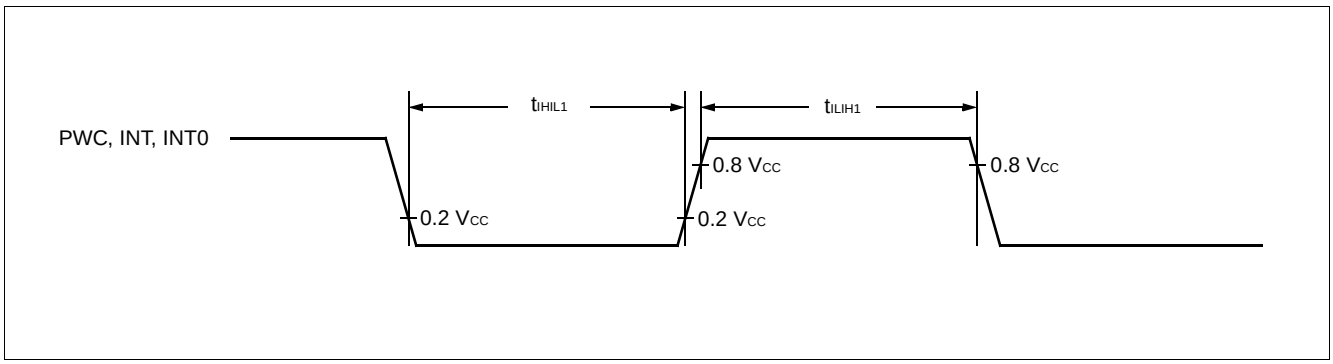


(6) Peripheral Input Timing

(V_{CC} = 5.0 V ±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min.	Max.		
Peripheral input “H” level pulse width 1	t_{ILIH1}	PWC, INT1, INT0	2 t_{inst}*	—	µs	
Peripheral input “L” level pulse width 1	t_{IHIL1}	PWC, INT1, INT0	2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”



■ INSTRUCTIONS (136 INSTRUCTIONS)

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)

(Continued)

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Symbol	Meaning
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: The number of instructions

#: The number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- "–" indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH prior to the instruction executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:

Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Notes: • During byte transfer to A, T ← A is restricted to low bytes.
• Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1	→ C → A	–	–	–	+ + – +	03
ROLC A	2	1	C ← A ←	–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

■ INSTRUCTION MAP

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR A,@IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

MB89950 Series

■ MASK OPTIONS

No.	Model	MB89951 MB89953	MB89P955	MB89PV950
	Specification method	**Select when ordering mask**	**Set by EPROM**	**Fixed**
1	Pull-up resistors P40 to P46	Can be selected for each pin	Can be selected for each pin	No pull-up resistor
2	Port/segment output P00 to P07, P10 to P17, P20 to P25	Can be selected for every 8 to 1 pins*2	Port/segment output*3	Port/segment output*3
3	Power-on reset Power-on reset available Power-on reset unavailable	Selectable	Selectable	Power-on reset available
4	Selection of main clock oscillation stabilization time (at 5 MHz)*1 Approx. $2^{18}/F_C$ (Approx. 52.4 ms) Approx. $2^{14}/F_C$ (Approx. 3.28 ms)	Selectable	Selectable	$2^{18}/F_C$
5	Reset pin output Reset output available Reset output unavailable	Selectable	Selectable	Reset output available

*1: The main clock oscillation stabilization time is generated by dividing the main clock oscillation. Since the oscillation cycle is unstable immedeately after oscillation starts, the time in this table is only a guide.

*2: Port/segment output switching should be specified in the same manner as the port allocation set by the segment output select register in the LCD controller/driver.

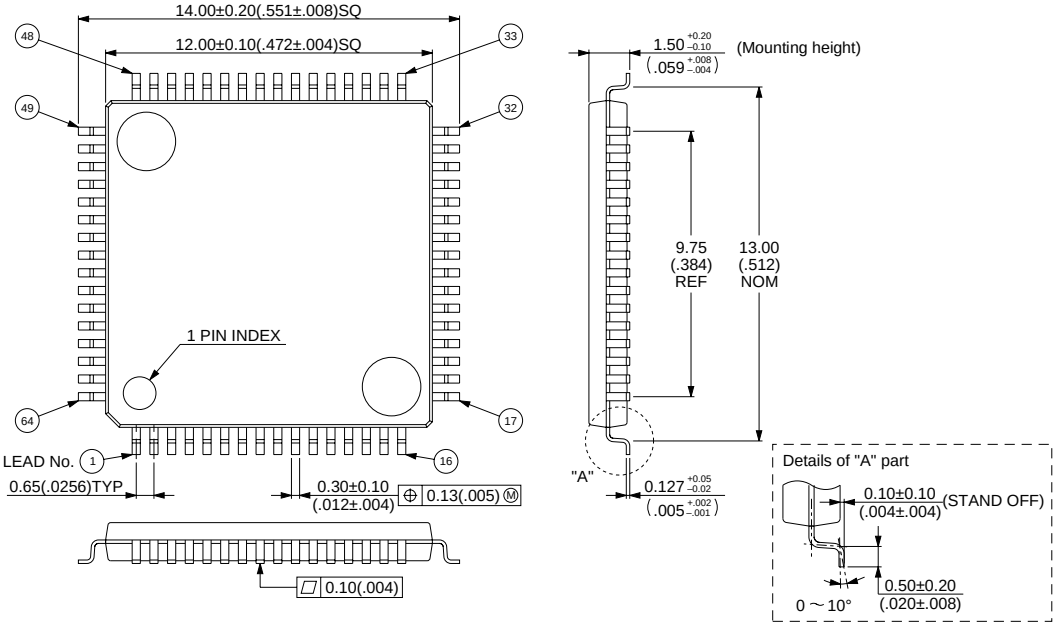
*3: When those pins are used as ports, applied voltage should never be jogjer than V3.

■ ORDERING INFORMATION

Part Number	Package	Remarks
MB89951PFM MB89953PFM MB89951PFM	64-pin Plastic QFP (FPT-64P-M09)	
MB89PV950CF	64-pin Ceramic MQFP (MQP-64C-M01)	

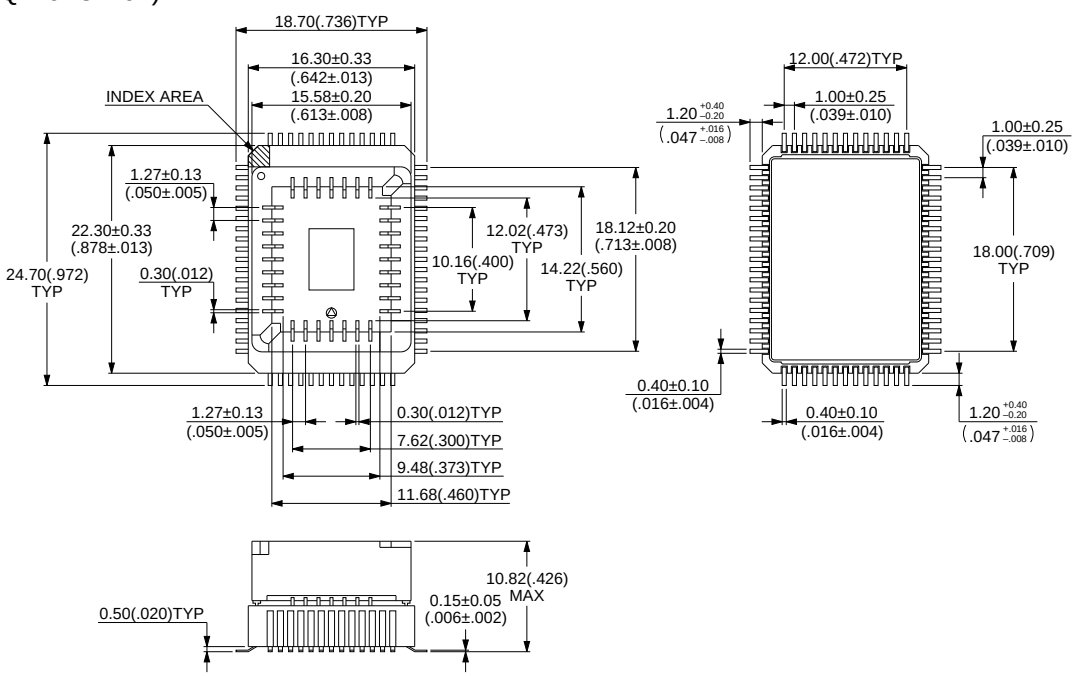
■ PACKAGE DIMENSIONS

64-pin Plastic QFP
(FPT-64P-M09)



Dimensions in mm (inches)

64-pin Ceramic MQFP
(MQP-64C-P01)



Dimensions in mm (inches)

MB89950 Series

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