3.3V 64K/128K/256K x 36 and 128K/256K x 18 Synchronous Dual-Port RAM

Features (all)

- **True dual-ported memory cells that allow simultaneous access of the same memory location**
- **Synchronous pipelined**
- **Organization of 2M, 4.5M, and 9M devices**
  - **256K × 36 (CY7C0853V)**
  - **128K × 36 (CY7C0852V)**
  - **64K × 36 (CY7C0851V)**
  - **256K × 18 (CY7C0832V)**
  - **128K × 18 (CY7C0831V)**
- **Pipelined output mode allows fast 150-MHz operation**
- **0.18-micron CMOS for optimum speed and power**
- **High-speed clock to data access: 4.0 ns (max.)**
- **3.3V low operating power**
  - **Active = 300 mA (typical)**
  - **Standby = 10 mA (typical)**
- **Interrupt flags for message passing**
- **Global master reset**
- **Separate byte enables on both ports**
- **Commercial and industrial temperature ranges**
- **IEEE 1149.1-compatible JTAG boundary scan**
- **172-ball BGA (1 mm pitch) (15 mm × 15 mm)**
- **120-pin TQFP (14 mm × 14 mm × 1.4 mm)**
- **176-pin TQFP (24 mm × 24 mm × 1.4 mm)**
- **FLEx36™ devices are pin footprint upgradeable from 2M to 4M to 9M**

Features (all except CY7C0853V)

- **Counter wrap around control**
  - **Internal mask register controls counter wrap-around**
  - **Counter-interrupt flags to indicate wrap-around**
  - **Memory block retransmit operation**
- **Counter readback on address lines**
- **Mask register readback on address lines**
- **Dual Chip Enables on both ports for easy depth expansion**

Functional Description (all)

The CY7C085XV/CY7C083XV are 2M, 4.5M, and 9M pipelined, synchronous, true dual-port static RAMs that are high-speed, low-power 3.3V CMOS. Two ports are provided, permitting independent, simultaneous access for Reads from any location in memory. A particular port can write to a certain location while another port is reading that location. The result of writing to the same location by more than one port at the same time is undefined. Registers on control, address, and data lines allow for minimal set-up and hold time.

Functional Description (all except CY7C0853V)

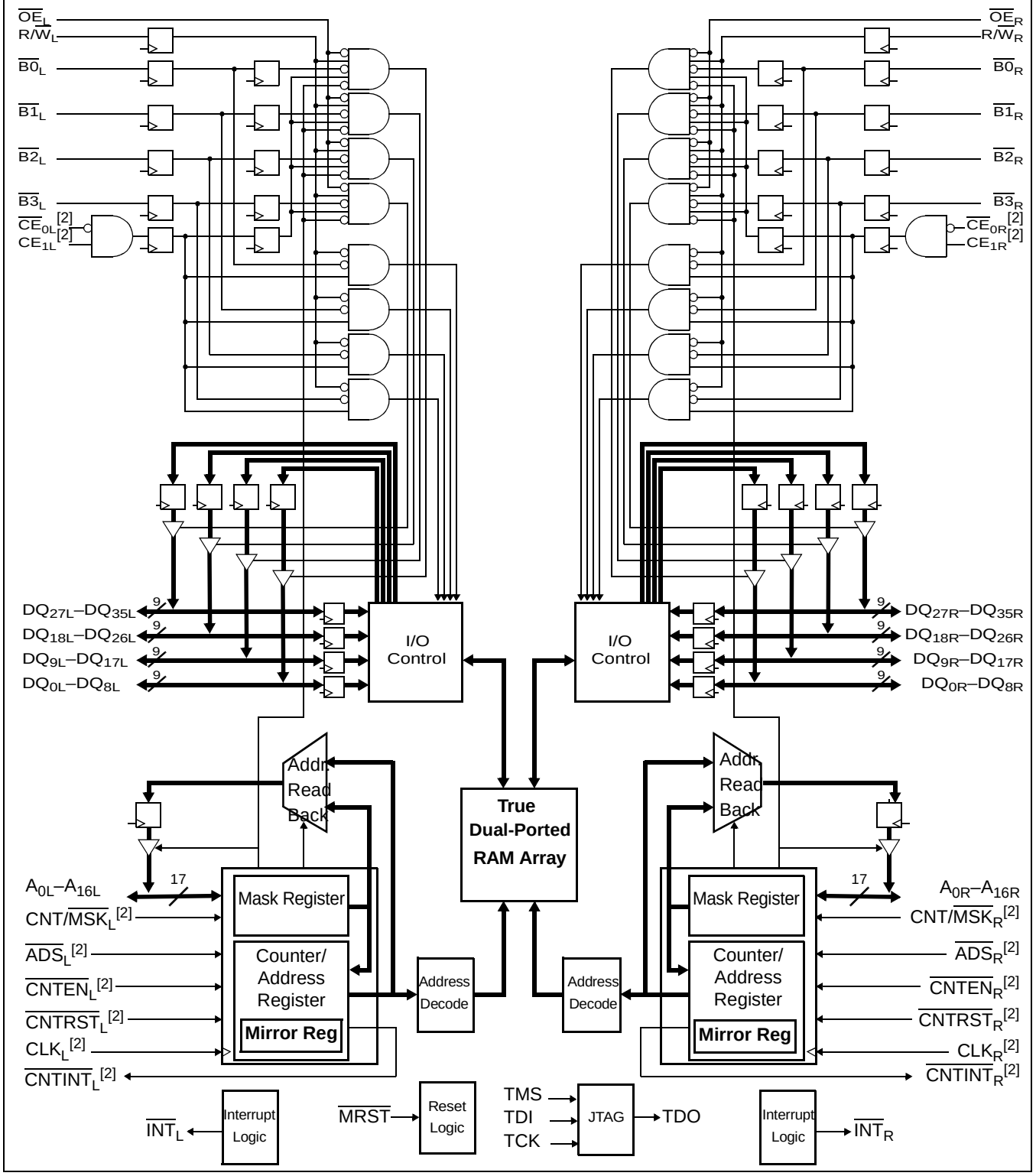
During a Read operation, data is registered for decreased cycle time. Clock to data valid t_{CD2} = 4.0 ns at 150 MHz. Each port contains a burst counter on the input address register. After externally loading the counter with the initial address, the counter will increment the address internally (more details to follow). The internal Write pulse width is independent of the duration of the R/$\overline{W}$ input signal. The internal Write pulse is self-timed to allow the shortest possible cycle times.

A HIGH on $\overline{CE0}$ or LOW on CE1 for one clock cycle will power down the internal circuitry to reduce the static power consumption. One cycle with chip enables asserted is required to reactivate the outputs.

Counter enable (CNTEN) inputs are provided to stall the operation of the address input and utilize the internal address generated by the internal counter for fast, interleaved memory applications. A port's burst counter is loaded when the port's address strobe ($\overline{ADS}$) and $\overline{CNTEN}$ signals are LOW. When the port's $\overline{CNTEN}$ is asserted and the $\overline{ADS}$ is deasserted, the address counter will increment on each LOW to HIGH transition of that port's clock signal. This will Read/Write one word from/into each successive address location until $\overline{CNTEN}$ is deasserted. The counter can address the entire memory array, and will loop back to the start. Counter reset ($\overline{CNTRST}$) is used to reset the unmasked portion of the burst counter to 0s. A counter-mask register is used to control the counter wrap. The counter and mask register operations are described in more detail in the following sections.

New features added to the CY7C08X1V/CY7C08X2V devices include: readback of burst-counter internal address value on address lines, counter-mask registers to control the counter wrap-around, counter interrupt ($\overline{CNTINT}$) flags, readback of mask register value on address lines, retransmit functionality, interrupt flags for message passing, JTAG for boundary scan, and asynchronous Master Reset (MRST).

Logic Block Diagram[1]



Notes:

1. CY7C0851V has 16 address bits instead of 17. CY7C0832V and CY7C0853V have 18 address bits instead of 17. CY7C083XV does not have $\overline{B2}$ and $\overline{B3}$ inputs. CY7C083XV does not have DQ18–DQ35 data bits. JTAG not implemented on CY7C083XV.
2. This feature is not available on the CY7C0853V.

Pin Configurations

172-ball BGA
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	DQ32L	DQ30L	$\overline{\text{CNTINTL}}$	VSSQ	DQ13L	VDDQ	DQ11L	DQ11R	VDDQ	DQ13R	VSSQ	$\overline{\text{CNTINTR}}$	DQ30R	DQ32R
B	A0L	DQ33L	DQ29L	DQ17L	DQ14L	DQ12L	DQ9L	DQ9R	DQ12R	DQ14R	DQ17R	DQ29R	DQ33R	A0R
C	NC	A1L	DQ31L	DQ27L	$\overline{\text{INTL}}$	DQ15L	DQ10L	DQ10R	DQ15R	$\overline{\text{INTR}}$	DQ27R	DQ31R	A1R	NC
D	A2L	A3L	DQ35L	DQ34L	DQ28L	DQ16L	VSSQ	VSSQ	DQ16R	DQ28R	DQ34R	DQ35R	A3R	A2R
E	A4L	A5L	CE1L	$\overline{\text{B0L}}$	VDDQ	VSSA			VDDA	VDDQ	$\overline{\text{B0R}}$	CE1R	A5R	A4R
F	VDD	A6L	A7L	$\overline{\text{B1L}}$	VDDA					VSSA	$\overline{\text{B1R}}$	A7R	A6R	VDD
G	$\overline{\text{OEL}}$	$\overline{\text{B2L}}$	$\overline{\text{B3L}}$	$\overline{\text{CE0L}}$			CY7C0851V CY7C0852V				$\overline{\text{CE0R}}$	$\overline{\text{B3R}}$	$\overline{\text{B2R}}$	$\overline{\text{OER}}$
H	VSS	R/$\overline{\text{WL}}$	A8L	CLKL							CLKR	A8R	R/$\overline{\text{WR}}$	VSS
J	A9L	A10L	VSS	$\overline{\text{ADSL}}$	VSSA					VDDA	$\overline{\text{ADSR}}$	$\overline{\text{MRST}}$	A10R	A9R
K	A11L	A12L	A15L	$\overline{\text{CNTRSTL}}$	VDDQ	VDDA			VSSA	VDDQ	$\overline{\text{CNTRSTR}}$	A15R	A12R	A11R
L	CNT/$\overline{\text{MSKL}}$	A13L	$\overline{\text{CNTENL}}$	DQ26L	DQ25L	DQ19L	VSSQ	VSSQ	DQ19R	DQ25R	DQ26R	$\overline{\text{CNTENR}}$	A13R	CNT/$\overline{\text{MSKR}}$
M	A16L[3]	A14L	DQ22L	DQ18L	TDI	DQ7L	DQ2L	DQ2R	DQ7R	TCK	DQ18R	DQ22R	A14R	A16R[3]
N	DQ24L	DQ20L	DQ8L	DQ6L	DQ5L	DQ3L	DQ0L	DQ0R	DQ3R	DQ5R	DQ6R	DQ8R	DQ20R	DQ24R
P	DQ23L	DQ21L	TDO	VSSQ	DQ4L	VDDQ	DQ1L	DQ1R	VDDQ	DQ4R	VSSQ	TMS	DQ21R	DQ23R

Note:
3. For CY7C0851V, pins M1 and M14 are NC.

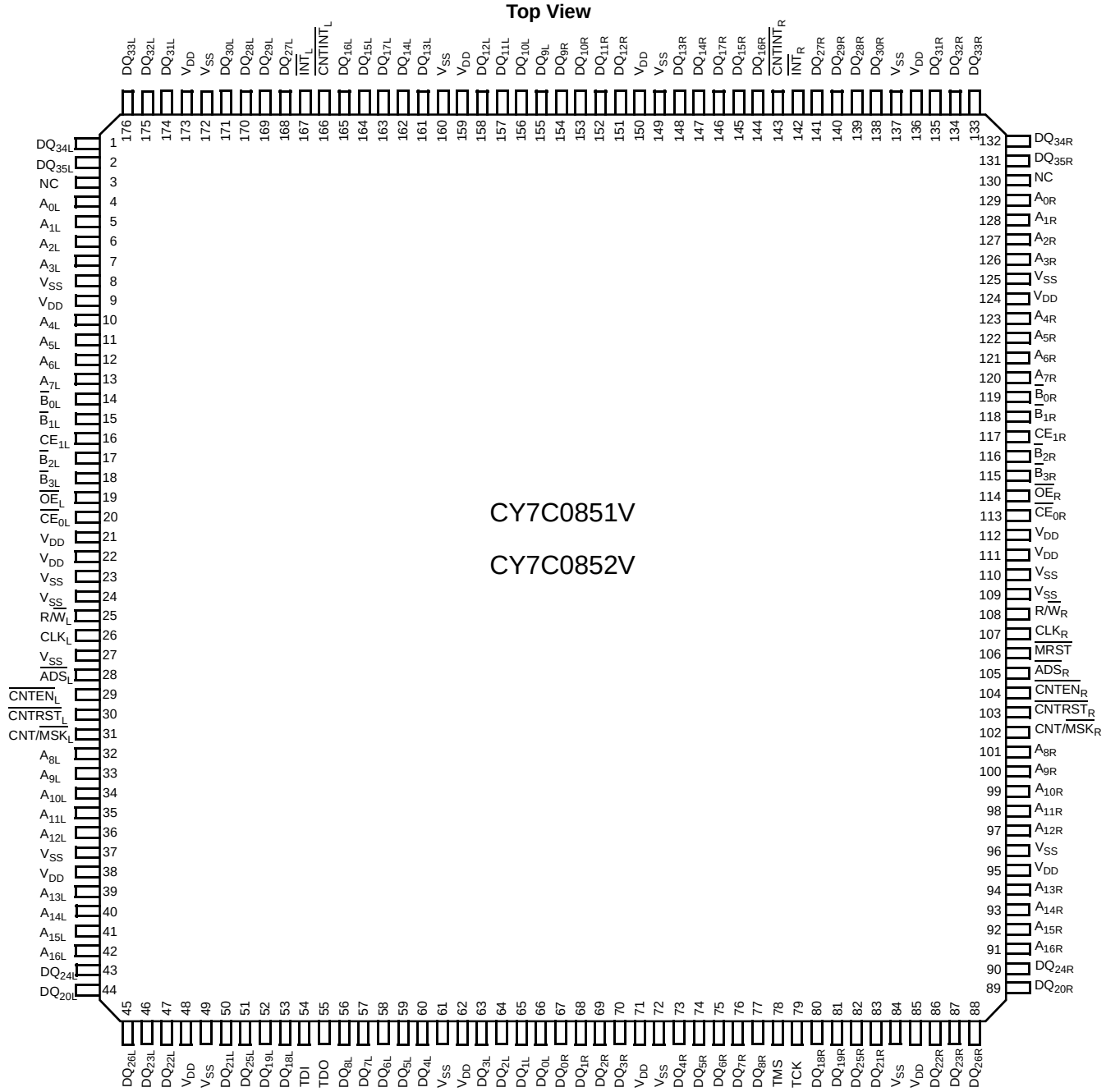
Pin Configurations (continued)

172-ball BGA
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	DQ32L	DQ30L	$\overline{NC}$	VSSQ	DQ13L	VDDQ	DQ11L	DQ11R	VDDQ	DQ13R	VSSQ	$\overline{NC}$	DQ30R	DQ32R
B	A0L	DQ33L	DQ29L	DQ17L	DQ14L	DQ12L	DQ9L	DQ9R	DQ12R	DQ14R	DQ17R	DQ29R	DQ33R	A0R
C	A17L	A1L	DQ31L	DQ27L	$\overline{INTL}$	DQ15L	DQ10L	DQ10R	DQ15R	$\overline{INTR}$	DQ27R	DQ31R	A1R	A17R
D	A2L	A3L	DQ35L	DQ34L	DQ28L	DQ16L	VSSQ	VSSQ	DQ16R	DQ28R	DQ34R	DQ35R	A3R	A2R
E	A4L	A5L	VDD	$\overline{B0L}$	VDDQ	VSSA			VDDA	VDDQ	$\overline{B0R}$	VDD	A5R	A4R
F	VDD	A6L	A7L	$\overline{B1L}$	VDDA					VSSA	$\overline{B1R}$	A7R	A6R	VDD
G	$\overline{OEL}$	$\overline{B2L}$	$\overline{B3L}$	VSS			CY7C0853V				VSS	$\overline{B3R}$	$\overline{B2R}$	$\overline{OER}$
H	VSS	R/$\overline{WL}$	A8L	CLKL							CLKR	A8R	R/$\overline{WR}$	VSS
J	A9L	A10L	VSS	VSS	VSSA					VDDA	VSS	$\overline{MRST}$	A10R	A9R
K	A11L	A12L	A15L	VDD	VDDQ	VDDA			VSSA	VDDQ	VDD	A15R	A12R	A11R
L	VDD	A13L	VSS	DQ26L	DQ25L	DQ19L	VSSQ	VSSQ	DQ19R	DQ25R	DQ26R	VSS	A13R	VDD
M	A16L	A14L	DQ22L	DQ18L	TDI	DQ7L	DQ2L	DQ2R	DQ7R	TCK	DQ18R	DQ22R	A14R	A16R
N	DQ24L	DQ20L	DQ8L	DQ6L	DQ5L	DQ3L	DQ0L	DQ0R	DQ3R	DQ5R	DQ6R	DQ8R	DQ20R	DQ24R
P	DQ23L	DQ21L	TDO	VSSQ	DQ4L	VDDQ	DQ1L	DQ1R	VDDQ	DQ4R	VSSQ	TMS	DQ21R	DQ23R

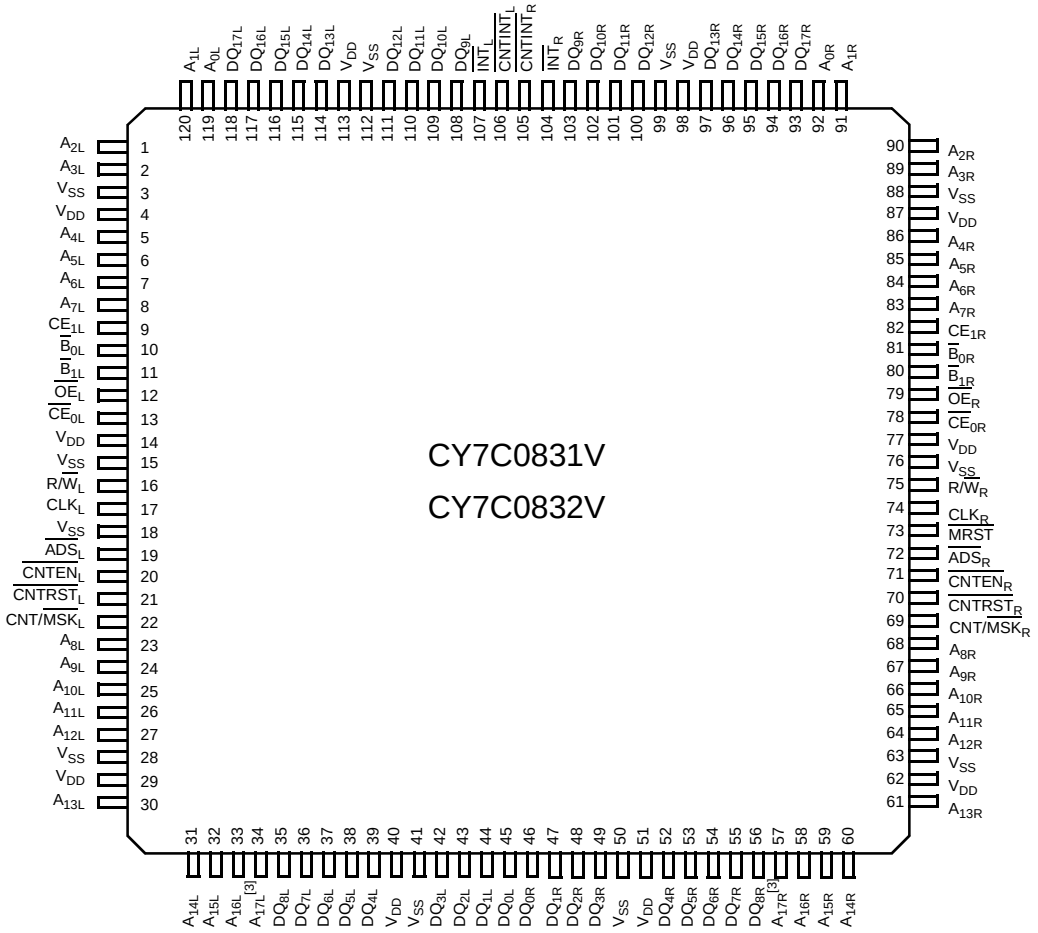
Pin Configurations (continued)

176-pin Thin Quad Flat Pack (TQFP)
Top View



Pin Configurations (continued)

120-pin Thin Quad Flat Pack (TQFP)[4]
Top View



Selection Guide

	CY7C0853V CY7C0851V CY7C0852V CY7C0853V[6] -150	CY7C0853V CY7C0851V CY7C0852V CY7C0853V -133	CY7C0853V CY7C0851V CY7C0852V CY7C0853V -100	Unit
f_{MAX}	150	133	100	MHz
Max. Access Time (Clock to Data)	4.0	4.4	5	ns
Typical Operating Current I_{CC}	300	270	200	mA
Typical Standby Current for I_{SB3} (Both Ports CMOS Level)[5]	10	10	10	mA

Notes:
4. NC for CY7C0831V.
5. Not applicable for CY7C0853V.
6. For CY7C0853V all 150 MHz values are advance information.

Pin Definitions

Left Port	Right Port	Description
A_{0L}–A_{16L}[1]	A_{0R}–A_{16R}[1]	***Address Inputs***.
$\overline{ADS}_L$	$\overline{ADS}_R$	***Address Strobe Input***. Used as an address qualifier. This signal should be asserted LOW for the part using the externally supplied address on the address pins and for loading this address into the burst address counter.
$\overline{CE0}_L$	$\overline{CE0}_R$	***Active LOW Chip Enable Input***.[2]
$CE1_L$	$CE1_R$	***Active HIGH Chip Enable Input***.[2]
CLK_L	CLK_R	***Clock Signal***. Maximum clock input rate is f_{MAX}.
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	***Counter Enable Input***.[2] Asserting this signal LOW increments the burst address counter of its respective port on each rising edge of CLK. The increment is disabled if $\overline{ADS}$ or $\overline{CNTRST}$ are asserted LOW.
$\overline{CNTRST}_L$	$\overline{CNTRST}_R$	***Counter Reset Input***.[2] Asserting this signal LOW resets to zero the unmasked portion of the burst address counter of its respective port. $\overline{CNTRST}$ is not disabled by asserting $\overline{ADS}$ or $\overline{CNTEN}$.
CNT/$\overline{MSK}_L$	CNT/$\overline{MSK}_R$	***Address Counter Mask Register Enable Input***.[2] Asserting this signal LOW enables access to the mask register. When tied HIGH, the mask register is not accessible and the address counter operations are enabled based on the status of the counter control signals.
DQ_{0L}–DQ_{35L}[1]	DQ_{0R}–DQ_{35R}[1]	***Data Bus Input/Output***.
$\overline{OE}_L$	$\overline{OE}_R$	***Output Enable Input***. This asynchronous signal must be asserted LOW to enable the DQ data pins during Read operations.
$\overline{INT}_L$	$\overline{INT}_R$	***Mailbox Interrupt Flag Output***. The mailbox permits communications between ports. The upper two memory locations can be used for message passing. $\overline{INT}_L$ is asserted LOW when the right port writes to the mailbox location of the left port, and vice versa. An interrupt to a port is deasserted HIGH when it reads the contents of its mailbox.
$\overline{CNTINT}_L$	$\overline{CNTINT}_R$	***Counter Interrupt Output***.[2] This pin is asserted LOW when the unmasked portion of the counter is incremented to all “1s.”
R/$\overline{W}_L$	R/$\overline{W}_R$	***Read/Write Enable Input***. Assert this pin LOW to write to, or HIGH to Read from the dual port memory array.
$\overline{B}_{0L}$–$\overline{B}_{3L}$	$\overline{B}_{0R}$–$\overline{B}_{3R}$	***Byte Select Inputs***. Asserting these signals enables Read and Write operations to the corresponding bytes of the memory array.
$\overline{MRST}$		***Master Reset Input***. $\overline{MRST}$ is an asynchronous input signal and affects both ports. Asserting $\overline{MRST}$ LOW performs all of the reset functions as described in the text. A $\overline{MRST}$ operation is required at power-up.
TMS		***JTAG Test Mode Select Input***. It controls the advance of JTAG TAP state machine. State machine transitions occur on the rising edge of TCK.
TDI		***JTAG Test Data Input***. Data on the TDI input will be shifted serially into selected registers.
TCK		***JTAG Test Clock Input***.
TDO		***JTAG Test Data Output***. TDO transitions occur on the falling edge of TCK. TDO is normally three-stated except when captured data is shifted out of the JTAG TAP.
V_{SS}		***Ground Inputs***.
V_{DD}		***Power Inputs***.

Master Reset

The CY7C0831V undergoes a complete reset by taking its $\overline{MRST}$ input LOW. The MRST input can switch asynchronously to the clocks. An MRST initializes the internal burst counters to zero, and the counter mask registers to all ones (completely unmasked). MRST also forces the Mailbox Interrupt ($\overline{INT}$) flags and the Counter Interrupt ($\overline{CNTINT}$) flags HIGH. MRST must be performed on the CY7C0831V after power-up.

Mailbox Interrupts

The upper two memory locations may be used for message passing and permit communications between ports. *Table 2* shows the interrupt operation for both ports. The highest memory location, 1FFFF is the mailbox for the right port and 1FFFE is the mailbox for the left port. *Table 2* shows that in order to set the $\overline{INT}_R$ flag, a Write operation by the left port to address 1FFFF will assert $\overline{INT}_R$ LOW. At least one byte has to be active for a Write to generate an interrupt. A valid Read of the 1FFFF location by the right port will reset $\overline{INT}_R$ HIGH. At least one byte has to be active in order for a Read to reset the interrupt. When one port Writes to the other port's mailbox, the $\overline{INT}$ of the port that the mailbox belongs to is asserted LOW. The $\overline{INT}$ is reset when the owner (port) of the mailbox Reads the contents of the mailbox. The interrupt flag is set in a flow-thru mode (i.e., it follows the clock edge of the writing port). Also, the flag is reset in a flow-thru mode (i.e., it follows the clock edge of the reading port).

Each port can read the other port's mailbox without resetting the interrupt. And each port can write to its own mailbox without setting the interrupt. If an application does not require message passing, $\overline{INT}$ pins should be left open.

Table 1. Address Counter and Counter-Mask Register Control Operation (Any Port)[2, 7, 8]

CLK	$\overline{MRST}$	CNT/$\overline{MSK}$	$\overline{CNTRST}$	$\overline{ADS}$	$\overline{CNTEN}$	Operation	Description
X	L	X	X	X	X	Master Reset	Reset address counter to all 0s and mask register to all 1s.
⎍	H	H	L	X	X	Counter Reset	Reset counter unmasked portion to all 0s.
⎍	H	H	H	L	L	Counter Load	Load counter with external address value presented on address lines.
⎍	H	H	H	L	H	Counter Readback	Read out counter internal value on address lines.
⎍	H	H	H	H	L	Counter Increment	Internally increment address counter value.
⎍	H	H	H	H	H	Counter Hold	Constantly hold the address value for multiple clock cycles.
⎍	H	L	L	X	X	Mask Reset	Reset mask register to all 1s.
⎍	H	L	H	L	L	Mask Load	Load mask register with value presented on the address lines.
⎍	H	L	H	L	H	Mask Readback	Read out mask register value on address lines.
⎍	H	L	H	H	X	Reserved	Operation undefined

Table 2. Interrupt Operation Example [1, 9, 10, 11]

Function	Left Port				Right Port			
	$R/\overline{W}_L$	$\overline{CE}_L$	A_{0L-16L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	A_{0R-16R}	$\overline{INT}_R$
Set Right $\overline{INT}_R$ Flag	L	L	1FFFF	X	X	X	X	L
Reset Right $\overline{INT}_R$ Flag	X	X	X	X	H	L	1FFFF	H
Set Left $\overline{INT}_L$ Flag	X	X	X	L	L	L	1FFFE	X
Reset Left $\overline{INT}_L$ Flag	H	L	1FFFE	H	X	X	X	X

Notes:
7. "X" = "Don't Care," "H" = HIGH, "L" = LOW.
8. Counter operation and mask register operation is independent of chip enables.
9. $\overline{CE}$ is internal signal. $\overline{CE}$ = LOW if CE_0 = LOW and CE_1 = HIGH. For a single Read operation, CE only needs to be asserted once at the rising edge of the CLK and can be deasserted after that. Data will be out after the following CLK edge and will be three-stated after the next CLK edge.
10. $\overline{OE}$ is "Don't Care" for mailbox operation.
11. At least one of B0, B1, B2, or B3 must be LOW.

Address Counter and Mask Register Operations [2, 12]

Each port of the CY7C085XV/CY7C083XV has a programmable burst address counter. The burst counter contains three 17-bit registers: a counter register, a mask register, and a mirror register.

The **counter register** contains the address used to access the RAM array. It is changed only by the Counter Load, Increment, Counter Reset, and by master reset (MRST) operations.

The **mask register** value affects the Increment and Counter Reset operations by preventing the corresponding bits of the counter register from changing. It also affects the counter interrupt output (CNTINT). The mask register is changed only by the Mask Load and Mask Reset operations, and by the MRST. The mask register defines the counting range of the counter register. It divides the counter register into two regions: zero or more "0s" in the most significant bits define the masked region, one or more "1s" in the least significant bits define the unmasked region. Bit 0 may also be "0," masking the least significant counter bit and causing the counter to increment by two instead of one.

The mirror register is used to reload the counter register on increment operations (see "retransmit," below). It always contains the value last loaded into the counter register, and is changed only by the Counter Load, and Counter Reset operations, and by the MRST.

Table 1 summarizes the operation of these registers and the required input control signals. The MRST control signal is asynchronous. All the other control signals in *Table 1* (CNT/MSK, CNTRST, ADS, CNTEN) are synchronized to the port's CLK. All these counter and mask operations are independent of the port's chip enable inputs (CE0 and CE1).

Counter Load Operation

The address counter and mirror registers are both loaded with the address value presented at the address lines. This value ranges from 0 to 1FFFF.

Mask Load Operation

The mask register is loaded with the address value presented at the address lines. This value ranges from 0 to 1FFFF, although not all values permit correct increment operations. Permitted values are of the form $2^n - 1$ or $2^n - 2$. From the most significant bit to the least significant bit, permitted values have zero or more "0s," one or more "1s," or one "0." Thus 1FFFF, 003FE, and 00001 are permitted values, but 1F0FF, 003FC, and 00000 are not.

Counter Readback Operation

The internal value of the counter register can be read out on the address lines. Readback is pipelined; the address will be valid t_{CA2} after the next rising edge of the port's clock. If address readback occurs while the port is enabled (CE0 LOW and CE1 HIGH), the data lines (DQs) will be three-stated. *Figure 1* shows a block diagram of the operation.

Mask Readback Operation

The internal value of the mask register can be read out on the address lines. Readback is pipelined; the address will be valid t_{CM2} after the next rising edge of the port's clock. If mask readback occurs while the port is enabled (CE0 LOW and CE1 HIGH), the data lines (DQs) will be three-stated. *Figure 1* shows a block diagram of the operation.

Mask Reset Operation

The mask register is reset to all "1s," which unmasks every bit of the counter. Master reset (MRST) also resets the mask register to all "1s."

Counter Reset Operation

All unmasked bits of the counter and mirror registers are reset to "0." All masked bits remain unchanged. A Mask Reset followed by a Counter Reset will reset the counter and mirror registers to 00000, as will master reset (MRST).

Increment Operation

Once the address counter register is initially loaded with an external address, the counter can internally increment the address value, potentially addressing the entire memory array. Only the unmasked bits of the counter register are incremented. The corresponding bit in the mask register must be a "1" for a counter bit to change. The counter register is incremented by 1 if the least significant bit is unmasked, and by 2 if it is masked. If all unmasked bits are "1," the next increment will wrap the counter back to the initially loaded value. If an Increment results in all the unmasked bits of the counter being "1s," a counter interrupt flag (CNTINT) is asserted. The next Increment will return the counter register to its initial value, which was stored in the mirror register. The counter address can instead be forced to loop to 00000 by externally connecting CNTINT to CNTRST.[13] An increment that results in one or more of the unmasked bits of the counter being "0" will de-assert the counter interrupt flag. The example in *Figure 2* shows the counter mask register loaded with a mask value of 0003Fh unmasking the first 6 bits with bit "0" as the LSB and bit "16" as the MSB. The maximum value the mask register can be loaded with is 1FFFFh. Setting the mask register to this value allows the counter to access the entire memory space. The address counter is then loaded with an initial value of 8h. The base address bits (in this case, the 6th address through the 16th address) are loaded with an address value but do not increment once the counter is configured for increment operation. The counter address will start at address 8h. The counter will increment its internal address value till it reaches the mask register value of 3Fh. The counter wraps around the memory block to location 8h at the next count. CNTINT is issued when the counter reaches its maximum value.

Hold Operation

The value of all three registers can be constantly maintained unchanged for an unlimited number of clock cycles. Such operation is useful in applications where wait states are needed, or when address is available a few cycles ahead of data in a shared bus interface.

Notes:

12. This section describes the CY7C0852V and CY7C0831V, which have 17 address bits and a maximum address value of 1FFFF. The CY7C0832V has 18 address bits, register lengths of 18 bits, and a maximum address value of 3FFFF. The CY7C0851V has 16 address bits, register lengths of 16 bits, and a maximum address value of FFFF.
13. CNTINT and CNTRST specs are guaranteed by design to operate properly at speed grade operating frequency when tied together.

Counter Interrupt

The counter interrupt ($\overline{\text{CNTINT}}$) is asserted LOW when an increment operation results in the unmasked portion of the counter register being all “1s.” It is deasserted HIGH when an Increment operation results in any other value. It is also de-asserted by Counter Reset, Counter Load, Mask Reset and Mask Load operations, and by $\overline{\text{MRST}}$.

Retransmit

Retransmit is a feature that allows the Read of a block of memory more than once without the need to reload the initial address. This eliminates the need for external logic to store and route data. It also reduces the complexity of the system design and saves board space. An internal “mirror register” is used to store the initially loaded address counter value. When the counter unmasked portion reaches its maximum value set by the mask register, it wraps back to the initial value stored in this “mirror register.” If the counter is continuously configured in increment mode, it increments again to its maximum value and wraps back to the value initially stored into the “mirror register.” Thus, the repeated access of the same data is allowed without the need for any external logic.

Counting by Two

When the least significant bit of the mask register is “0,” the counter increments by two. This may be used to connect the CY7C0851V/CY7C0852V as a 72-bit single port SRAM in which the counter of one port counts even addresses and the counter of the other port counts odd addresses. This even-odd address scheme stores one half of the 72-bit data in even memory locations, and the other half in odd memory locations.

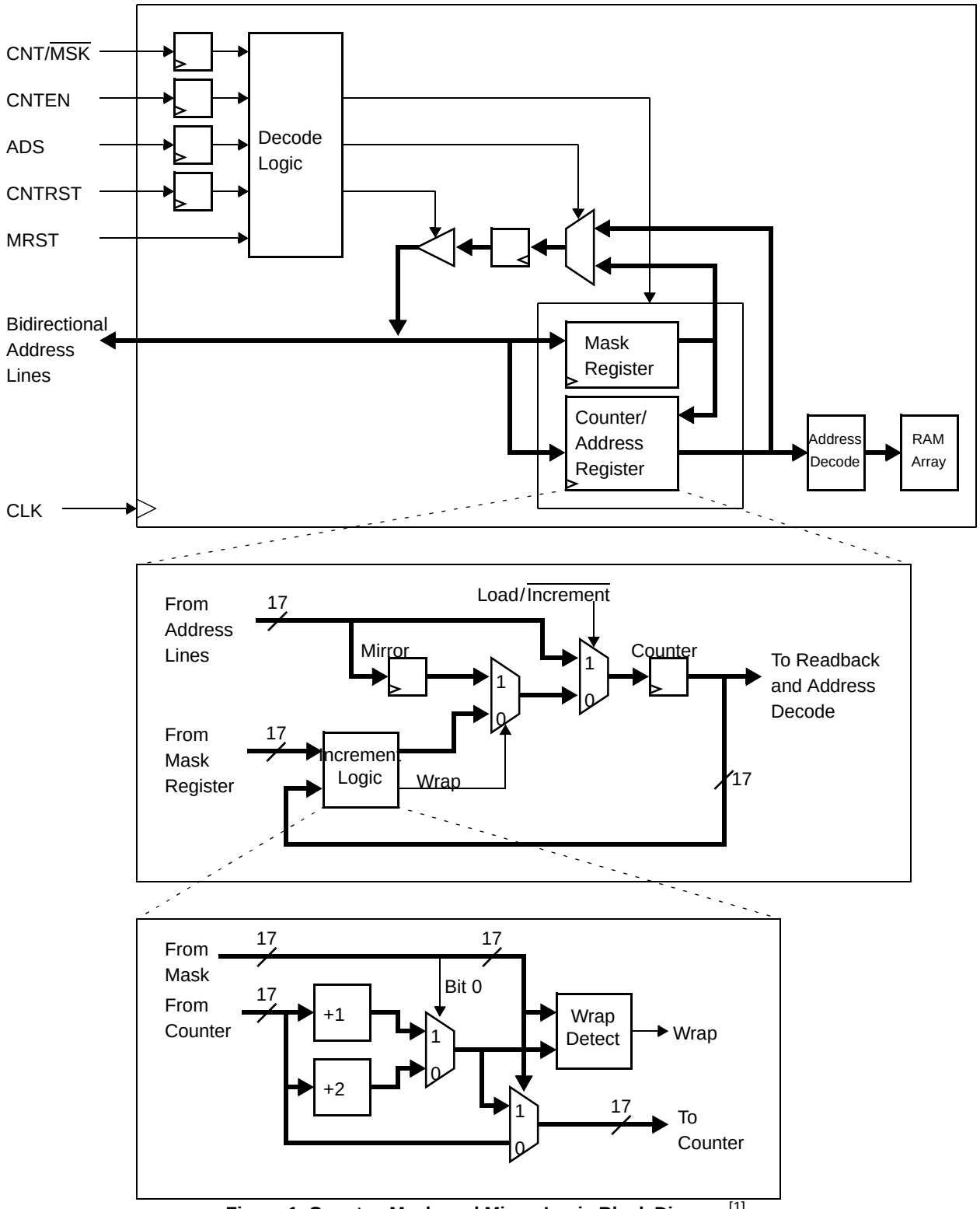


Figure 1. Counter, Mask, and Mirror Logic Block Diagram[1]

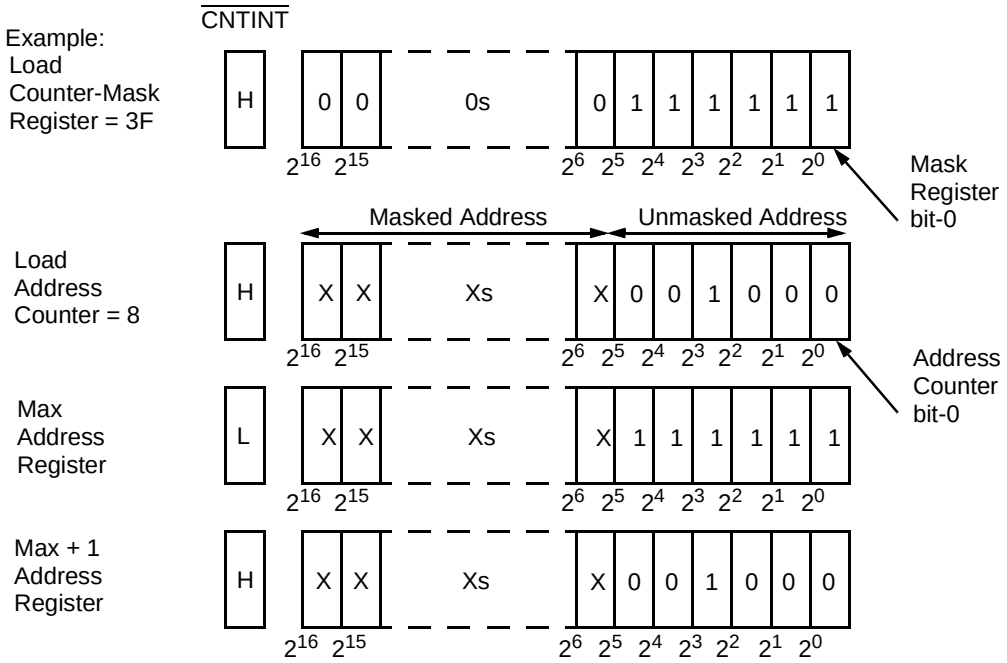


Figure 2. Programmable Counter-Mask Register Operation[1, 14]

IEEE 1149.1 Serial Boundary Scan (JTAG) [15]

The CY7C0851V/CY7C0852V/CY7C0853V incorporates an IEEE 1149.1 serial boundary scan test access port (TAP). The TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1-compliant TAPs. The TAP operates using JEDEC standard 3.3V I/O logic levels. It is composed of three input connections and one output connection required by the test logic defined by the standard.

Disabling the JTAG Feature

It is possible to operate the CY7C0851V/CY7C0852V/CY7C0853V without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternatively be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected.

Test Access Port–Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the MSB on any register.

Test Data Out (TDO)

The TDO output pin is used to serially clock data out from the registers. The output is active depending upon the current state of the TAP state machine (see TAP Controller State Diagram [FSM]). The output changes on the falling edge of TCK. TDO is connected to the LSB of any register.

Performing a TAP Reset

A reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This reset does not affect the operation of the CY7C0851V/CY7C0852V/CY7C0853V, and may be performed while the device is operating. An MRST must be performed on the CY7C0851V/CY7C0852V/CY7C0853V after power-up.

Performing a Pause/Restart

When a SHIFT-DR PAUSE-DR SHIFT-DR is performed the scan chain will output the next bit in the chain twice. For example, if the value expected from the chain is 1010101, the device will output a 11010101. This extra bit will cause some testers to report an erroneous failure for the CY7C0851/CY7C0852/CY7C0853 in a scan test. Therefore the tester should be configured to never enter the PAUSE-DR state.

Notes:
14. The “X” in this diagram represents the counter upper bits.
15. Boundary scan is IEEE 1149.1-compatible. See “Performing a Pause/Restart” for deviation from strict 1149.1 compliance.

TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the CY7C0851V/CY7C0852V/CY7C0853V test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register (IR)

Four-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in *Figure 4*, the JTAG/BIST Controller Block Diagram. On power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state, as described in the previous section.

When the TAP controller is in the CaptureIR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board level serial test path.

Bypass Register (BYR)

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain devices. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the CY7C0851V/CY7C0852V/CY7C0853V with minimal delay. The bypass register is set to “0” on the rising edge of TCK following entry into the Capture-DR state, if the current instruction causes the bypass register to be in the serial path between TDI and TDO.

Boundary Scan Register (BSR)

The boundary scan register is connected to all the input and output pins on the CY7C0851V/CY7C0852V/CY7C0853V, except the MRST pin. The boundary scan register is loaded with the contents of the CY7C0851V/CY7C0852V/CY7C0853V input and output ring when the TAP controller is in the Capture-DR state. It is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST and SAMPLE/PRELOAD instructions can be used to capture the contents of the input and output ring.

Identification Register (IDR)

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is in the instruction register. The IDCODE is hardwired into the CY7C0851V/CY7C0852V/CY7C0853V and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set

Sixteen different instructions are possible with the four-bit instruction register. All combinations are listed in *Table 5*. Other code combinations are listed as RESERVED and should not be used.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST allows circuitry external to the CY7C0851V/CY7C0852V/CY7C0853V package to be tested. Boundary-scan register cells at output pins are used to apply test stimuli, while those at input pins capture test results.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register on power-up or whenever the TAP controller is given a test logic reset state. The IDCODE value for the CY7C0851V is 0C001069h. The IDCODE value for the CY7C0852V is 0C002069h. The IDCODE value for the CY7C0853V is 0C002069h.

High-Z

The High-Z instruction causes the bypass register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all CY7C0851V/CY7C0852V/CY7C0853V outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions loaded into the instruction register and the TAP controller in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the CY7C0851V/CY7C0852V/CY7C0853V clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the CY7C0851V/CY7C0852V/CY7C0853V signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times. Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins. If the TAP controller goes into the Update-DR state, the sampled data will be updated.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected on a board.

CLAMP

The optional CLAMP instruction allows the state of the signals driven from CY7C0851V/CY7C0852V/CY7C0853V pins to be determined from the boundary-scan register while the BYPASS register is selected as the serial path between TDI and TDO. CLAMP controls boundary cells to 1 or 0.

NBSRST

This is the Non-Boundary Scan Reset instruction. NBSRST places the Bypass Register (BYR) between TDI and TDO when selected. Its function is to reset every logic (similar to $\overline{\text{MRST}}$) except that it does not reset the JTAG logic.

Boundary Scan Cells (BSC)

Every CY7C0851V/CY7C0852V/CY7C0853V output has two boundary scan cells; one for data, and one for three-state control. JTAG TAP pins (TDI, TMS, TDO, TCK), $\overline{\text{MRST}}$, and all power and ground pins have no scan cell. Other CY7C0851V/CY7C0852V/CY7C0853V inputs have only the data scan cell.

Active and Standby Supply Current[17]

When the instruction in the JTAG instruction register selects the Boundary Scan Register (BSR) and the TAP controller is in any state except TEST-LOGIC-RESET or RUN-TEST/IDLE, then the device supply current (ICC or ISB1/2/3/4) will increase. With the JTAG logic in this state, and both ports inactive with CMOS input levels, it is possible for the supply current to exceed the ISB3 value given in the Electrical Characteristics section of this datasheet.

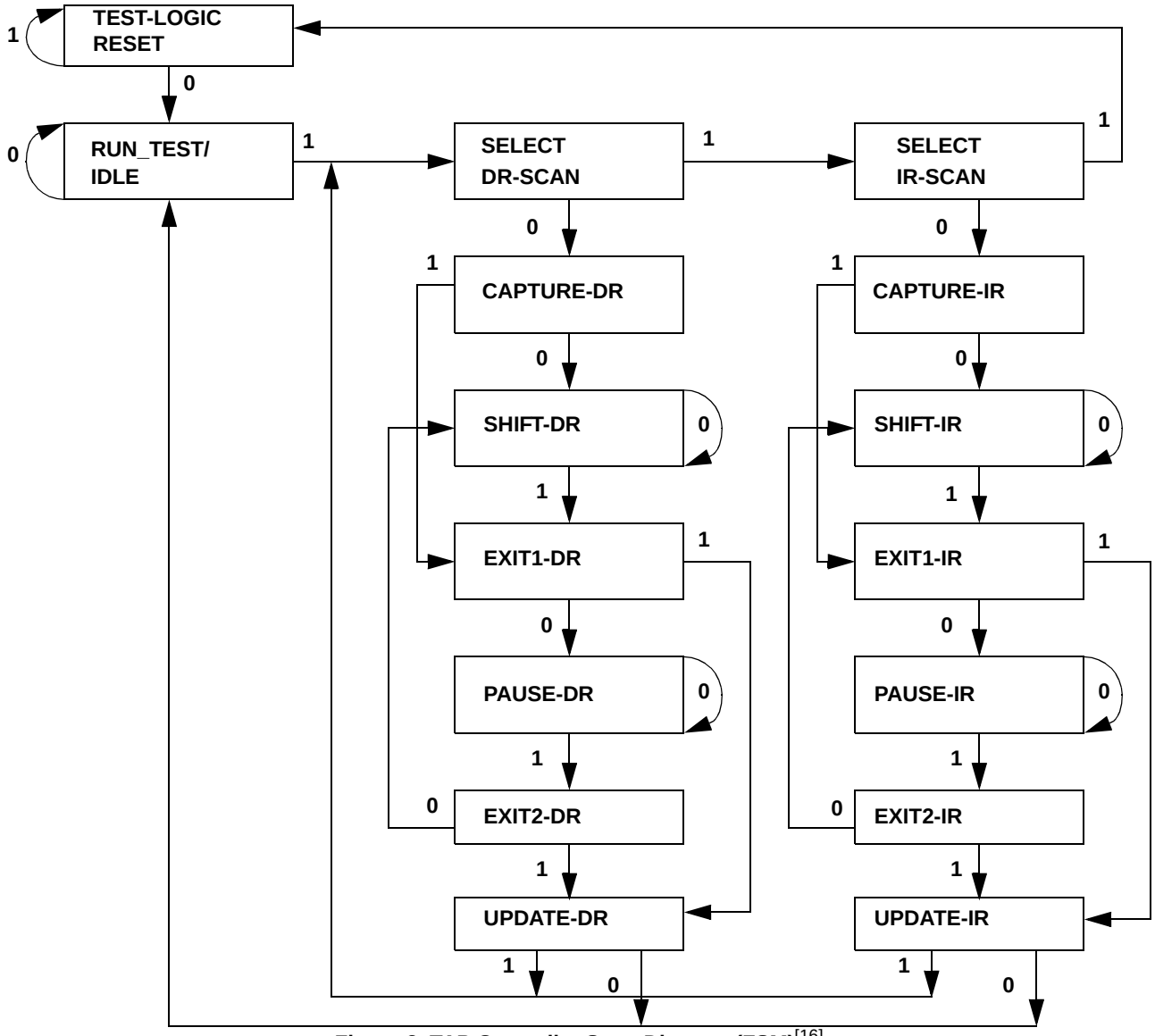


Figure 3. TAP Controller State Diagram (FSM)[16]

Notes:

16. The “0”/”1” next to each state represents the value at TMS at the rising edge of CLK.
17. I_{SB3} values only if JTAG pins are not active and mpdaster reset (MRST) not enabled.

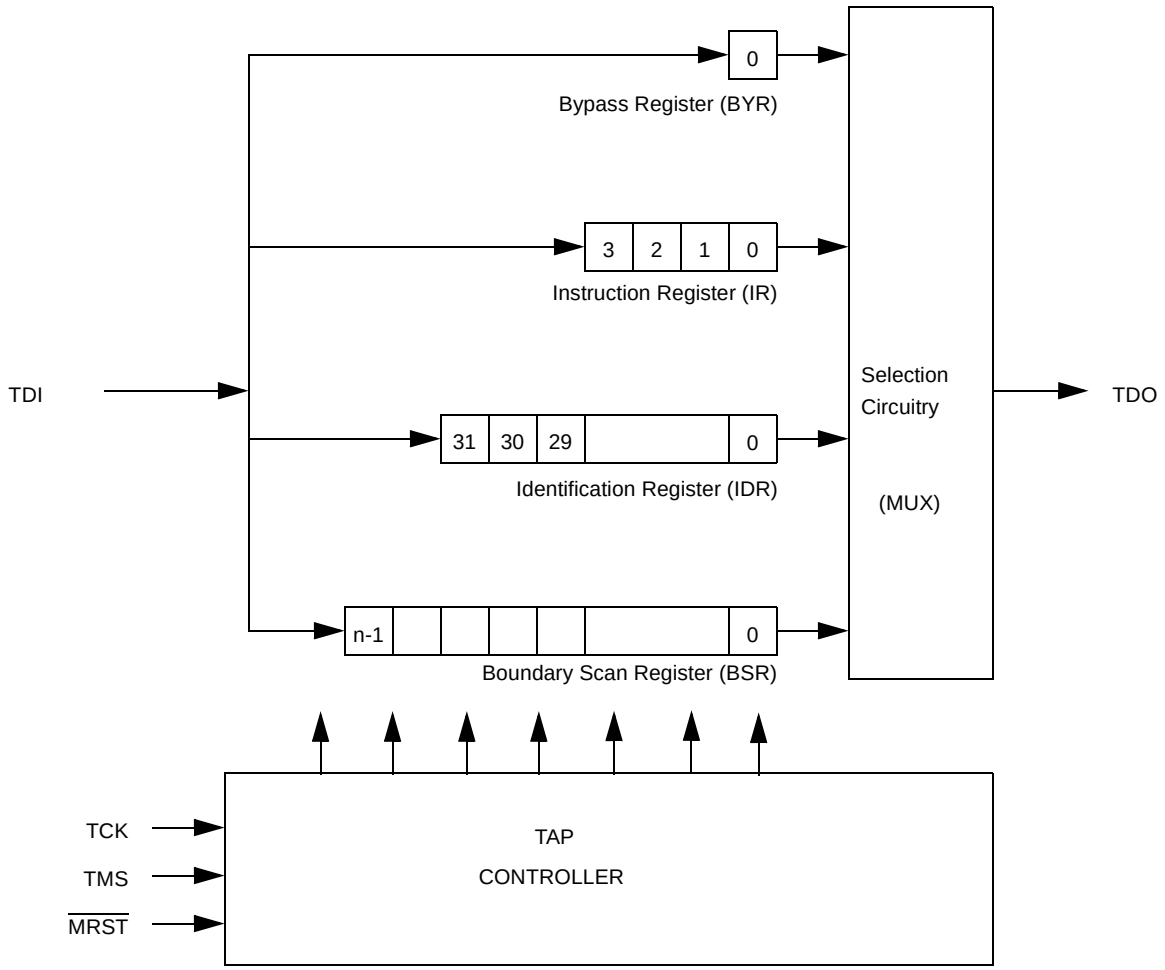


Figure 4. JTAG TAP Controller Block Diagram

Table 3. Identification Register Definitions

Instruction Field	Value	Description
Revision Number (31:28)	0h	Reserved for version number.
Cypress Device ID[18] (27:12)	C002h	Defines Cypress part number for CY7C0852V.
Cypress JEDEC ID (11:1)	034h	Allows unique identification of CY7C0851V/CY7C0852V/ CY7C0853V vendor.
ID Register Presence (0)	1	Indicates the presence of an ID register.

Table 4. Scan Registers Sizes

Register Name	Bit Size
Instruction	4
Bypass	1
Identification	32
Boundary Scan	n

Note:
18. Cypress Device ID is C001h for Cypress part CY7C0851V.

Table 5. Instruction Identification Codes

Instruction	Code	Description
EXTEST	0000	Captures the Input/Output ring contents. Places the BSR between the TDI and TDO.
BYPASS	1111	Places the BYR between TDI and TDO.
IDCODE	1011	Loads the IDR with the vendor ID code and places the register between TDI and TDO.
HIGHZ	0111	Places BYR between TDI and TDO. Forces all CY7C0851V/CY7C0852V/ CY7C0853V output drivers to a High-Z state.
CLAMP	0100	Controls boundary to 1/0. Places BYR between TDI and TDO.
SAMPLE/PRELOAD	1000	Captures the input/output ring contents. Places BSR between TDI and TDO.
NBSRST	1100	Resets the non-boundary scan logic. Places BYR between TDI and TDO.
RESERVED	All other codes	Other combinations are reserved. Do not use other than the above.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to + 150°C

Ambient Temperature with Power Applied.....–55°C to + 125°C

Supply Voltage to Ground Potential ..... –0.5V to + 4.6V

DC Voltage Applied to Outputs in High-Z State .....–0.5V to V_{DD} + 0.5V

DC Input Voltage ..... –0.5V to V_{DD} + 0.5V[19]

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage ..... > 2000V (JEDEC JESD22-A114-2000B)

Latch-up Current..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}
Commercial	0°C to +70°C	3.3V ± 165 mV
Industrial	–40°C to +85°C	3.3V ± 165 mV

Electrical Characteristics Over the Operating Range

Parameter	Description		CY7C0851V/CY7C0852V/CY7C0853V[6] CY7C0831V/CY7C0832V									Unit
			-150			-133			-100			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	Output HIGH Voltage (V_{DD} = Min., I_{OH}= –4.0 mA)		2.4			2.4			2.4			V
V_{OL}	Output LOW Voltage (V_{DD} = Min., I_{OL}= +4.0 mA)				0.4			0.4			0.4	V
V_{IH}	Input HIGH Voltage		2.0			2.0			2.0			V
V_{IL}	Input LOW Voltage				0.8			0.8			0.8	V
I_{OZ}	Output Leakage Current		–10		10	–10		10	–10		10	µA
I_{IX1}	Input Leakage Current Except TDI, TMS, $\overline{MRST}$		–10		10	–10		10	–10		10	µA
I_{IX2}	Input Leakage Current TDI, TMS, $\overline{MRST}$		–0.1		1.0	–0.1		1.0	–0.1		1.0	mA
I_{CC}	Operating Current (V_{DD} = Max., I_{OUT} = 0 mA) Outputs Disabled	Com'l.		300	450		270	400		200	310	mA
		Indust.										mA
I_{SB1}[5]	Standby Current (Both Ports TTL Level) $\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}	Com'l.		40	120		35	115		25	110	mA
		Indust.										mA
I_{SB2}[5]	Standby Current (One Port TTL Level) $\overline{CE}_L \mid \overline{CE}_R \geq V_{IH}$, f = f_{MAX}	Com'l.		230	280		220	250		145	190	mA
		Indust.										mA
I_{SB3}[17,5]	Standby Current (Both Ports CMOS Level) $\overline{CE}_L$ and $\overline{CE}_R \geq V_{DD} - 0.2V$, f = 0	Com'l.		10	75		10	75		10	75	mA
		Indust.										mA
I_{SB4}[5]	Standby Current (One Port CMOS Level) $\overline{CE}_L \mid \overline{CE}_R \geq V_{IH}$, f = f_{MAX}	Com'l.		200	255		180	230		130	175	mA
		Indust.										mA

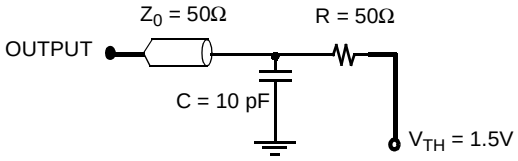
Shaded areas contain advance information.

Capacitance

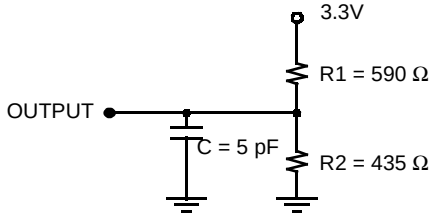
Parameter	Description	Test Conditions	Max. (all)	Max. (CY7C0853)	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V	13	22	pF
C_{OUT}	Output Capacitance		10	20	pF

Notes:
19. Pulse width < 20 ns.
20. (Internal I/O pad Capacitance = 10 pF) + AC Test Load.
21. External AC Test Load Capacitance = 10 pF.
22. Except JTAG signals (t_r and t_f < 10 ns [max.]).

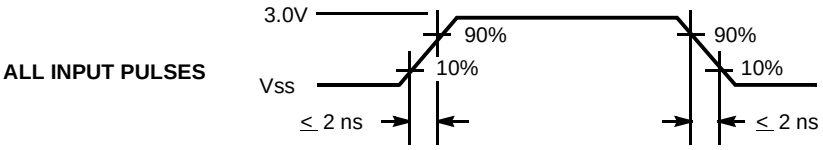
AC Test Load and Waveforms



(a) Normal Load (Load 1)



(b) Three-state Delay (Load 2)



Switching Characteristics Over the Operating Range

Parameter	Description	CY7C0851V/CY7C0852V/CY7C0853V[6] CY7C0831V/CY7C0832V						Unit
		-150		-133		-100		
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX2}	Maximum Operating Frequency		150		133		100	MHz
t_{CYC2}	Clock Cycle Time	6.7		7.5		10		ns
t_{CH2}	Clock HIGH Time	2.7		3.0		4.0		ns
t_{CL2}	Clock LOW Time	2.7		3.0		4.0		ns
t_R	Clock Rise Time		2.0		2.0		3.0	ns
t_F	Clock Fall Time		2.0		2.0		3.0	ns
t_{SA}	Address Set-Up Time	2.3		2.5		3.0		ns
t_{HA}	Address Hold Time	0.6		0.6		0.5		ns
t_{SB}	Byte Select Set-Up Time	2.3		2.5		3.0		ns
t_{HB}	Byte Select Hold Time	0.6		0.6		0.5		ns
t_{SC}	Chip Enable Set-Up Time	2.3		2.5		3.0		ns
t_{HC}	Chip Enable Hold Time	0.6		0.6		0.5		ns
t_{SW}	R/$\overline{W}$ Set-Up Time	2.3		2.5		3.0		ns
t_{HW}	R/$\overline{W}$ Hold Time	0.6		0.6		0.5		ns
t_{SD}	Input Data Set-Up Time	2.3		2.5		3.0		ns
t_{HD}	Input Data Hold Time	0.6		0.6		0.5		ns
t_{SAD}	$\overline{ADS}$ Set-Up Time	2.3		2.5		3.0		ns
t_{HAD}	$\overline{ADS}$ Hold Time	0.6		0.6		0.5		ns
t_{SCN}	$\overline{CNTEN}$ Set-Up Time	2.3		2.5		3.0		ns
t_{HCN}	$\overline{CNTEN}$ Hold Time	0.6		0.6		0.5		ns
t_{SRST}	$\overline{CNTRST}$ Set-Up Time	2.3		2.5		3.0		ns
t_{HRST}	$\overline{CNTRST}$ Hold Time	0.6		0.6		0.5		ns
t_{SCM}	CNT/$\overline{MSK}$ Set-Up Time	2.3		2.5		3.0		ns
t_{HCM}	CNT/$\overline{MSK}$ Hold Time	0.6		0.6		0.5		ns

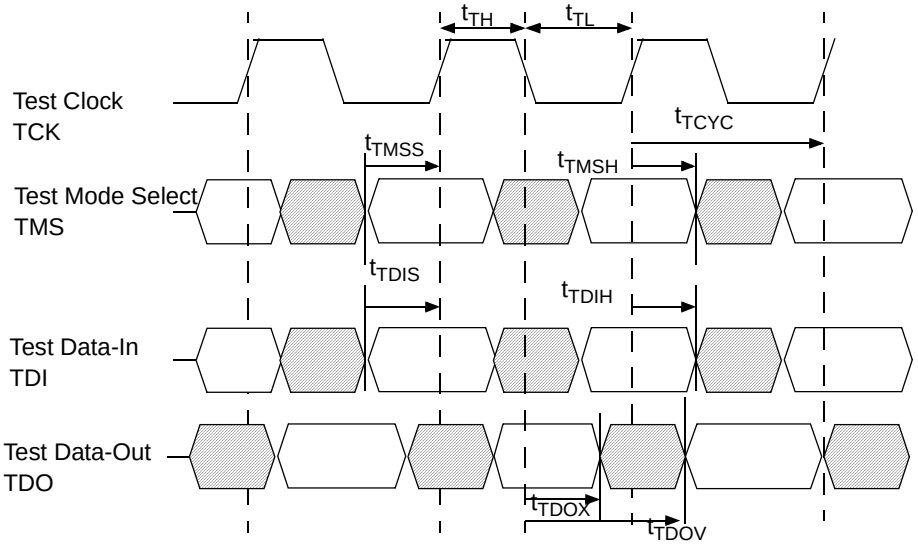
Switching Characteristics Over the Operating Range (continued)

Parameter	Description	CY7C0851V/CY7C0852V/CY7C0853V[6] CY7C0831V/CY7C0832V						Unit
		-150		-133		-100		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{OE}	Output Enable to Data Valid		4.0		4.4		5.0	ns
t_{OLZ}[23, 24]	$\overline{OE}$ to Low Z	0		0		0		ns
t_{OHZ}[23, 24]	$\overline{OE}$ to High Z	0	4.0	0	4.4	0	5.0	ns
t_{CD2}	Clock to Data Valid		4.0		4.4		5.0	ns
t_{CA2}	Clock to Counter Address Valid		4.0		4.4		5.0	ns
t_{CM2}	Clock to Mask Register Readback Valid		4.0		4.4		5.0	ns
t_{DC}	Data Output Hold After Clock HIGH	1.0		1.0		1.0		ns
t_{CKHZ}[23, 24]	Clock HIGH to Output High Z	0	4.0	0	4.4	0	5.0	ns
t_{CKLZ}[23, 24]	Clock HIGH to Output Low Z	1.0	4.0	1.0	4.4	1.0	5.0	ns
t_{SINT}	Clock to $\overline{INT}$ Set Time	0.5	6.7	0.5	7.5	0.5	10	ns
t_{RINT}	Clock to $\overline{INT}$ Reset Time	0.5	6.7	0.5	7.5	0.5	10	ns
t_{SCINT}	Clock to $\overline{CNTINT}$ Set Time	0.5	5.0	0.5	5.7	0.5	7.5	ns
t_{RCINT}	Clock to $\overline{CNTINT}$ Reset time	0.5	5.0	0.5	5.7	0.5	7.5	ns
Port to Port Delays								
t_{CCS}	Clock to Clock Skew	5.2		6.0		8.0		ns
Master Reset Timing								
t_{RS}	Master Reset Pulse Width	7.0		7.5		10		ns
t_{RSS}	Master Reset Set-Up Time	6.0		6.0		8.5		ns
t_{RSR}	Master Reset Recovery Time	6.0		7.5		10		ns
t_{RSF}	Master Reset to Outputs Inactive		6.0		6.5		8.0	ns
$t_{RSCNTINT}$	Master Reset to Counter Interrupt Flag Reset Time		5.8		7.0		8.0	ns

JTAG Timing and Switching Waveforms

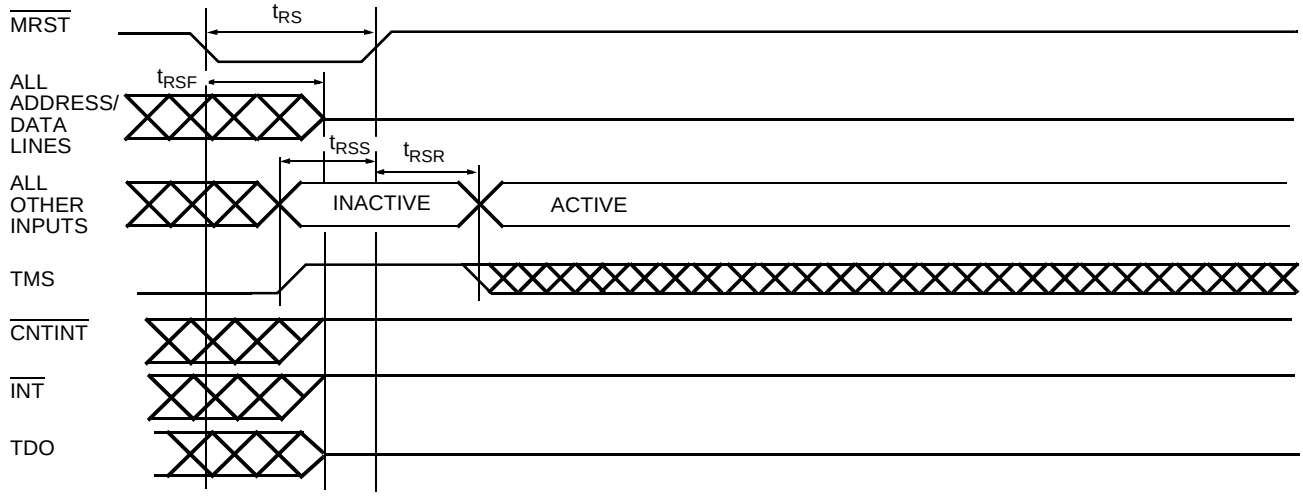
Parameter	Description	CY7C0852V -150/133/100		Unit
		Min.	Max.	
f_{JTAG}	Maximum JTAG TAP Controller Frequency		10	MHz
t_{TCYC}	TCK Clock Cycle Time	100		ns
t_{TH}	TCK Clock HIGH Time	40		ns
t_{TL}	TCK Clock LOW Time	40		ns
t_{TMSS}	TMS Set-Up to TCK Clock Rise	10		ns
t_{TMSH}	TMS Hold After TCK Clock Rise	10		ns
t_{TDIS}	TDI Set-Up to TCK Clock Rise	10		ns
t_{TDIH}	TDI Hold after TCK Clock Rise	10		ns
t_{TDOV}	TCK Clock LOW to TDO Valid		30	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns

Notes:
23. This parameter is guaranteed by design, but it is not production tested.
24. Test conditions used are Load 2.



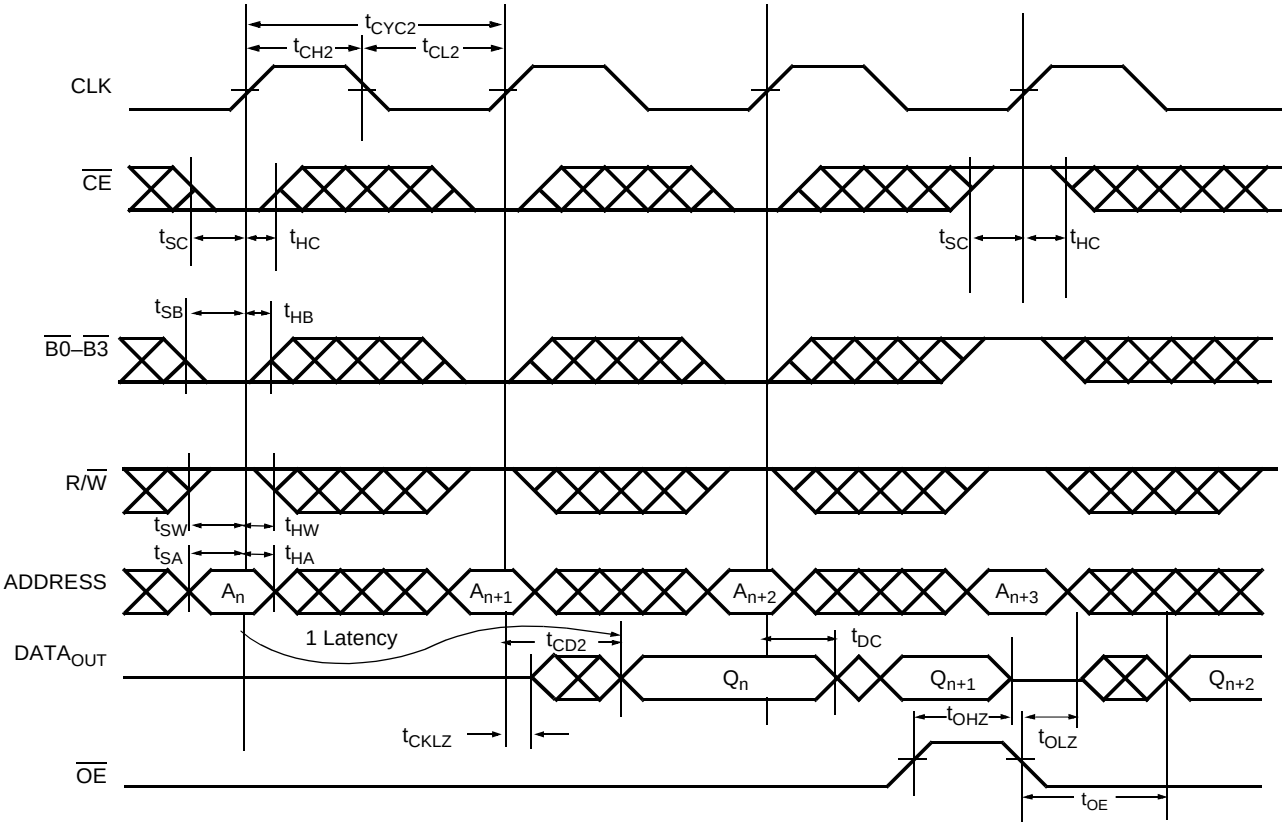
Switching Waveforms

Master Reset



Switching Waveforms (continued)

Read Cycle[25, 26, 27, 28, 9]

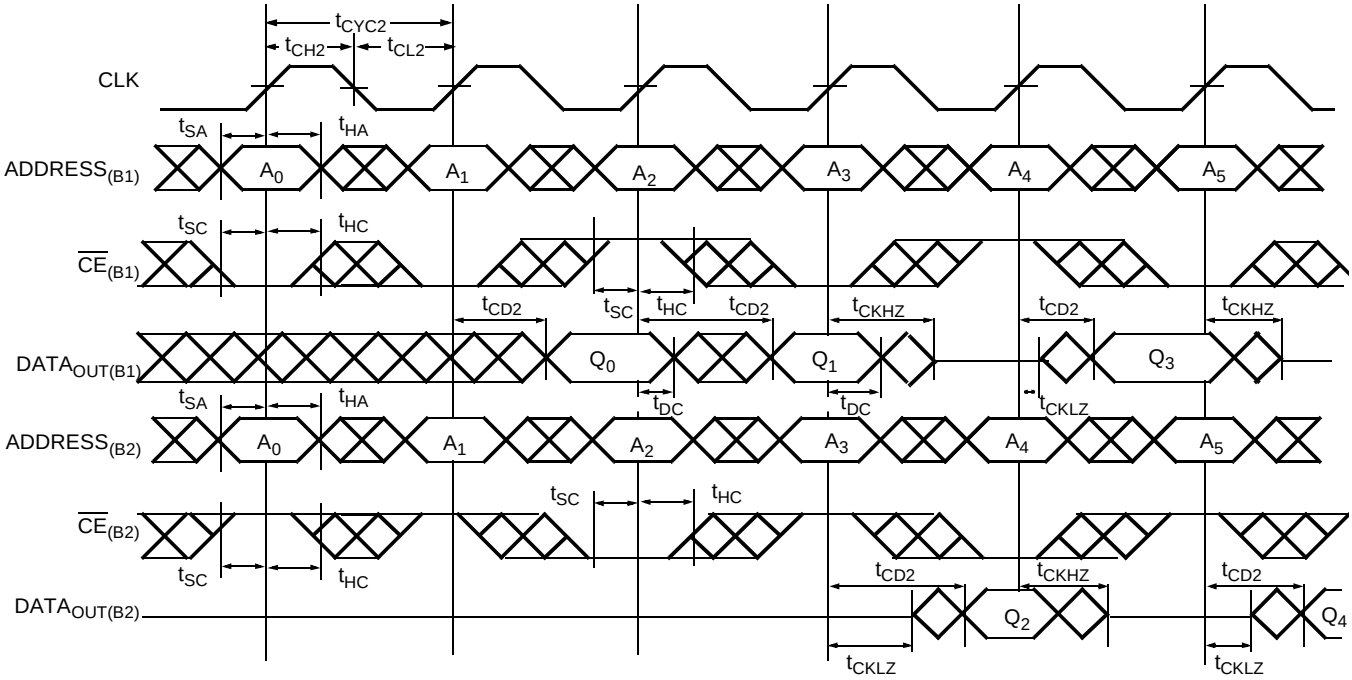


Notes:

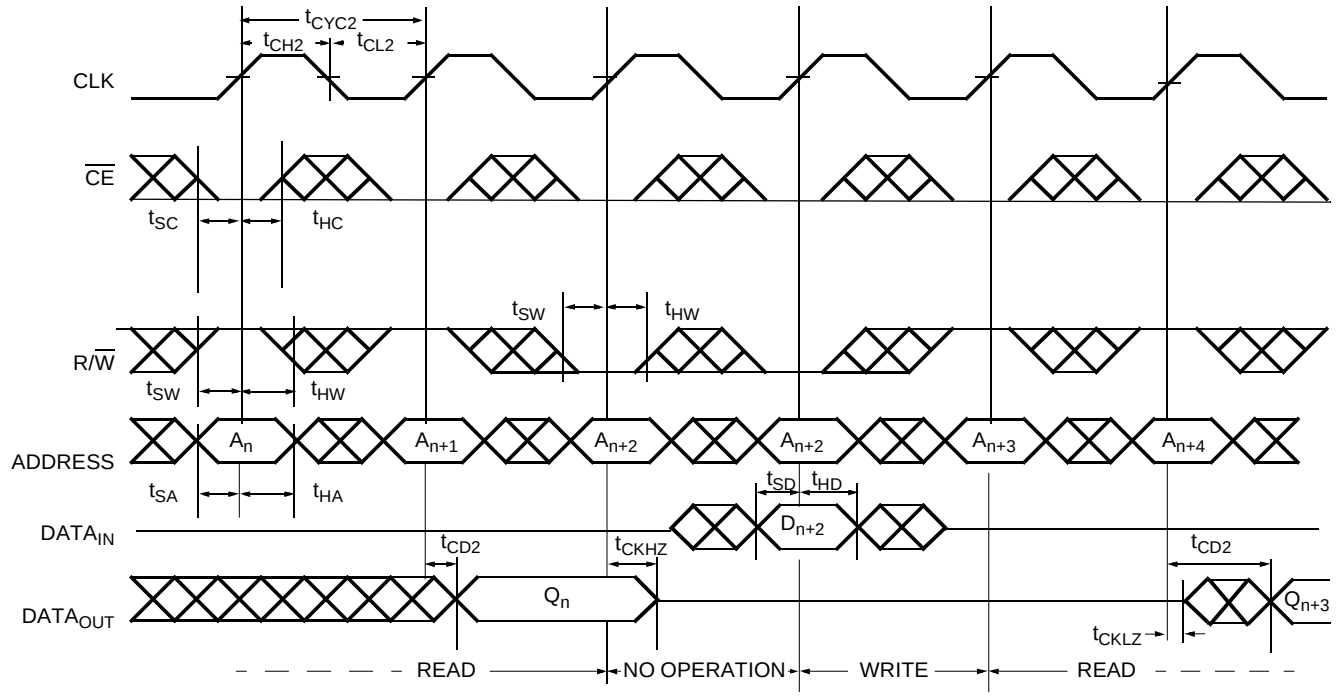
25. OE is asynchronously controlled; all other inputs (excluding MRST and JTAG) are synchronous to the rising clock edge.
26. ADS = CNTEN = LOW, and MRST = CNTRST = CNT/MSK = HIGH.
27. The output is disabled (high-impedance state) by CE = V_{IH} following the next rising edge of the clock.
28. Addresses do not have to be accessed sequentially since ADS = CNTEN = V_{IL} with CNT/MSK = V_{IH} constantly loads the address on the rising edge of the CLK. Numbers are for reference only.

Switching Waveforms (continued)

Bank Select Read[29, 30]



Read-to-Write-to-Read ($\overline{OE}$ = LOW)[28, 31, 32, 33, 34]

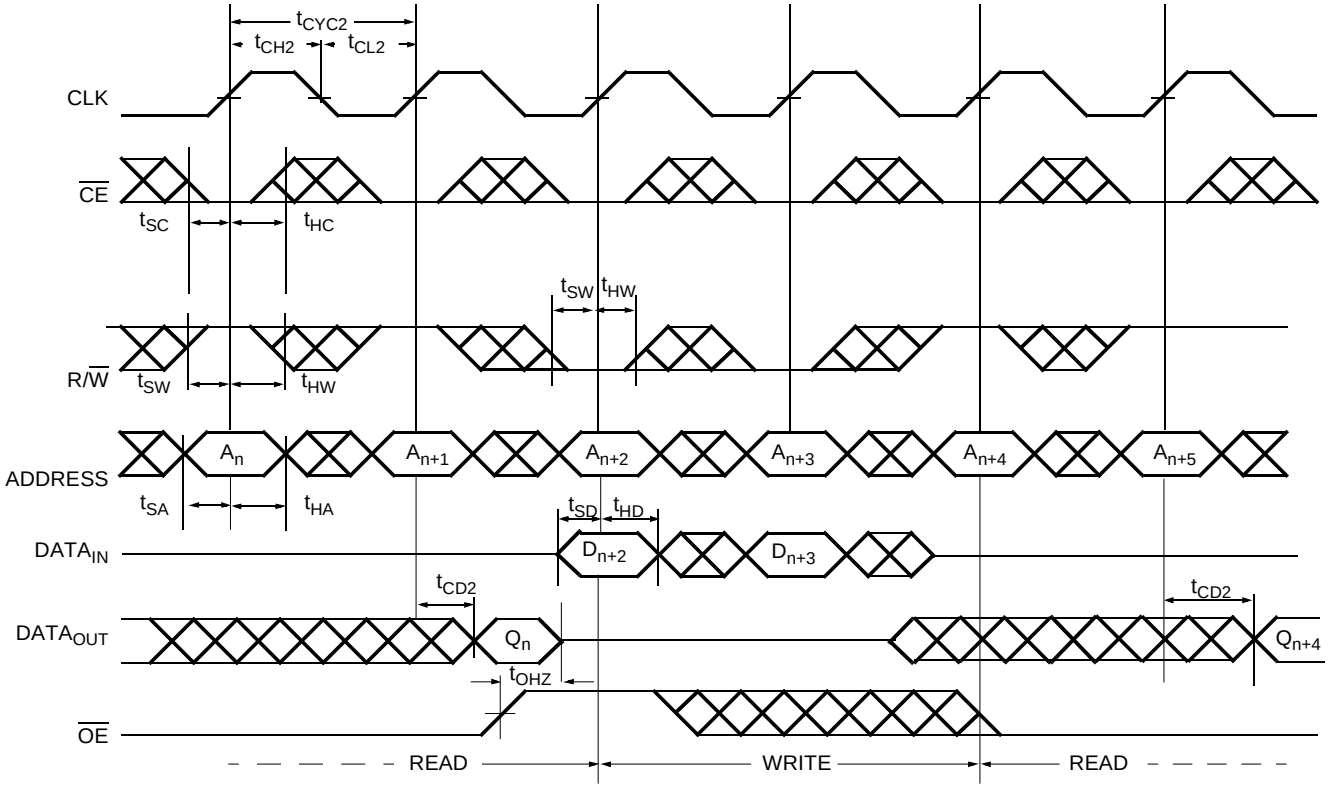


Notes:

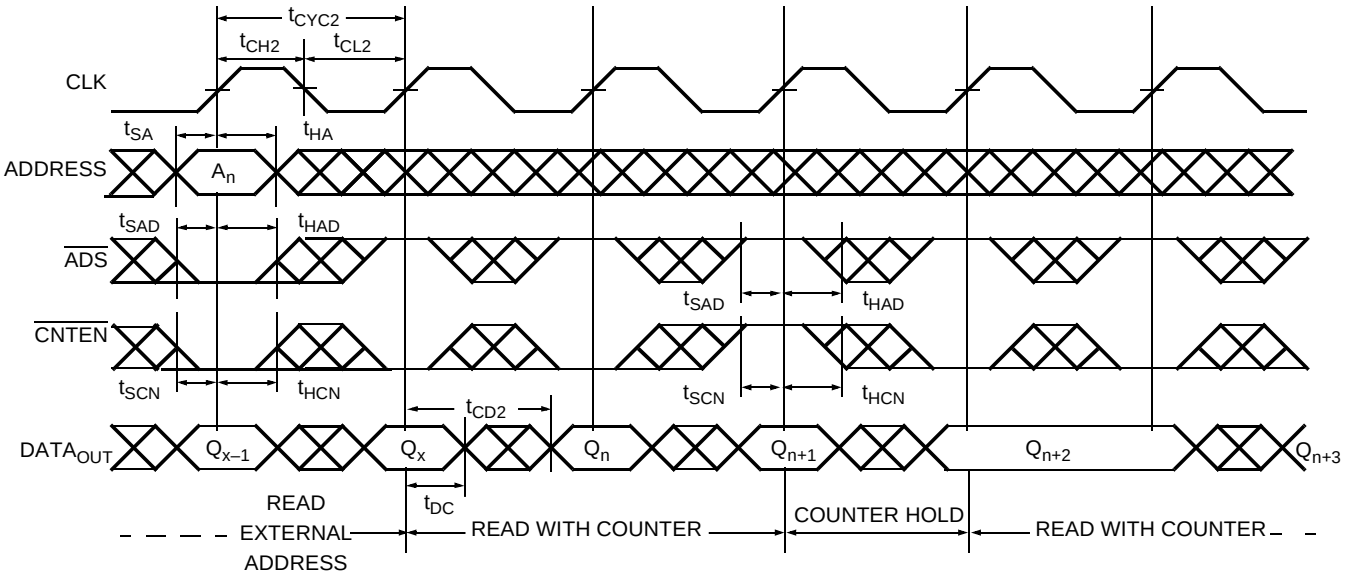
29. In this depth-expansion example, B1 represents Bank #1 and B2 is Bank #2; each bank consists of one Cypress CY7C085XV device from this data sheet. $ADDRESS_{(B1)}$ = $ADDRESS_{(B2)}$.
30. $\overline{ADS}$ = CNTEN= B0 – B3 = $\overline{OE}$ = LOW; $\overline{MRST}$ = $\overline{CNTRST}$ = CNT/$\overline{MSK}$ = HIGH.
31. Output state (HIGH, LOW, or high-impedance) is determined by the previous cycle control signals.
32. During "No Operation," data in memory at the selected address may be corrupted and should be rewritten to ensure data integrity.
33. $\overline{CE_0}$ = $\overline{OE}$ = B0 – B3 = LOW; CE_1 = R/$\overline{W}$ = CNTRST = MRST = HIGH.
34. $\overline{CE_0}$ = B0 – B3 = R/$\overline{W}$ = LOW; $\overline{CE_1}$ = CNTRST = MRST = CNT/MSK = HIGH. When R/$\overline{W}$ first switches low, since OE = LOW, the Write operation cannot be completed (labelled as no operation). One clock cycle is required to three-state the I/O for the Write operation on the next rising edge of CLK.

Switching Waveforms (continued)

Read-to-Write-to-Read ($\overline{OE}$ Controlled)[28, 31, 33, 34]

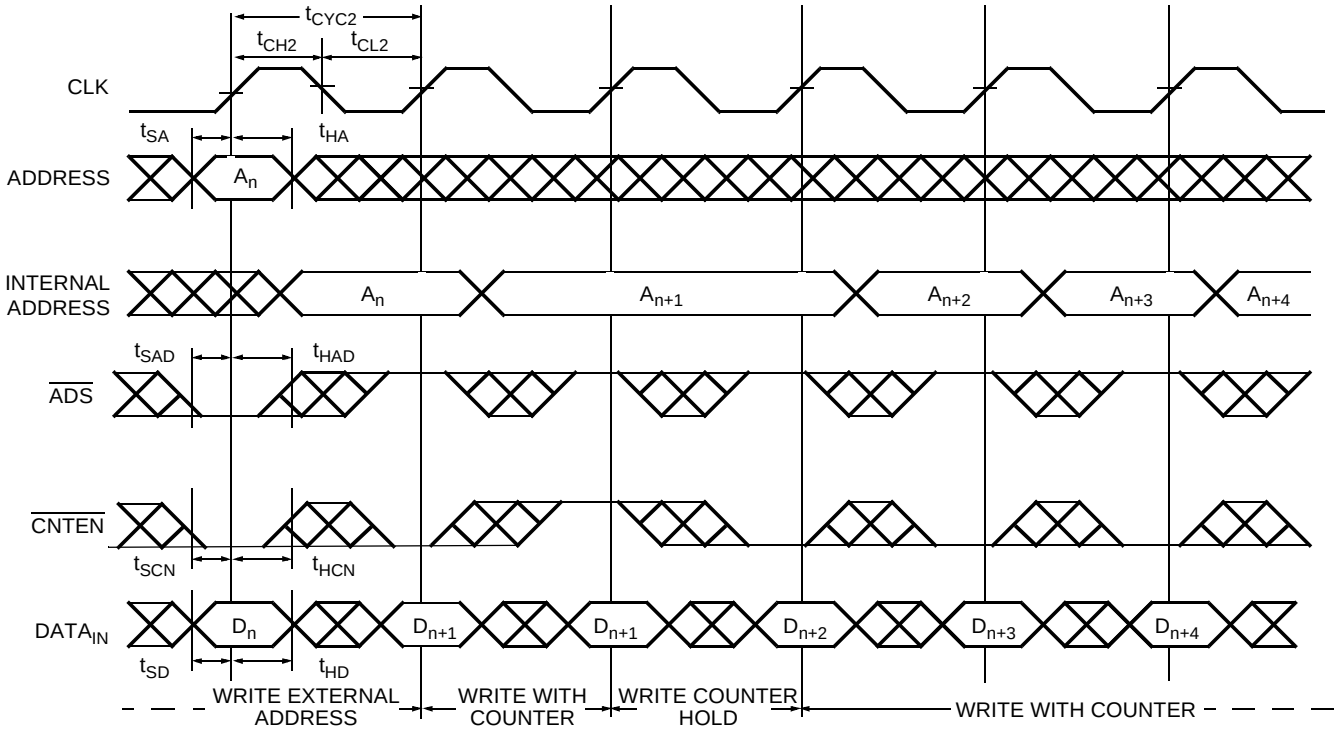


Read with Address Counter Advance[2, 33]



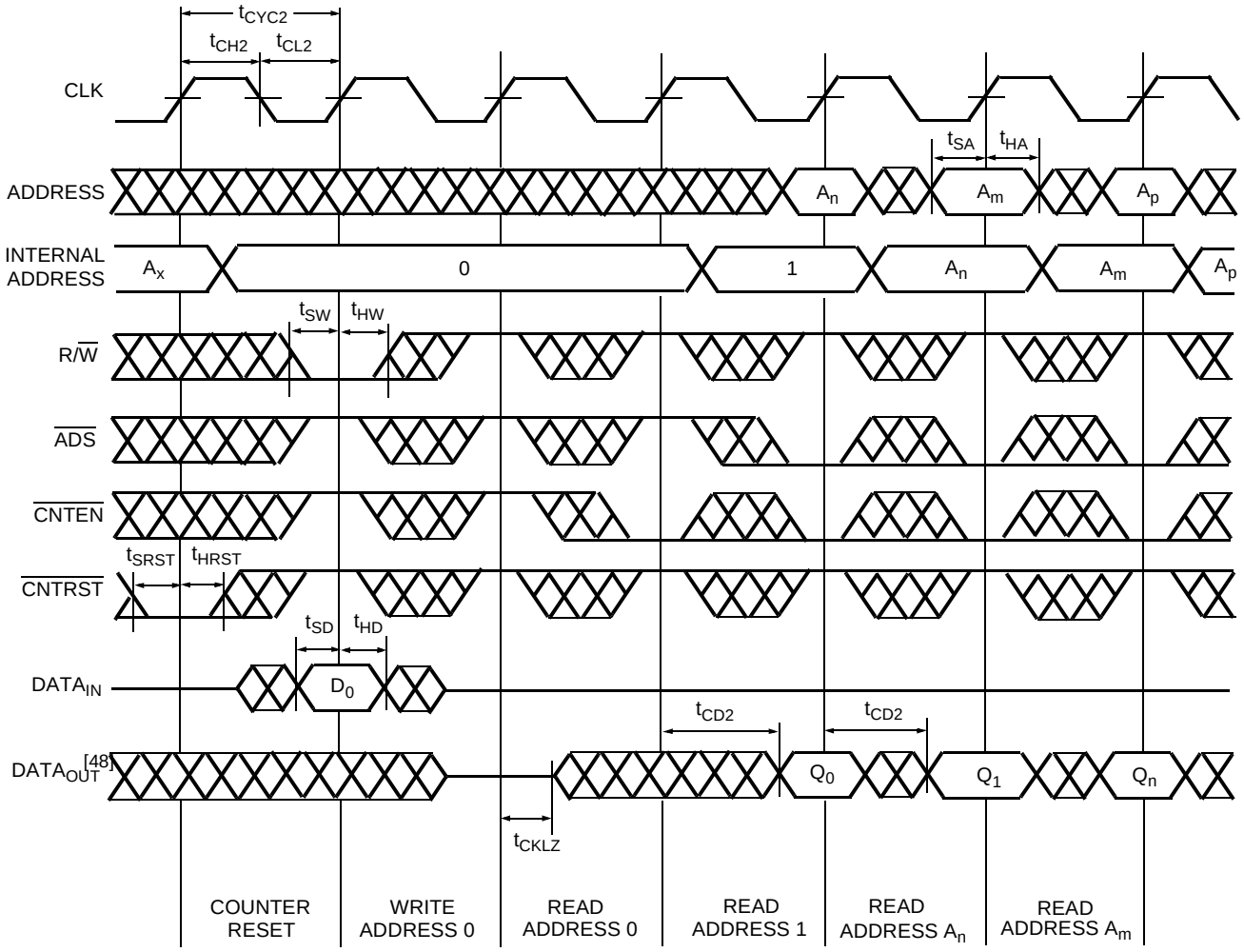
Switching Waveforms (continued)

Write with Address Counter Advance [2, 34]



Switching Waveforms (continued)

Counter Reset [2, 35, 36]

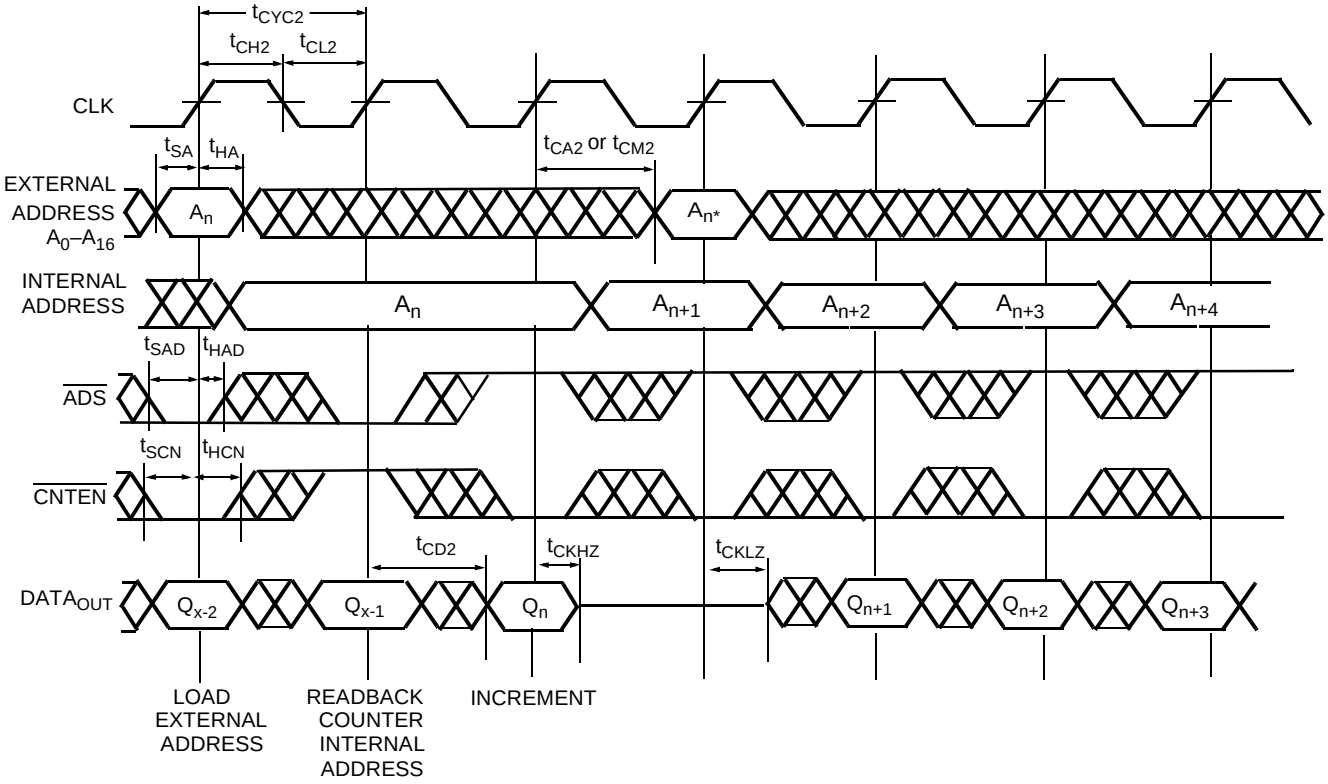


Notes:

35. $\overline{CE_0}$ = $\overline{B0}$ – $\overline{B3}$ = LOW; CE_1 = $\overline{MRST}$ = CNT/$\overline{MSK}$ = HIGH.
36. No dead cycle exists during counter reset. A Read or Write cycle may be coincidental with the counter reset.

Switching Waveforms (continued)

Readback State of Address Counter or Mask Register[2, 37, 38, 39, 40]

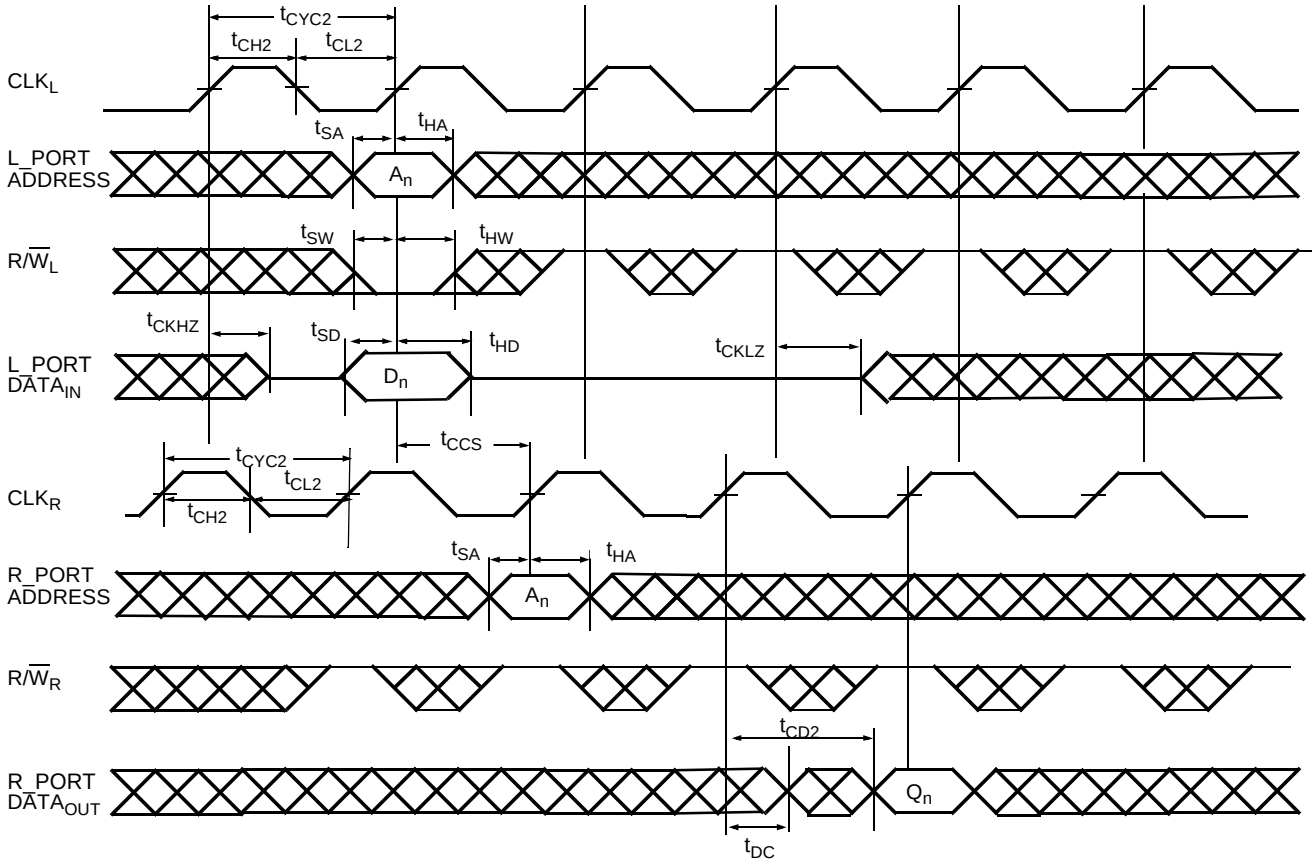


Notes:

37. $\overline{CE_0}$ = $\overline{OE}$ = $\overline{B0}$ – $\overline{B3}$ = LOW; CE_1 = R/$\overline{W}$ = $\overline{CNTRST}$ = $\overline{MRST}$ = HIGH.
38. Address in output mode. Host must not be driving address bus after t_{CKLZ} in next clock cycle.
39. Address in input mode. Host can drive address bus after t_{CKHZ}.
40. An * is the internal value of the address counter (or the mask register depending on the CNT/$\overline{MSK}$ level) being Read out on the address lines.

Switching Waveforms (continued)

Left_Port (L_Port) Write to Right_Port (R_Port) Read[41, 42, 43]

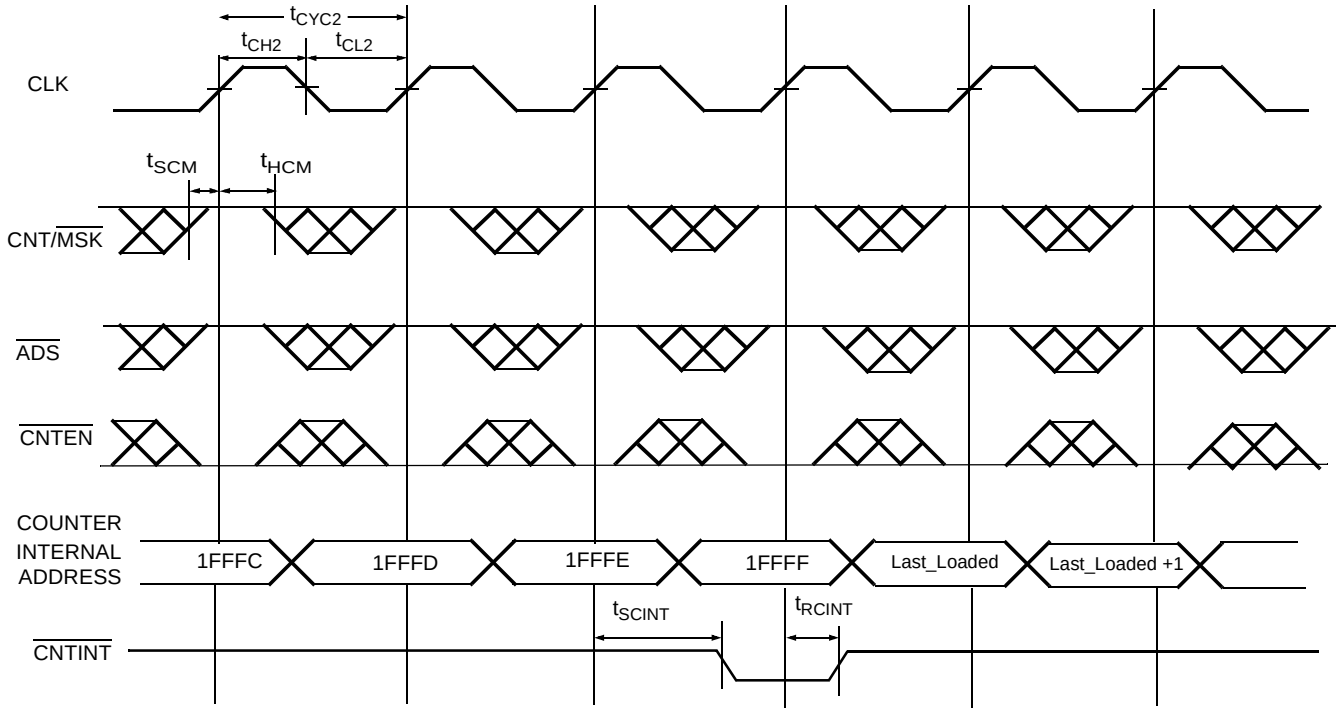


Notes:

41. $\overline{CE_0}$ = $\overline{OE}$ = $\overline{ADS}$ = $\overline{CNTEN}$ = $\overline{B0}$ – $\overline{B3}$ = LOW; CE_1 = $\overline{CNTRST}$ = $\overline{MRST}$ = CNT/$\overline{MSK}$ = HIGH.
42. This timing is valid when one port is writing, and other port is reading the same location at the same time. If t_{CCS} is violated, indeterminate data will be Read out.
43. If t_{CCS} < minimum specified value, then R_Port will Read the most recent data (written by L_Port) only (2 * t_{CYC2} + t_{CD2}) after the rising edge of R_Port's clock. If t_{CCS} ≥ minimum specified value, then R_Port will Read the most recent data (written by L_Port) (t_{CYC2} + t_{CD2}) after the rising edge of R_Port's clock.

Switching Waveforms (continued)

Counter Interrupt and Retransmit[2, 44, 45, 46, 47, 48]



Notes:
44. $\overline{CE_0}$ = $\overline{OE}$ = $\overline{B0}$ – $\overline{B3}$ = LOW; CE_1 = R/$\overline{W}$ = $\overline{CNTRST}$ = $\overline{MRST}$ = HIGH.
45. $\overline{CNTINT}$ is always driven.
46. CNTINT goes LOW when the unmasked portion of the address counter is incremented to the maximum value.
47. The mask register assumed to have the value of 1FFFFh.
48. Retransmit happens if the counter remains in increment mode after it wraps to initially loaded value.

Switching Waveforms (continued)

MailBox Interrupt Timing[49, 50, 51, 52, 53]

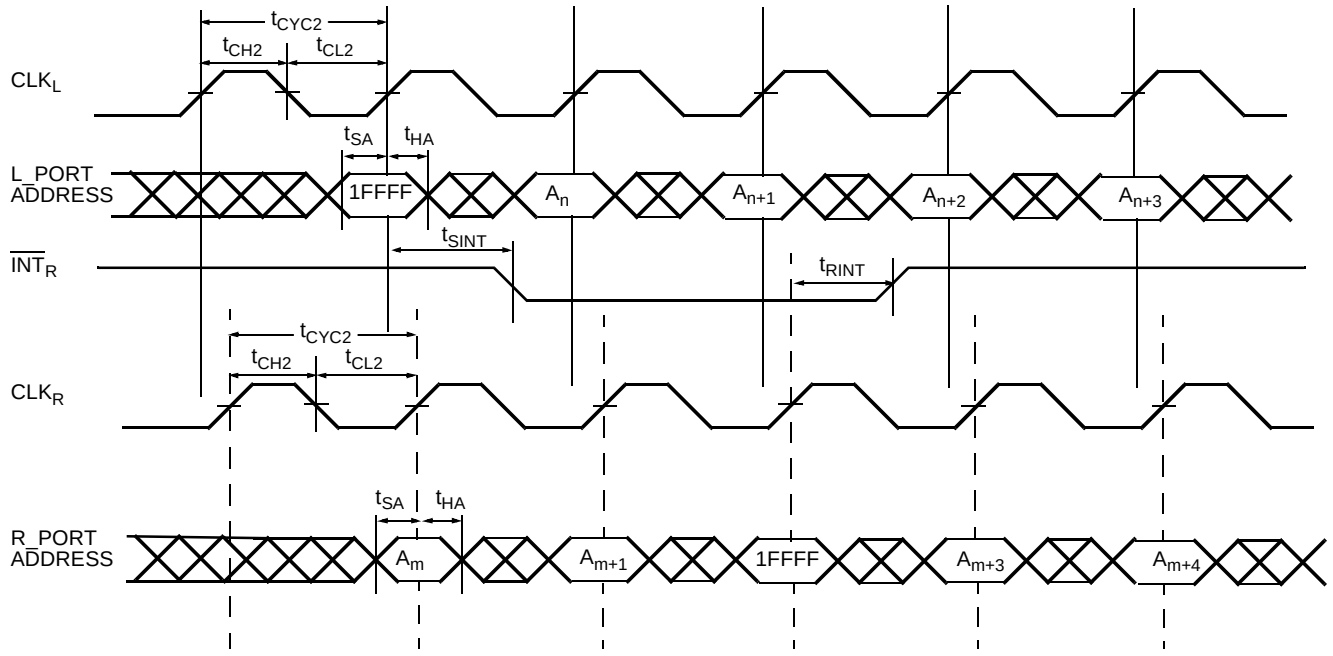


Table 6. Read/Write and Enable Operation (Any Port)[1, 7, 54, 55, 56]

Inputs					Outputs	
$\overline{OE}$	CLK	$\overline{CE_0}$	CE_1	R/$\overline{W}$	$DQ_0 - DQ_{35}$	Operation
X	↑	H	X	X	High-Z	Deselected
X	↑	X	L	X	High-Z	Deselected
X	↑	L	H	L	D_{IN}	Write
L	↑	L	H	H	D_{OUT}	Read
H	X	L	H	X	High-Z	Outputs Disabled

Notes:
49. $\overline{CE_0}$ = $\overline{OE}$ = $\overline{ADS}$ = $\overline{CNTEN}$ = LOW; CE_1 = $\overline{CNTRST}$ = $\overline{MRST}$ = CNT/$\overline{MSK}$ = HIGH.
50. Address "1FFFF" is the mailbox location for R_Port.
51. L_Port is configured for Write operation, and R_Port is configured for Read operation.
52. At least one byte enable (B0 – B3) is required to be active during interrupt operations.
53. Interrupt flag is set with respect to the rising edge of the Write clock, and is reset with respect to the rising edge of the Read clock.
54. $\overline{OE}$ is an asynchronous input signal.
55. When $\overline{CE}$ changes state, deselection and Read happen after one cycle of latency.
56. $\overline{CE_0}$ = $\overline{OE}$ = LOW; CE_1 = R/$\overline{W}$ = HIGH.

Ordering Information

256K × 36 (9M) 3.3V Synchronous CY7C0853V Dual-Port SRAM

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
150	CY7C0853V-150BBC	BB172	172-ball Grid Array 15 mm × 15 mm with 1.0 mm pitch (BGA)	Commercial
133	CY7C0853V-133BBC	BB172	172-ball Grid Array 15 mm × 15 mm with 1.0 mm pitch (BGA)	Commercial
100	CY7C0853V-100BBC	BB172	172-ball Grid Array 15 mm × 15 mm with 1.0 mm pitch (BGA)	Commercial
	CY7C0853V-100BBI	BB172	172-ball Grid Array 15 mm × 15 mm with 1.0 mm pitch (BGA)	Industrial

256K × 18 (4M) 3.3V Synchronous CY7C0832V Dual-Port SRAM

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
150	CY7C0832V-150AC	A120	120-pin Flat Pack 14 mm × 14 mm (TQFP)	Commercial
133	CY7C0832V-133AC	A120	120-pin Flat Pack 14 mm × 14 mm (TQFP)	Commercial
100	CY7C0832V-100AC	A120	120-pin Flat Pack 14 mm × 14 mm (TQFP)	Commercial
	CY7C0832V-100AI	A120	120-pin Flat Pack 14 mm × 14 mm (TQFP)	Industrial

128K × 36 (4M) 3.3V Synchronous CY7C0852V Dual-Port SRAM

150	CY7C0852V-150BBC	BB172	172-ball Grid Array 15 mm × 15 mm with 1.0 mm pitch (BGA)	Commercial
	CY7C0852V-150AC	A176	176-pin Flat Pack 24 mm × 24 mm (TQFP)	Commercial
133	CY7C0852V-133BBC	BB172	172-ball Grid Array 15 mm × 15 mm with 1.0 mm pitch (BGA)	Commercial
	CY7C0852V-133BBI	BB172	172-ball Grid Array 15 mm × 15 mm with 1.0 mm pitch (BGA)	Industrial
	CY7C0852V-133AC	A176	176-pin Flat Pack 24 mm × 24 mm (TQFP)	Commercial
100	CY7C0852V-100BBC	BB172	172-ball Grid Array 15 mm × 15 mm with 1.0 mm pitch (BGA)	Commercial
	CY7C0852V-100AC	A176	176-pin Flat Pack 24 mm × 24 mm (TQFP)	Commercial
	CY7C0852V-100BBI	BB172	172-ball Grid Array 15 mm × 15 mm with 1.0 mm pitch (BGA)	Industrial
	CY7C0852V-100AI	A176	176-pin Flat Pack 24 mm × 24 mm (TQFP)	Industrial

128K × 18 (2M) 3.3V Synchronous CY7C0831V Dual-Port SRAM

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
150	CY7C0831V-150AC	A120	120-pin Flat Pack 14 mm × 14 mm (TQFP)	Commercial
133	CY7C0831V-133AC	A120	120-pin Flat Pack 14 mm × 14 mm (TQFP)	Commercial
100	CY7C0831V-100AC	A120	120-pin Flat Pack 14 mm × 14 mm (TQFP)	Commercial

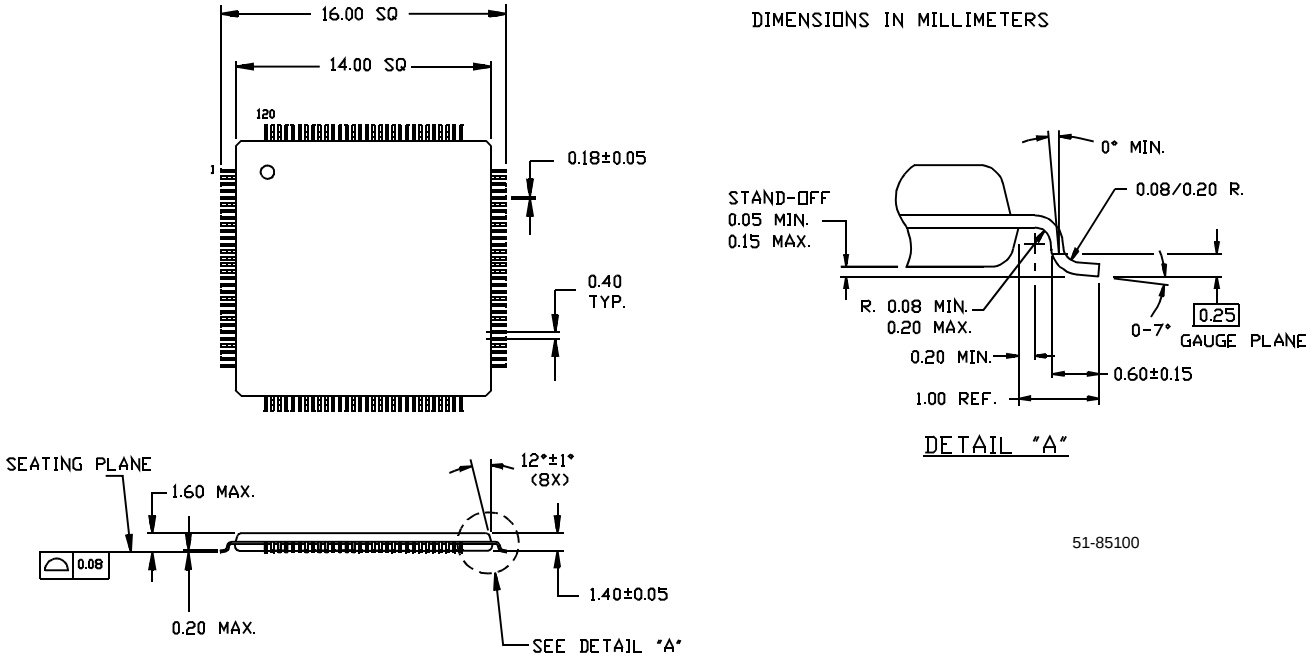
64K × 36 (2M) 3.3V Synchronous CY7C0851V Dual-Port SRAM

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
150	CY7C0851V-150BBC	BB172	172-ball Grid Array 15 mm × 15 mm with 1.0 mm pitch (BGA)	Commercial
	CY7C0851V-150AC	A176	176-pin Flat Pack 24 mm × 24 mm (TQFP)	Commercial
133	CY7C0851V-133BBC	BB172	172-ball Grid Array 15 mm × 15 mm with 1.0 mm pitch (BGA)	Commercial
	CY7C0851V-133AC	A176	176-pin Flat Pack 24 mm × 24 mm (TQFP)	Commercial
	CY7C0851V-133BBI	BB172	172-ball Grid Array 15 mm × 15 mm with 1.0 mm pitch (BGA)	Industrial
100	CY7C0851V-100BBC	BB172	172-ball Grid Array 15 mm × 15 mm with 1.0 mm pitch (BGA)	Commercial
	CY7C0851V-100AC	A176	176-pin Flat Pack 24 mm × 24 mm (TQFP)	Commercial

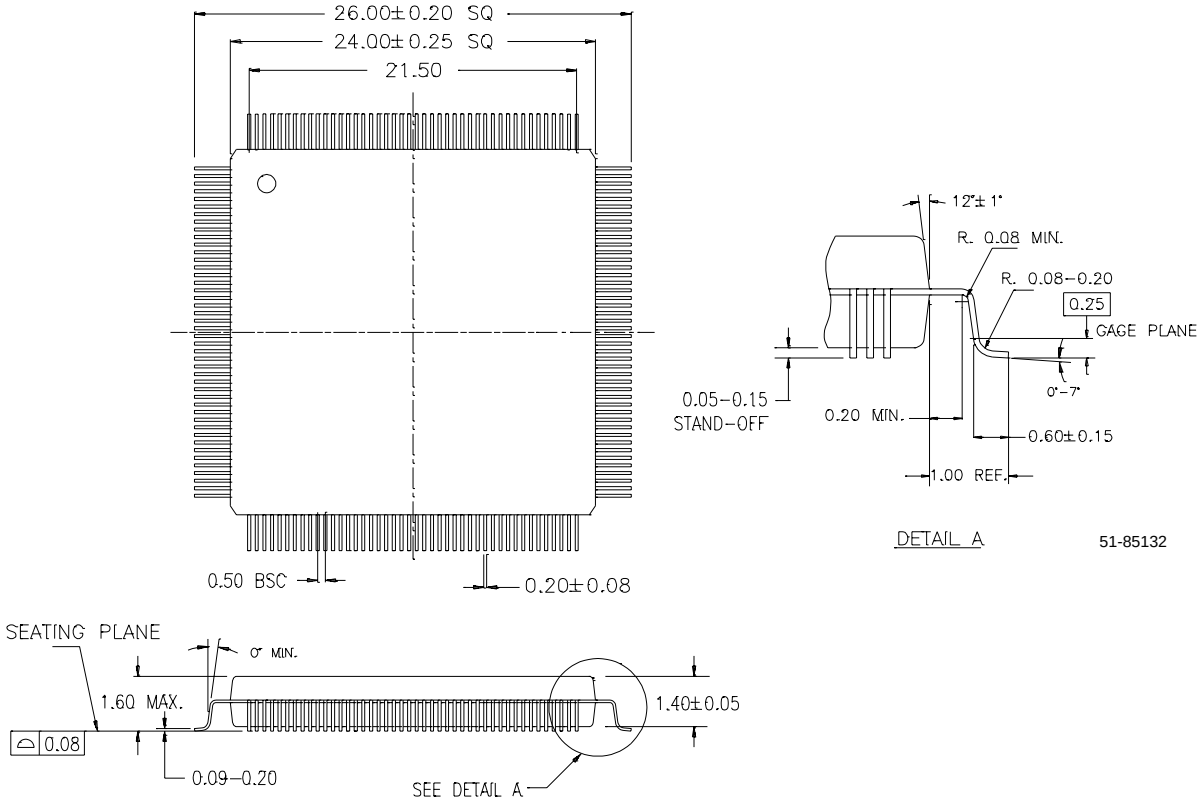
Shaded areas contain advance information.

Package Diagrams

120-pin thin Quad Flatpack (14 × 14 × 1.4 mm) A120

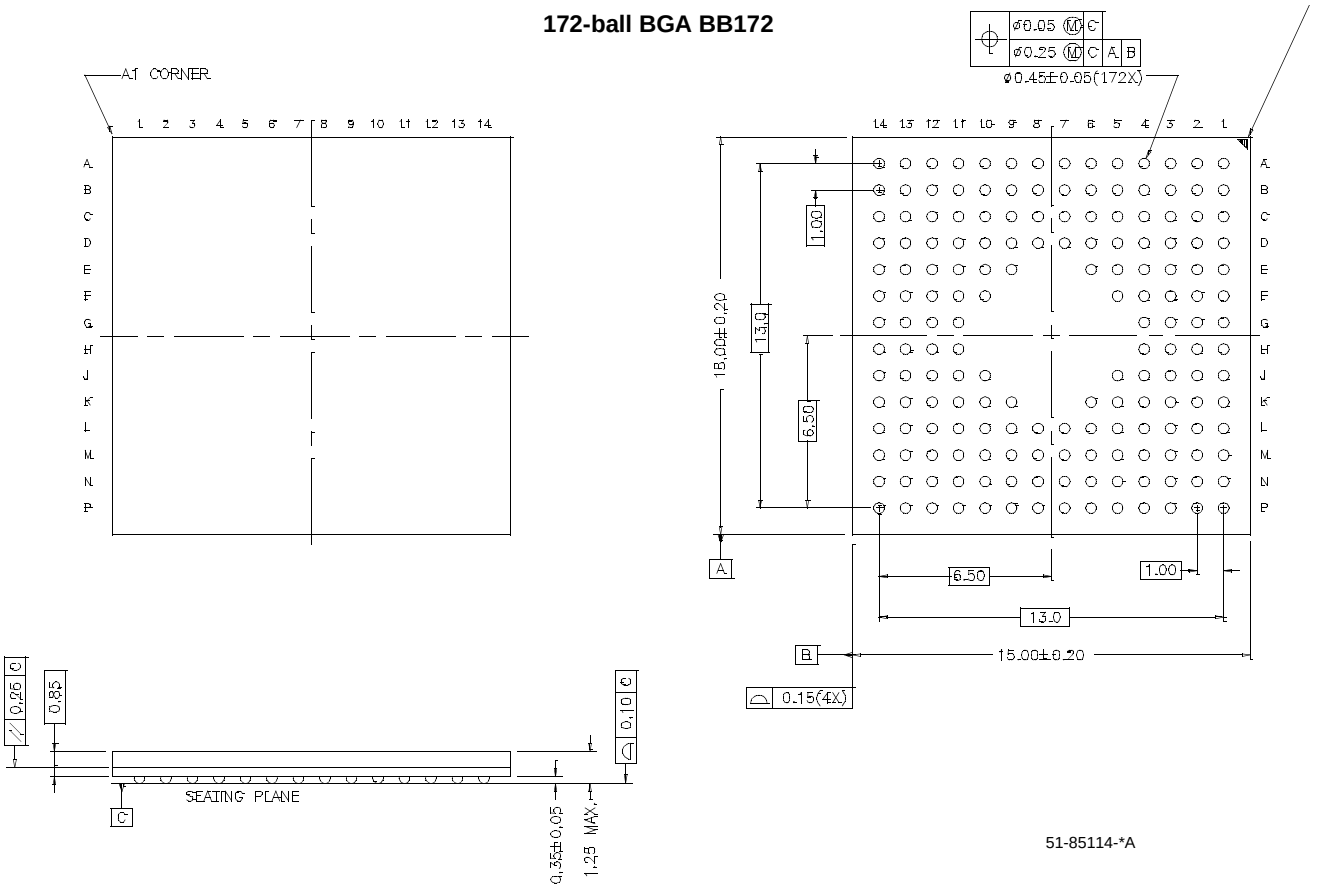


176-lead Thin Quad Flat Pack (24 × 24 × 1.4 mm) A176



Package Diagrams (continued)

172-ball BGA BB172



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Document Number: 38-06059

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	111473	11/27/01	DSG	Change from Spec number: 38-01056 to 38-06059
*A	111942	12/21/01	JFU	Updated capacitance values Updated switching parameters and I_{SB3} Updated “Read-to-Write-to-Read ($\overline{OE}$ Controlled)” waveform Revised static discharge voltage Revised footnote regarding I_{SB3}
*B	113741	04/02/02	KRE	Updated I_{sb} values Updated ESD voltage Corrected 0853 pins L3 and L12
*C	114704	04/24/02	KRE	Added discussion of Pause/Restart for JTAG boundary scan