AAT3125
USB OTG 5V Charge Pump

ChargePump™

General Description

The AAT3125 USB On-the-Go (OTG) Charge Pump is a member of AnalogicTech™'s Total Power Management™ IC product family. The device integrates a high efficiency 1.5x fractional 100mA Regulated Charge Pump for supplying V_{BUS} with the additional functions required for OTG-devices (formerly known as Dual Role Devices). Four voltage detectors monitor V_{BUS} and a current source, dedicated for V_{BUS} pulsing, are provided for compliance with Session Request Protocol (SRP) as defined by the USB OTG Supplement.

The charge pump section uses a high efficiency fractional topology, with a high frequency 750kHz switching speed which enables the use of small capacitors less than 3.3µF. The AAT3125 features extremely low quiescent current to extend battery run time. Additionally, the device integrates protection features such as undervoltage lockout, output short circuit and thermal protection.

The AAT3125 is available in a surface mount QFN-16 package, and is rated from -40°C to 85°C.

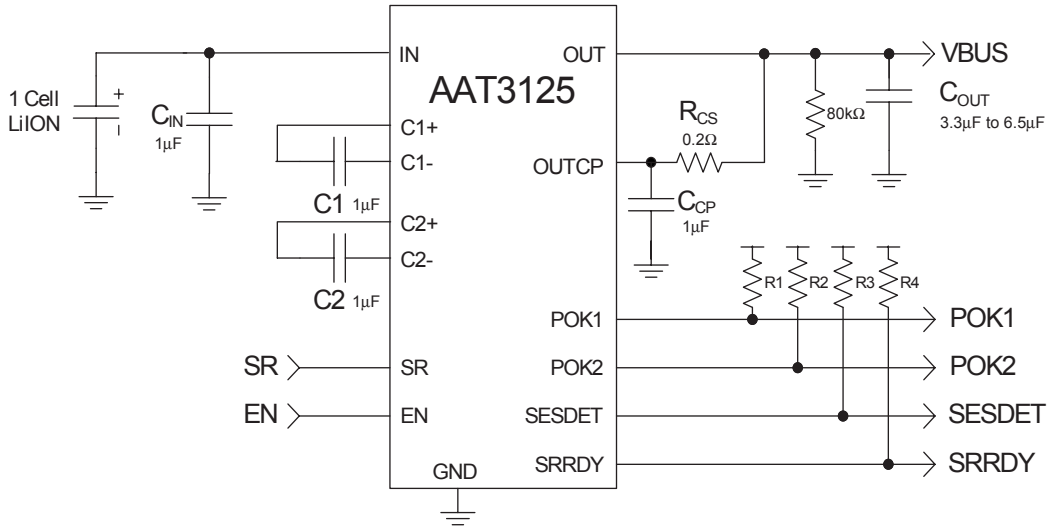
Features

- Regulated Fractional Charge Pump
- 100 mA Output Current
- Reverse Load Protection
- Power Good Flag
- SRP detection Flag
- SRP Ready Flag
- Output Short Circuit and Thermal Protection
- Under Voltage Protection
- Less than 1µA consumed while disabled
- Designed to allow operation with output capacitance as low as 3.3µF.
- 16-pin 4x4mm QFN package

Applications

- Cell Phones
- Hand Held Computers
- PDAs

Typical Application

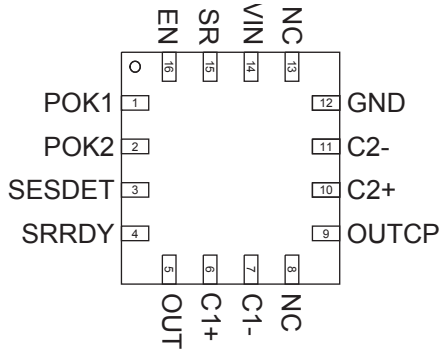


Pin Descriptions

Pin #	Symbol	Function
1	POK1	Power OK 1. Open drain output with 4.0V voltage detector. When the OUT pin rises above the detected Voltage (4.0 V), POK1 will transition from low to high state. Similarly, when the output falls below 4.0 Volts, POK1 will transition from high to low. A 10 KΩ pull up resistor is recommended.
2	POK2	Power OK 2. Open drain output with 4.4V voltage detector. When the OUT pin rises above the detected Voltage (4.4 V), POK2 will transition from low to high state. Similarly, when the output falls below 4.4 Volts, POK2 will transition from high to low. A 10 KΩ pull up resistor is recommended.
3	SESDET	Session detect. Open drain output with 2.0V voltage detector. When the OUT pin rises above the detected Voltage (2.0 V), it will transition from low to high state. Similarly, when the output falls below 2.0 Volts, SESDET will transition from high to low. A 10 KΩ pull up resistor is recommended.
4	SRRDY	Session request ready. Open drain output with 0.6V voltage detector. When the OUT pin rises above the detected Voltage (0.6 V), it will transition from low to high state. Similarly, when the output falls below 0.6 Volts, SRRDY will transition from high to low. A 10 KΩ pull up resistor is recommended.
5	OUT	Power output to VBUS
6	C1+	Flying Capacitor 1 + terminal
7	C1-	Flying Capacitor 1 - terminal
8	NC	No Connect
9	OUTCP	Charge pump output. Requires 1µF bypass capacitor to ground.
10	C2+	Flying Capacitor 2 + terminal
11	C2-	Flying Capacitor 2 - terminal
12	GND	Ground
13	NC	No Connect
14	VIN	Input power supply. Requires 1µF bypass capacitor to ground.
15	SR	Session request input control pin. Should not be left floating. Must connect to high or low. For more details, see table 1.
16	EN	Enable input control pin. When in the low state, AAT3125 is powered down, and consumes small amount of power. When connected high, it is in normal operation. This pin should not be left floating. For more details, see table 1.

Pin Configuration

16 LD 4x4 QFN



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_{IN}, V_{OUT}	Any Pin to GND	-0.3 to 6	V
t_{SC}	OUT short circuit duration	indefinite	s
I_{OUT}[(2)]	Output Current	150	mA
T_J	Operation temp. range	-40 to 85	°C
T_S	Storage temp. range	-65 to 150	°C
V_{ESD}	ESD Rating[3] - HBM	2000	V

Notes:
1: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
2: Based on long-term current density limitation.
3. Human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Thermal Information

Symbol	Description	Value	Units
θ_{JA}	Thermal Resistance [4]	50	°C/W
P_D	Maximum Power Dissipation (T_A = 25°C) [5]	2	W

Note 4: Mounted on an FR4 board.
Note 5: Derate 20mW/°C above 25°C.

Electrical Characteristics[1]

V_{IN} = 3.5V; C_{IN} = C_{OUT} = C1 = C2 = 1.0µF; T_A = -40 to 85°C. Unless otherwise noted, typical values are T_A = 25°C

Symbol	Description	Conditions	Min	Typ	Max	Units
Input Power Supply						
V_{IN} operation range			2.9		5.5	V
I_{cc3}	Operating Current SRP	EN = 1, SR = 1, OUT = IN		60	110	µA
I_{cc2}	Operating Current CP	EN = 1, SR = 0		1	3	mA
I_{cc1}	Shutdown Current 1	EN = 0, SR = 1		1	2	µA
I_{cc0}	Shutdown Current 0	EN = 0, SR = 0			1	µA
Output Power Supply						
V_{OUT}	Output Regulation	I_{OUT} = 0	4.6		5.25	V
I_{CCOUT}	Operating Current	EN = 0		7	12	µA
I_{OUT}	Output Current	3.2 ≤ V_{IN} ≤ 5.5V, V_{OUT} > 4.4V	50	65		mA
		3.35 ≤ V_{IN} ≤ 5.5V, V_{OUT} > 4.4V		100		
V_{CS}	Current Sense Trip Level	VCS = I_{OUT} x R_{CS}	40	60	90	mV
Roff	Pull down resistance	EN = 0, SR = 1	700	1000	1500	Ω
I_{SR}	SR Current Pulse	OUT < (IN-1.0v)	5	10	20	mA
Charge Pump						
η	Efficiency	V_{IN} = 3.75V, I_{OUT} = 50mA		90		%
Ts	Soft start time	OUT < 0.1 to OUT > 4.4		100		µs
Fclk	Clock Frequency			750		KHz

Electrical Characteristics[1]

V_{IN} = 3.5V; C_{IN} = C_{OUT} = C1 = C2 = 1.0µF; T_A = -40 to 85°C. Unless otherwise noted, typical values are T_A = 25°C

Symbol	Description	Conditions	Min	Typ	Max	Units
EN, SR						
V_{IL}	Input Threshold Low				0.4	V
V_{IH}	Input Threshold High		1.4			V
$I_{EN(SINK)}$	EN Input Current	V_{IN} = V_{EN} = 5.5V	-1		1	µA
$I_{SR(SINK)}$	SR Input Current	V_{IN} = V_{SR} = 5.5V	-1		1	µA
POK1						
V_{POK1}	POK Trip Threshold	V_{OUT} Rising	3.8	4.0	4.2	V
$V_{POK1(HYS)}$	POK Hysteresis			50		mV
$V_{POK1(OL)}$	POK output voltage	I_{SINK} = 1mA			0.3	V
I_{POK1}	POK Leakage Current	V_{POK} = 5.5, 25°C			100	nA
POK2						
V_{POK2}	POK Trip Threshold	V_{OUT} Rising	4.18	4.4	4.62	V
$V_{POK2(HYS)}$	POK Hysteresis			50		mV
$V_{POK2(OL)}$	POK output voltage	I_{SINK} = 1mA			0.3	V
I_{POK2}	POK Leakage Current	V_{POK} = 5.5, 25°C			100	nA
SESDET						
V_{SD}	SD Trip Threshold	V_{OUT} Rising	1.9	2.0	2.1	V
$V_{SD(HYS)}$	SD Hysteresis			50		mV
$V_{SD(OL)}$	SD output voltage	I_{SINK} = 1mA			0.3	V
I_{SD}	SD Leakage Current	V_{SD} = 5.5, 25°C			100	nA
SRRDY						
V_{SRRDY}	SRRDY Trip Threshold	V_{OUT} Rising	0.4	0.6	0.8	V
$V_{SRRDY(HYS)}$	SRRDY Hysteresis			20		mV
$V_{SRRDY(OL)}$	SRRDY output voltage	I_{SINK} = 1mA			0.3	V
I_{SRRDY}	SRRDY Leakage Current	V_{SRRDY} = 5.5, 25°C			100	nA

Note 1: The AAT3125 is guaranteed to meet performance specification over the -40 to +85°C operating temperature range, and are assured by design, characterization and correlation with statistical process controls.

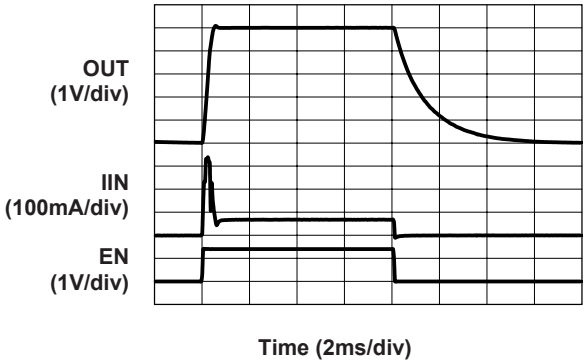
Table 1: Operational States

EN	SR	Charge Pump	Current Source	SRRDY	POK	SESDET	Discharge Resistor
1	0	ON	OFF	ON	ON	ON	OFF
1	1	OFF	ON	ON	ON	ON	OFF
0	0	OFF	OFF	OFF	OFF	ON	OFF
0	1	OFF	OFF	OFF	OFF	ON	ON

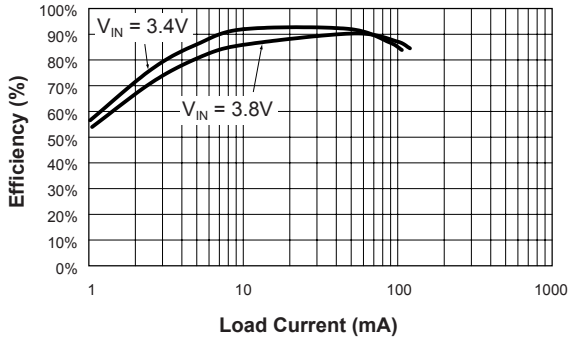
Typical Characteristics

(Unless otherwise noted, V_{IN} = 3.5V, C_{IN} = C_{OUT} = C1 = C2 = 1µF, T_A = 25°C

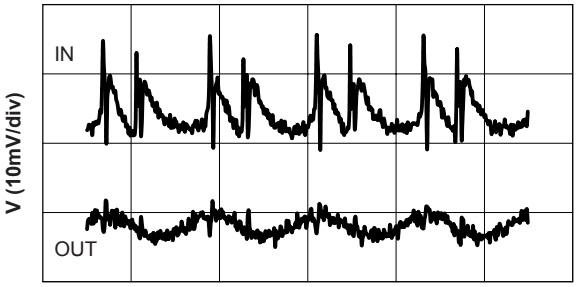
Charge Pump ON/OFF Timing



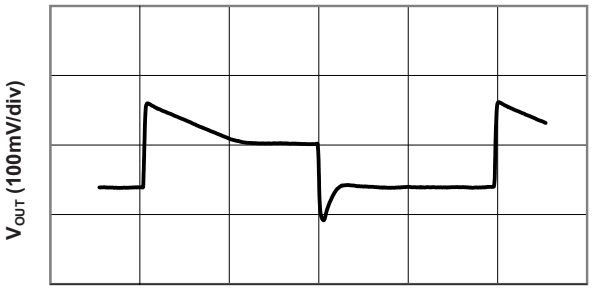
Efficiency vs. Load Current



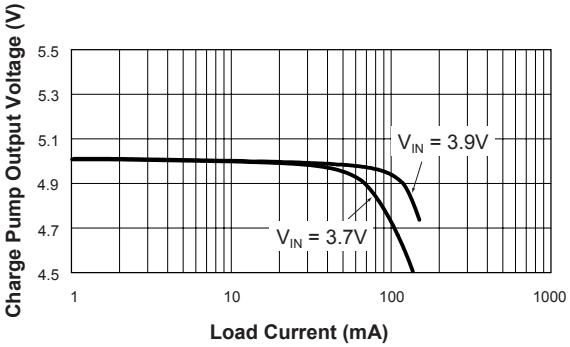
Charge Pump Waveforms
100mA load



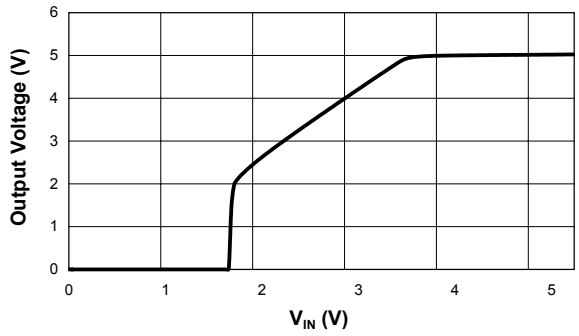
Load Transient Response
10mA to 100mA



Charge Pump Output Voltage
vs. Load Current



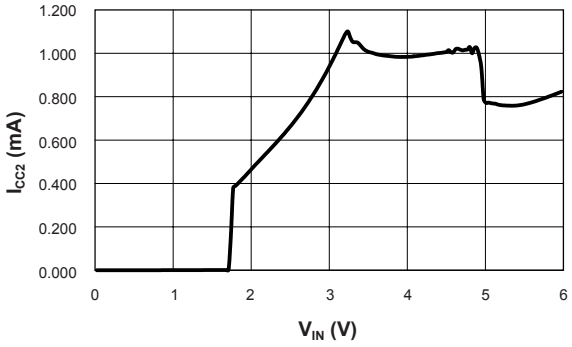
Charge Pump Output Voltage vs. Input Voltage
I_{LOAD} = 100mA



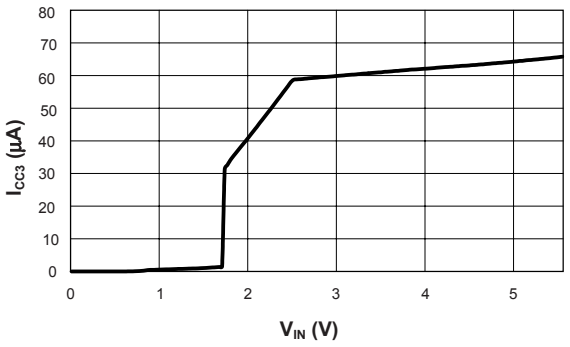
Typical Characteristics

(Unless otherwise noted, V_{IN} = 3.5V, C_{IN} = C_{OUT} = C1 = C2 = 1µF, T_A = 25°C

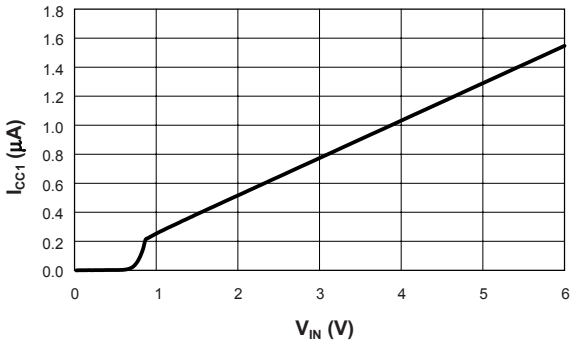
Operating Current vs. Input Voltage
EN = 1, SR = 0 (Charge Pump Mode)



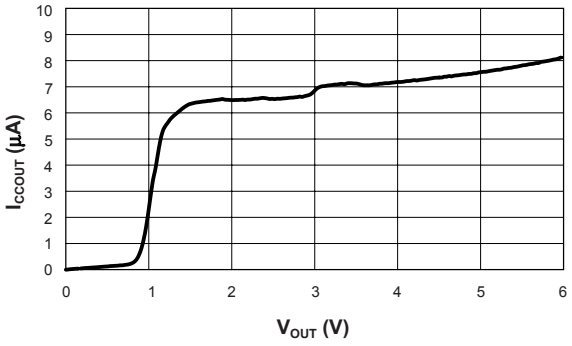
Operating Current vs. Input Voltage
EN = 1, SR = 0 (Outside Current Source Mode)



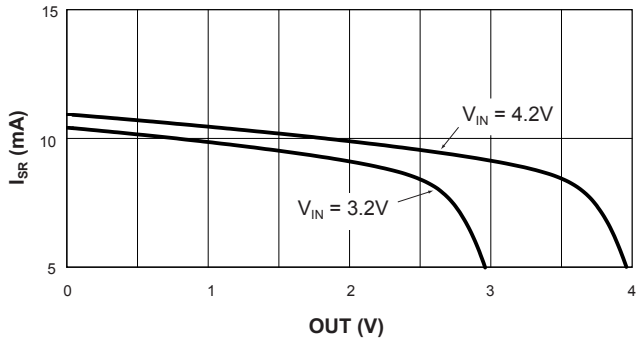
Shutdown Current vs. Input Voltage
EN = 0, SR = 1



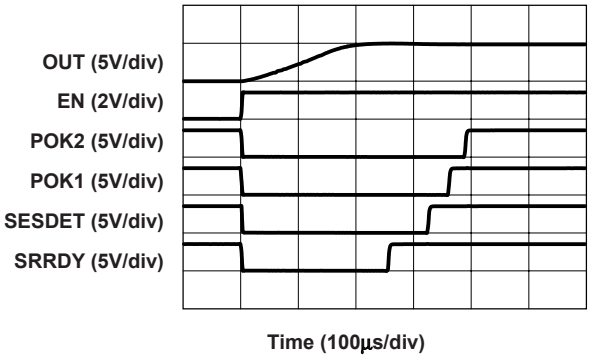
I_{CCOUT} vs. V_{OUT}



I_{SR} vs. OUT
EN = 1, SR = 1



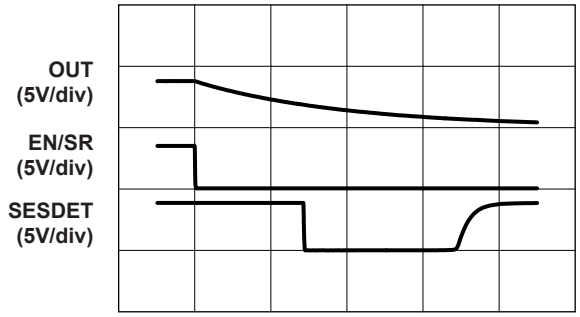
Charge Pump POK Timing



Typical Characteristics

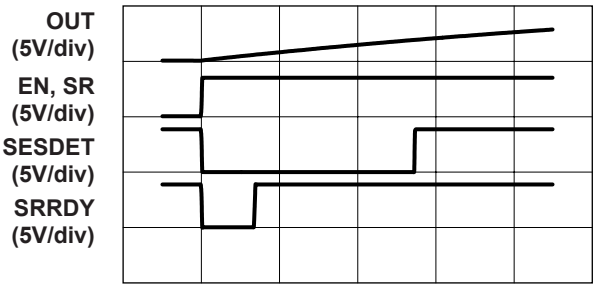
(Unless otherwise noted, V_{IN} = 3.5V, C_{IN} = C_{OUT} = C1 = C2 = 1µF, T_A = 25°C

Falling SESDET Timing



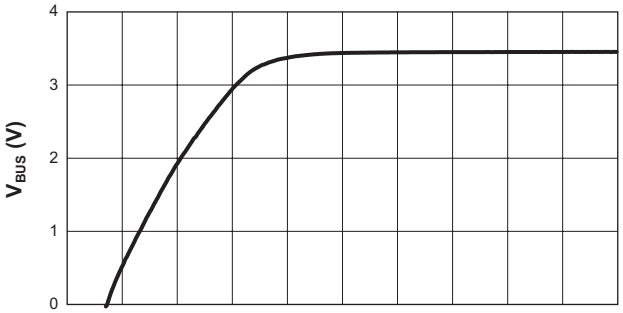
Time (100ms/div)

**Rising SESDET, SRRDY Timing
120µF Load**



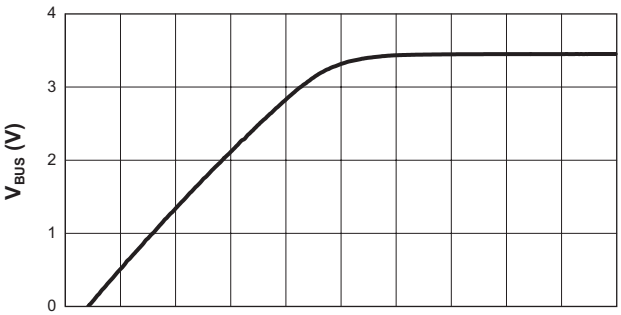
Time (10ms/div)

**V_{BUS} Pulsing for SRP
V_{BUS} Risetime, 5µF on V_{BUS}**



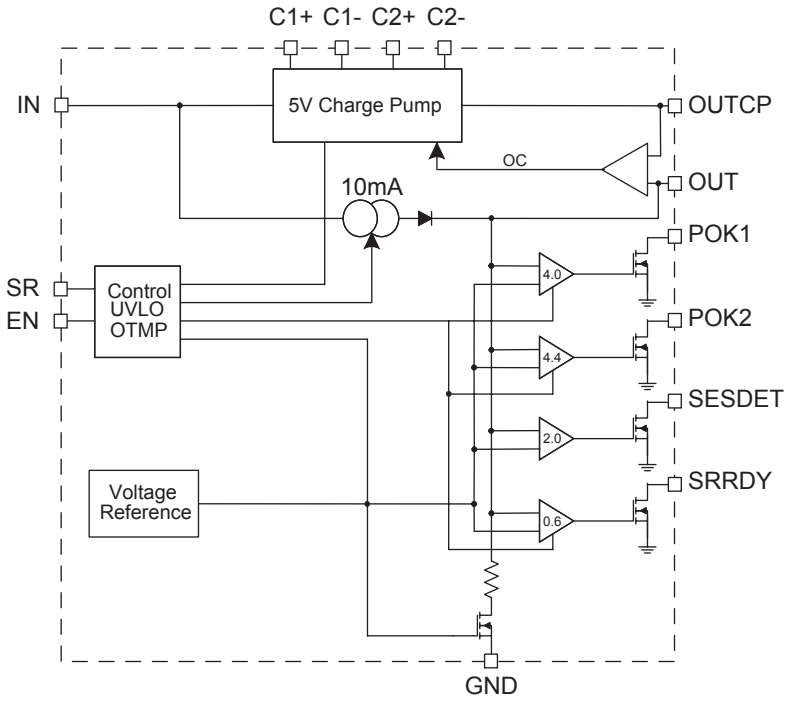
1ms/div

**V_{BUS} Pulsing for SRP
V_{BUS} Risetime, 100µF on V_{BUS}**



10ms/div

Functional Block Diagram



Functional Description

Charge Pump

The charge pump uses a 1.5 X topology - the two flying capacitors are charged in series and discharged in parallel. Using this topology, output current is approximately 2/3 input current. Since the power bus in battery operated devices that use a single cell lithium-ion battery ranges from 3 V to 4.5 V, output voltage above 4.4 V can be maintained. Output voltage is regulated to 5 V and output current is limited by the value of R_{CS}. The charge pump is designed to operate safely with any combination of input and output voltages. Current is not allowed to flow from OUT to IN.

10 mA Current Source

A 10 mA current source supplies current to OUT for VBUS pulsing during SRP. During VBUS pulsing, the length of time needed to charge capacitance connected to OUT distinguishes between non-SRP capable devices and SRP capable devices. Using 10 mA, SESDET should rise about 7 ms after SRRDY rises when an OTG device is connected. With a non-OTG device connected, this period is at least 70 ms. 10 mA should not damage non SRP capable hosts that allow reverse current flow from the bus. Current is not allowed to flow from OUT to IN through the current source.

SESDET (Micro Power Voltage Detector)

The SESDET open drain output signals the use of SRP while the system is acting as the A device. OUT powers this detector because the local 5 V bus may not be powered when the B device initiates SRP. Since VBUS provides no more than 150µA to OUT, the detector consumes only 7µA.

SRRDY Voltage Detector

The SRRDY open drain output signals that VBUS is ready for SRP. SRRDY is powered by IN and is active as long as IN is above the UVLO level. SRRDY is true (low) when OUT is below the SRRDY threshold (0.6V nom). SRRDY is false

(open) when OUT is above the SRRDY threshold or when EN is a logic low. Upon activation by EN, there is no negative glitch that can be mistaken for OUT below 0.8V.

Power OK

USB OTG devices connected as Host must maintain VOUT above 4.4 volts, or report that it is below 4.4 volts. Two Power OK outputs, POK1 and POK2 provide a window comparison of the VOUT voltage. The POK1 open drain output is pulled low if VOUT drops below 4.0V +/- 5%, and the POK2 open drain output is pulled low if VOUT drops below 4.4V +/- 5%.

Under voltage lockout

Circuits other than the micro power voltage detector (SESDET) require voltage to be present on IN. Under voltage lockout (UVLO) guarantees that sufficient voltage is present on IN to insure operation. All functions other than the SESDET flag are disabled if the voltage on IN is less than 2V.

Discharge Resistor

In accordance with the USB OTG specification, a pulldown resistor is provided to discharge VBUS at a current of not more than 8mA.

Over Temperature Protection

If the AAT3125 junction temperature exceeds 125°C, the charge pump is shut down.

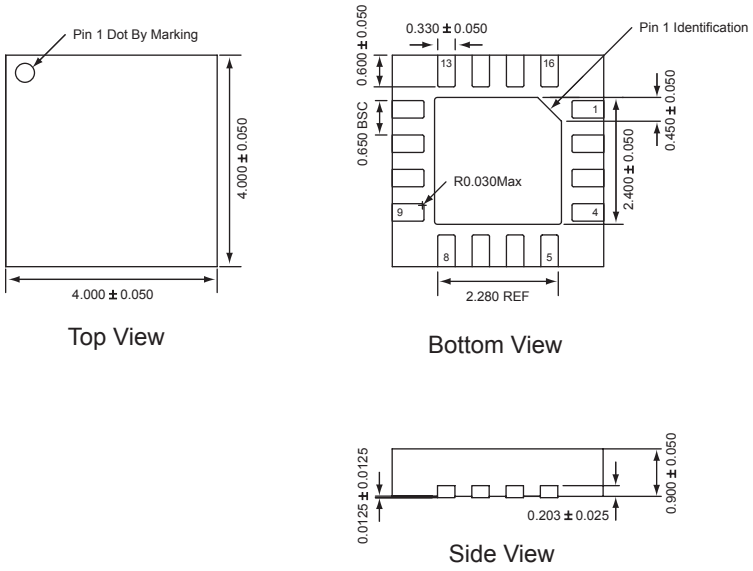
Ordering Information

Package	Marking[1]	Part Number (Tape and Reel)
QFN44-16	ITXYY	**AAT3125ISN-T1**

Note: Sample stock is held on part numbers listed in **bold**.
Note 1: XYY = assembly and date code.

Package Information

QFN44-16



All dimensions in millimeters.

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