PRELIMINARY

BIT MAP LCD DRIVER

■ GENERAL DESCRIPTION

The NJU6455 is a bit map LCD driver to display graphics or characters.

It contains 10,400 bit display data RAM, microprocessor interface circuits, instruction decoder, 128-segment and totally 33-common (32 out of 33-driver can use as both of common and segment) drivers.

The bit image display data is transferred to the display data RAM by serial or 8-bit parallel mode.

33 x 128 dot graphics or 8-character 2-line by 16 x 16 dot character with icon are displayed by NJU6455 itself.

Also, the NJU6455 can extend its display capacity to 33 x 288 dots of graphics or character display by connecting one more NJU6455.

The wide operating voltage like as 2.4 to 5.5V and low operating current are useful to apply small sized battery operated items.

■ PACKAGE OUTLINE

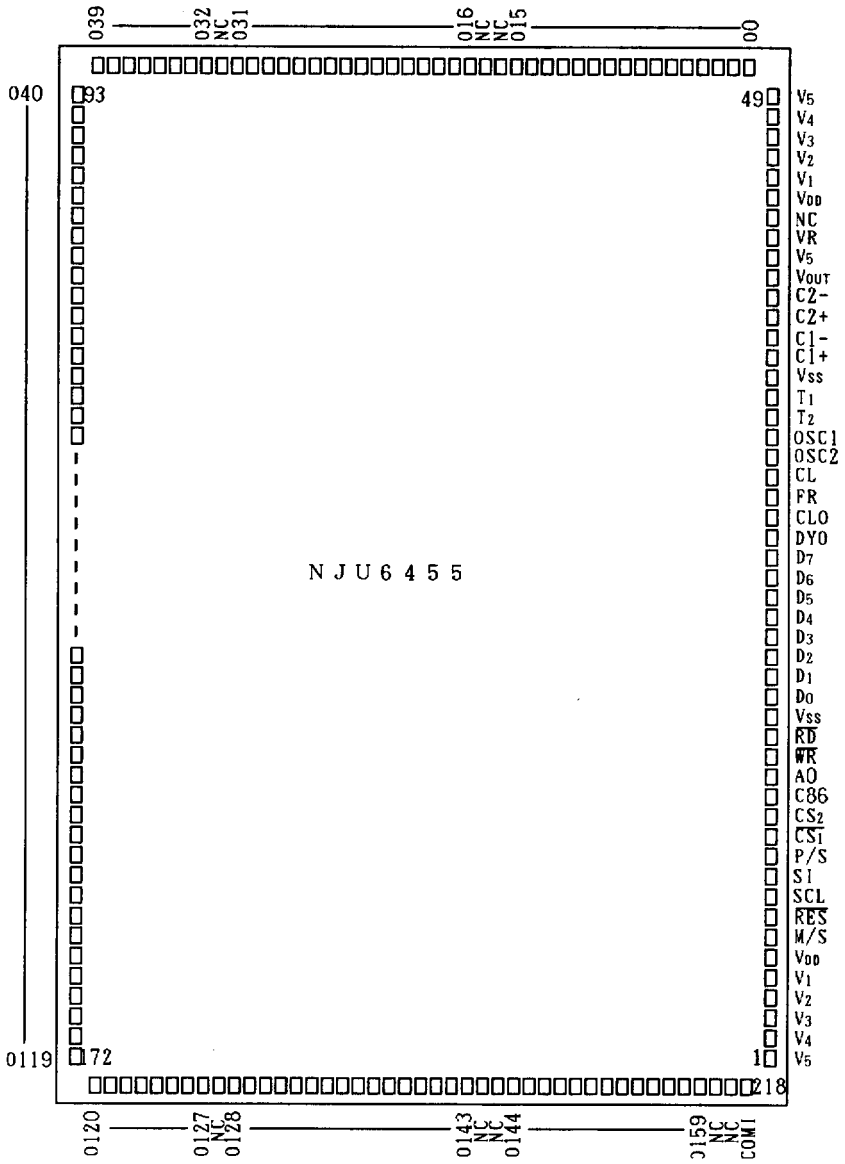
NJU6455C

5

■ FEATURES

- Direct Correspondence between Display Data RAM and LCD Pixel
- Display Data RAM - 10,400 bits
- 160 LCD Drivers - 33 common(32 out of 33 can assign as segment driver) or 128-segment
- Number of Common Driver can select by the Instruction
- Direct Interface with both of 68 and 80 type MPU
- Serial Interface
- Extension Function (can combine with one more NJU6455)
- Programmable Duty Ratio ; 1/32 or 1/33 Duty
- Useful Instruction Set
  Display Data Read/Write, Display ON/OFF Cont, Inverse Display, Page Address Set, Display Starting Line Set, Column Address Set, Status Read, All On/Off, Icon Display, Read Modify Write, Common Driver order Assignment and Power Saving.
- Power Supply Circuits for LCD Incorporated
  Step up Circuits, Regulator, Voltage Follower x 4
- Electrical Variable Resistance
- Low Power Consumption
- Incorporated CR Oscillator
- Operating Voltage --- 2.4V ~ 5.5V
- LCD Driving Voltage --- 6.0V ~ 13.5V
- Package Outline --- Chip / Bumped Chip / TCP
- C-MOS Technology

■ PAD LOCATION



Chip Center	X=0um, Y=0um
Chip Size	X=7.77mm, Y=5.09mm
Chip Thickness	400um ± 30um
Pad Size	40um x 100um
Bump Height	25um TYP.
Bump Material	Au

■ PAD COORDINATES

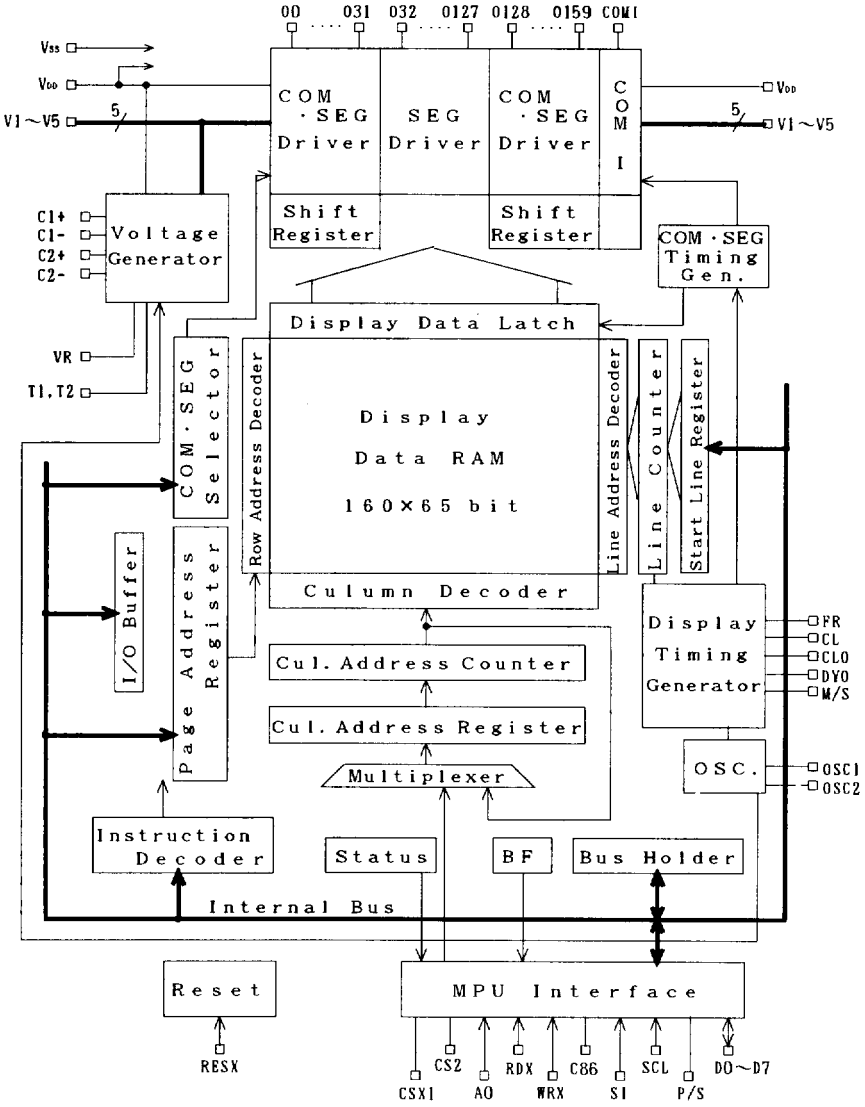
Chip Size 7.33mm x 5.09mm(Chip Center X=0um,Y=0um)

PAD No.	Terminal	X=(μ m)	Y=(μ m)
1	V_5	3335	2327
2	V_4	3196	2327
3	V_3	3057	2327
4	V_2	2918	2327
5	V_1	2778	2327
6	V_{DD}	2639	2327
7	M/S	2500	2327
8	RST	2361	2327
9	SCL	2222	2327
10	SI	2082	2327
11	P/S	1943	2327
12	CS_1	1804	2327
13	CS_2	1665	2327
14	C86	1526	2327
15	A0	1386	2327
16	WR	1247	2327
17	RD	1108	2327
18	V_{SS}	969	2327
19	D_0	830	2327
20	D_1	690	2327
21	D_2	551	2327
22	D_3	412	2327
23	D_4	273	2327
24	D_5	134	2327
25	D_6	-6	2327
26	D_7	-145	2327
27	DYO	-284	2327
28	CLO	-423	2327
29	FR	-563	2327
30	CL	-702	2327
31	OSC_2	-841	2327
32	OSC_1	-980	2327
33	T_2	-1119	2327
34	T_1	-1259	2327
35	V_{SS}	-1398	2327
36	$C1^+$	-1537	2327
37	$C1^-$	-1676	2327
38	$C2^+$	-1815	2327
39	$C2^-$	-1955	2327
40	V_{OUT}	-2094	2327
41	V_5	-2233	2327
42	VR	-2372	2327
43	NC	-2511	2327
44	V_{DD}	-2651	2327
45	V_1	-2790	2327
46	V_2	-2929	2327
47	V_3	-3068	2327
48	V_4	-3207	2327
49	V_5	-3347	2327
50	O_0	-3444	1597
51	O_1	-3444	1517
52	O_2	-3444	1437
53	O_3	-3444	1357
54	O_4	-3444	1277
55	O_5	-3444	1197
56	O_6	-3444	1117
57	O_7	-3444	1037
58	O_8	-3444	957
59	O_9	-3444	877
60	O_{10}	-3444	797
61	O_{11}	-3444	717
62	O_{12}	-3444	637
63	O_{13}	-3444	557
64	O_{14}	-3444	477
65	O_{15}	-3444	397
66	NC	-3444	317
67	NC	-3444	237
68	O_{16}	-3444	157
69	O_{17}	-3444	77
70	O_{18}	-3444	-3
71	O_{19}	-3444	-83
72	O_{20}	-3444	-163
73	O_{21}	-3444	-243
74	O_{22}	-3444	-323
75	O_{23}	-3444	-403
76	O_{24}	-3444	-483
77	O_{25}	-3444	-563
78	O_{26}	-3444	-643
79	O_{27}	-3444	-723
80	O_{28}	-3444	-803
81	O_{29}	-3444	-883
82	O_{30}	-3444	-963
83	O_{31}	-3444	-1043
84	NC	-3444	-1123
85	O_{32}	-3444	-1203
86	O_{33}	-3444	-1283
87	O_{34}	-3444	-1363
88	O_{35}	-3444	-1443
89	O_{36}	-3444	-1523
90	O_{37}	-3444	-1603
91	O_{38}	-3444	-1683
92	O_{39}	-3444	-1763
93	O_{40}	-3146	-2324
94	O_{41}	-3066	-2324
95	O_{42}	-2986	-2324
96	O_{43}	-2906	-2324
97	O_{44}	-2826	-2324
98	O_{45}	-2746	-2324
99	O_{46}	-2666	-2324
100	O_{47}	-2586	-2324
101	O_{48}	-2506	-2324
102	O_{49}	-2426	-2324
103	O_{50}	-2346	-2324
104	O_{51}	-2266	-2324
105	O_{52}	-2186	-2324
106	O_{53}	-2106	-2324
107	O_{54}	-2026	-2324
108	O_{55}	-1946	-2324
109	O_{56}	-1866	-2324
110	O_{57}	-1786	-2324
111	O_{58}	-1706	-2324
112	O_{59}	-1626	-2324
113	O_{60}	-1546	-2324
114	O_{61}	-1466	-2324
115	O_{62}	-1386	-2324
116	O_{63}	-1306	-2324
117	O_{64}	-1226	-2324
118	O_{65}	-1146	-2324
119	O_{66}	-1066	-2324
120	O_{67}	-986	-2324
121	O_{68}	-906	-2324
122	O_{69}	-826	-2324
123	O_{70}	-746	-2324
124	O_{71}	-666	-2324
125	O_{72}	-586	-2324
126	O_{73}	-506	-2324
127	O_{74}	-426	-2324
128	O_{75}	-346	-2324
129	O_{76}	-266	-2324
130	O_{77}	-186	-2324
131	O_{78}	-106	-2324
132	O_{79}	-26	-2324
133	O_{80}	54	-2324
134	O_{81}	134	-2324
135	O_{82}	214	-2324
136	O_{83}	294	-2324
137	O_{84}	374	-2324
138	O_{85}	454	-2324
139	O_{86}	534	-2324
140	O_{87}	614	-2324
141	O_{88}	694	-2324
142	O_{89}	774	-2324
143	O_{90}	854	-2324
144	O_{91}	934	-2324
145	O_{92}	1014	-2324
146	O_{93}	1094	-2324
147	O_{94}	1174	-2324
148	O_{95}	1254	-2324
149	O_{96}	1334	-2324
150	O_{97}	1414	-2324

PAD No.	Terminal	X=(μ m)	Y=(μ m)
151	O 98	1494	-2324
152	O 99	1574	-2324
153	O 100	1654	-2324
154	O 101	1734	-2324
155	O 102	1814	-2324
156	O 103	1894	-2324
157	O 104	1974	-2324
158	O 105	2054	-2324
159	O 106	2134	-2324
160	O 107	2214	-2324
161	O 108	2294	-2324
162	O 109	2374	-2324
163	O 110	2454	-2324
164	O 111	2534	-2324
165	O 112	2614	-2324
166	O 113	2694	-2324
167	O 114	2774	-2324
168	O 115	2854	-2324
169	O 116	2934	-2324
170	O 117	3014	-2324
171	O 118	3094	-2324
172	O 119	3174	-2324
173	O 120	3444	-1763
174	O 121	3444	-1683
175	O 122	3444	-1603
176	O 123	3444	-1523
177	O 124	3444	-1443
178	O 125	3444	-1363
179	O 126	3444	-1283
180	O 127	3444	-1203
181	NC	3444	-1123
182	O 128	3444	-1043
183	O 129	3444	-963
184	O 130	3444	-883

PAD No.	Terminal	X=(μ m)	Y=(μ m)
185	O 131	3444	-803
186	O 132	3444	-723
187	O 133	3444	-643
188	O 134	3444	-563
189	O 135	3444	-483
190	O 136	3444	-403
191	O 137	3444	-323
192	O 138	3444	-243
193	O 139	3444	-163
194	O 140	3444	-83
195	O 141	3444	-3
196	O 142	3444	77
197	O 143	3444	157
198	NC	3444	237
199	NC	3444	317
200	O 144	3444	397
201	O 145	3444	477
202	O 146	3444	557
203	O 147	3444	637
204	O 148	3444	717
205	O 149	3444	797
206	O 150	3444	877
207	O 151	3444	957
208	O 152	3444	1037
209	O 153	3444	1117
210	O 154	3444	1197
211	O 155	3444	1277
212	O 156	3444	1357
213	O 157	3444	1437
214	O 158	3444	1517
215	O 159	3444	1597
216	NC	3444	1677
217	NC	3444	1757
218	COMI	3444	1837

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

No.	Symbol	I/O	Function
6,44	V_{DD}	Power	Power Supply:VDD=5V. Less than 4.5V should be use when voltage tripler using.
18,35	V_{SS}	Power	GND :VSS=0V
5,45 4,46 3,47 2,48 1,49,41	V_1 V_2 V_3 V_4 V_5	Power	LCD Driving Voltage Supplying Terminal. If internal voltage tripler does not use, supply each level from outside maintained following relation. $V_{DD} \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_5$ When M/S="H" and internal power supply are on, internal circuits generated and supply following LCD bias voltage to $V_1 \sim V_4$ terminals. Term. / Volt.: V_1 = V_5 +5.7/6.7V LCD; V_2 = V_5 +4.7/6.7V LCD; V_3 = V_5+2/6.7V LCD; V_4 = V_5+1/6.7V LCD ($V_{LCD} = V_{DD} - V_5$)
36 37 38 39	C1 + C1 − C2 + C2 −	O	Step up capacitor connecting terminals. In case of tripler operation, connect the capacitor between C1 + and C1 −, C2+ and C2−. In case of doubler operation, connect the capacitor between C2 + and C2 −, connect C2+ to C1+, and C1− should be open.
40	V_{OUT}	O	Step up voltage output terminal. Connect the capacitor between this terminal and V_{SS}.
42	VR	I	Voltage adjust terminal. V_5 level is adjusted by external bleeder resistance al connect between V_{DD} and V5 terminal.
34,33	T_1 ,T_2	I	LCD bias voltage control terminals. ※ Don't Care T_1 / T_2 / Step up cir. / Voltage Adj. / V/F Cir.: L / ※ / Available / Available / Available H / L / Not Avail. / Available / Available H / H / Not Avail. / Not Avail. / Available
19 ~ 26	D_0 ~ D_7	I/O	Tri-state bilateral Data I/O terminal when 8-bit parallel operation.
15	A0	I	Connect to the Address bus of MPU. The data on the D_0 to D_7 is distinguished Display data or Instruction by this signal. A0 / Dist.: H = Display Data; L = Instruction
8	$\overline{RES}$	I	Reset terminal. When the $\overline{RES}$ signal goes to "L", the initialization is performed. Reset operation is executing during "L" state of $\overline{RES}$.
12 13	$\overline{CS}_1$ CS_2	I	Chip select terminal. Data I/O is available by following setting. Terminal / State: $\overline{CS}_1$ = "L"; CS_2 = "H"
17	$\overline{RD}$ (E)	I	<When interface with 80 type MPU> $\overline{RD}$ signal of 80 type MPU input terminal. Active"L". During this signal "L", the data bus becomes as output terminal. <When interface with 68 type MPU> Enable clock of 68 type MPU input terminal. Active "H".

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>F u n c t i o n</th></tr>
<tr><td>16</td><td>$\overline{WR}$
(R/$\overline{W}$)</td><td>I</td><td><When interface with 80 type MPU>
Connect the 80 type MPU $\overline{WR}$ signal. Active "L".
The data on the data bus input synchronizing the rise edge of this signal.
<When interface with 68 type MPU>
Read/write control signal of 68 type MPU input terminal.
<table><tr><td>R/$\overline{W}$</td><td>H</td><td>L</td></tr><tr><td>State</td><td>Read</td><td>Write</td></tr></table></td></tr>
<tr><td>14</td><td>C86</td><td>I</td><td>Select the MPU interface type.
<table><tr><td>C86</td><td>H</td><td>L</td></tr><tr><td>Status</td><td>68 Type</td><td>80 Type</td></tr></table></td></tr>
<tr><td>10</td><td>SI</td><td>I</td><td>Serial data input terminal when serial data interface.</td></tr>
<tr><td>9</td><td>SCL</td><td>I</td><td>Serial data clock signal input terminal when serial data interface.
SI data input at the rise edge of SCL in successively. It convert to the parallel data at the 8th SCL clock rise edge.</td></tr>
<tr><td>11</td><td>P/S</td><td>I</td><td>Serial or parallel interface select terminal.
<table><tr><td>P/S</td><td>Chip Select</td><td>Data/Command</td><td>Data</td><td>Read/Write</td><td>Serial CLK</td></tr><tr><td>"H"</td><td>$\overline{CS_1}$,$\overline{CS_2}$</td><td>A_0</td><td>D_0~ D_7</td><td>$\overline{RD}$ 、 $\overline{WR}$</td><td>—</td></tr><tr><td>"L"</td><td>$\overline{CS_1}$,$\overline{CS_2}$</td><td>A_0</td><td>SI</td><td>Write only</td><td>SCL</td></tr></table>*RAM data and status read operation is impossible when select the serial interface.
・ When select the parallel interface (P/S="H"), SI and SCL must be fixed "H" or "L".
・ When select the serial interface (P/S="L"), $\overline{RD}$ and $\overline{WR}$ must be fix "H" or "L", and D_0～ D_7 becomes to the high impedance state.</td></tr>
<tr><td>7</td><td>M/S</td><td>I</td><td>Select the Master or Slave operation.
<table><tr><td>M/S</td><td>H</td><td>L</td></tr><tr><td>State</td><td>Master</td><td>Slave</td></tr></table>The function of oscillator, internal power supply, FR, OSC_1 and OSC_2 change by the M/S setting.
<table><tr><td>Status</td><td>OSC</td><td>Power S</td><td>FR</td><td>OSC_1</td><td>OSC_2</td></tr><tr><td>Master</td><td>Available</td><td>Available</td><td>Out</td><td>In</td><td>Out</td></tr><tr><td>Slave</td><td>Not Avail</td><td>Not Avail</td><td>In</td><td>NC</td><td>In</td></tr></table></td></tr>
<tr><td>32
31</td><td>OSC_1
OSC_2</td><td>I
I/O</td><td>Oscillator Resistance connecting terminals.
・ In case of Master mode operation
Oscillation resistance Rf connecting between OSC_1 and OSC_2.
OSC_2 is output terminal of internal oscillator.
・ In case of slave mode operation.
OSC_2 is a input terminal of the oscillation signal.
OSC_1 must be open.
*Fix the CL terminal to V_{SS} level when use internal oscillator for display clock.</td></tr>
</table>

5

No.	Symbol	I/O	Function
30	CL	I	Display clock input terminal. This signal latch the display data. The line counter increment at the rise edge and the LCD waveform renew at the fall edge. *When the display clock input from outside, fix the OSC_1 terminal to V_{DD} and the OSC_2 terminal to V_{SS}. then reset by $\overline{RES}$ signal.
28	CLO	O	Display clock output terminal. Display clock output only in Master mode. In case of slave mode, this terminal put on high impedance state.
29	FR	I/O	Alternate signal for LCD input/output terminal. If the two NJU6455 using as a master and slave, connect both FR terminal each other. M/S: H = Output, L = Input FR: H = Output, L = Input
27	DYO	O	Common timing synchronization signal output terminal. Connect to DIO terminal each other.
50 ~ 65	O_0 ~ O_{15}	O	LCD drive output terminals. • Both as a Common and Segment output terminals : O_0 to O_{31}, O_{128} to O_{159} • Segment exclusive output terminals : O_{32} to O_{127} *Common or Segment in Common and Segment output terminals is set by the instruction. • Segment output terminal Segment driving output terminals. The following output voltage is selected by combination of FR and data in the RAM.
68 ~ 83	O_{16} ~ O_{31}		
85 ~ 180	O_{32} ~ O_{127}		
182 ~ 197	O_{128} ~ O_{143}		
200 ~ 215	O_{144} ~ O_{159}		

RAM Data	FR	Output Voltage: Normal	Output Voltage: Reverse
H	H	V_{DD}	V_2
	L	V_5	V_3
L	H	V_2	V_{DD}
	L	V_3	V_5

• Common Output Terminal
Common driving output terminals. The following output voltage is selected by combination of FR and common scanning data.

Scan data	FR	Output Voltage
H	H	V_5
	L	V_{DD}
L	H	V_1
	L	V_4

No.	Symbol	I/O	Function
210	COMI	O	Icon common exclusive output terminal. Icon common exclusive output when Icon Display instruction execution. State: Icon Display ON = COM_{32}, Icon Display OFF = V_1 or V_4

(Terminals 43, 66, 67, 84, 181, 198, 199, 216, 217 are NC)

■ Functional Description

(1) Description for each blocks

(1-1) Busy Flag (BF)

When the internal circuits are in the operation mode, the busy flag(BF) is "1", and any instruction except the status read are inhibited.
The busy flag output from D_7 terminal when status read instruction is executed.
If enough cycle time over than t_{cyc} is kept, no need to check the busy flag and it realized high performance for the MPU.

(1-2) Display Start Line Register

The Display Start Line Register is a pointer register which indicate the address in the Display Data RAM corresponded with COM_0 (normally it display the top line in the LCD Panel). This register can use for scroll the screen, change the display page and so on. The Display Start Line Set instruction set the display start address of the Display Data RAM represented in 6-bit to this register. When Icon Display Instruction is executed, the icon display RAM address set automatically as a last display line as shown in Fig. 1. During Icon Display Instruction do not executed, the icon display RAM address do not selected.

(1-3) Line Counter

The Display Start Address stored in the Display Start Line Register is set to the Line Counter when the FR signal changing. The Line Counter count up by synchronizing common signal cycle and generate the line address which addressing the read out line of Display Data RAM.

5

(1-4) Column Address Counter

The column address counter is 8-bit presettable counter which addressing the column address as shown in Fig. 1. This counter increments (+1) up to $(A0)_H$ when the Display Data Read/Write instruction is executed.
The count up is stop at $(A0)_H$, do not count up non existing address of over than $(A0)_H$ by the count lock function. This count lock is released by new column address set.
Furthermore, this counter is independent with the Page Register.
By the Address Inverse Instruction, the column address decoder inverse the column address of Display Data RAM correspondence to the Segment Driver.

(1-5) Page Register

This register gives page address of Display Data RAM as shown Fig. 1. When the MPU access the data by changing the page, the page address set instruction is required. Page address "8"(D3="H" and D2=D1=D0="L") is Icon exclusive RAM area, the data only for the D0 is valid.

(1-6) Display Data RAM

Display Data RAM consists of 10,400 bits stores the bit image display data (each bit correspond to the each pixel so called bit map method). The each bit in the Display Data RAM correspond to the each dot of the LCD panel and control the display by following bit data.

When Normal Display : On="1" , Off="0"
When Inverse Display : On="0" , Off="1"

The Display Data RAM output 160-bit parallel data addressed by the line counter, and these data ares set into the Display Data Latch.
This RAM and MPU are operating independently, therefore, there is no influence by the unsynchronize rewriting.
The relation between column address and segment output can inverse by the Address Inverse Instruction ADC as shown in Fig. 1.

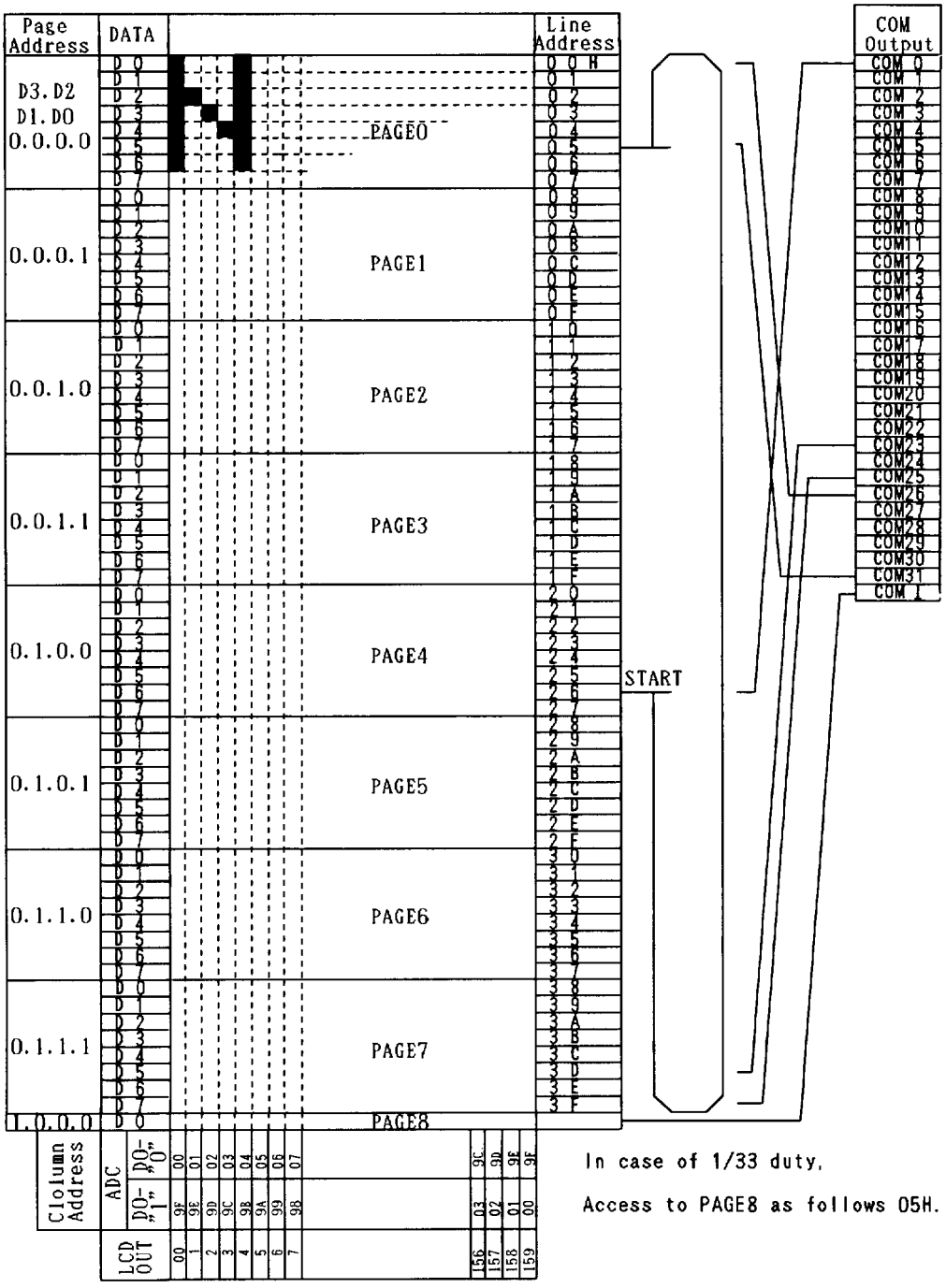


Fig.1 Correspondence with Display Data RAM and Address
(For example the Display start line is 26th)

(1-7) Common and Segment Driver Assignment

NJU6455 incorporates 160 LCD driver and 1 Icon exclusive LCD driver. For easy assembly, 64 LCD driver ca n assign as both of Common and Segment driver and 96 LCD drivers are fixed as a segment driver.

Can assign as both of Common and Segment Driver — O_0 to O_{31} and O_{128} to O_{159}

Assign only to Segment Driver — O_{32} to O_{127}

When the Output Assignment Register Set instruction which select one assignment from case 1 to case 4, is e xecuted, each LCD driver is fixed its function automatically as shown below table 1;

Table 1

ADC (D_0)			
L	0 →	→ 159	
H	159 ←	Column Address	← 0
	Display Data RAM		

Case	Status Register				LCD Driver Assignment									
	D_3	D_2	D_1	D_0	O_0	O_{15}	O_{16}	O_{31}	O_{32}	O_{127}	O_{128}	O_{143}	O_{144}	O_{159}
1	0	*	1	1	COM_{31} ← COM_0				SEG_{128}					
	1	*	1	1	COM_0 → COM_{31}				SEG_{128}					
2	0	*	1	0	SEG_{128}						COM_0 → COM_{31}			
	1	*	1	0	SEG_{128}						COM_{31} ← COM_0			
3	0	*	0	1	COM_{15} ← $_0$				SEG_{128}				COM_{16} → $_{31}$	
	1	*	0	1	COM_{16} → $_{31}$				SEG_{128}				COM_{15} ← $_0$	
4	*	*	0	0	SEG_{160}									

(* : Don't Care)

5

Though the MCU can access to whole column address space of the Display RAM, but the column address are a which assign as the Common Driver can not to use for the data display area, or, display(segment) data store d address must be control by the MCU software. Icon display is regardless with this function, therefore Icon D isplay Instruction must be executed when Icon display needed. In this time, the Icon display Driver COM_1 is fi xed to COM_{32} regardless the other Common Driver assignment. Case1 through Case4 is selected by setting the lower two bits of D_0 and D_1, and the Common Driver scanning order is also set by "1", or "0" written int o D_3 in same time.

Master/Slave operation and LCD Driver assignment function are independent completely, therefor in the multi-c hip application the Common driving function can assign either one of Master or Slave chip.

(1-8) Reset Circuits

The NJU6455 performs following initialization when the RST input is put on the "L" level.

Initialization

① Display Off
② Normal Display(Non-inverse display)
③ Icon Display Reset
④ ADC Select : Normal (ADC Instruction D0="1")
⑤ Read Modify Write Mode Off
⑥ Internal Power supply(Step up) circuits Off
⑦ Clear the serial interface register
⑧ Set the 1st line to the Display Start Register
⑨ Set the address $(00)_H$ to the Column Address Counter
⑩ Set the page "0" to the Page Address Register
⑪ Select the Case 4 of the LCD Driver Assignment
⑫ Set the EVR register to $(00)_H$

The $\overline{RES}$ terminal connect to the Reset terminal of MPU to reset at same time as shown in "MPU Interface Ex ample". The reset signal require over than 10us $\overline{RES}$="L" level input as shown in "Electrical Characteristics". After 1us from the rise edge of $\overline{RES}$ signal, the normal operation is starting.

In case of the internal power supply(Step up) circuits do not use, the $\overline{RES}$ terminal must be "L" when external power supply turn on. $\overline{RES}$="L" input reset internal register and set above default, but oscillation circuits and output terminals like as OSC2, FR, CLO, DYO, and D0 through D7 are no influence.
No initialization by $\overline{RES}$ when power turns on, will make Hung up condition, therefore please initialize by the $\overline{RES}$ when power turns on. By the reset Instruction performs only ⑧ through ⑫ mentioned in above.
The noise into the $\overline{RES}$ terminal should be cared when of the application design to avoid the error function.

(1-9) LCD Driving

(a) LCD Driving Circuits
NJU6455 incorporate 160 LCD Drivers like as 96 Segment exclusive drivers, 64 both of Common and Segment drivers and 1 Icon exclusive driver. Both of Common and Segment drivers incorporate the shift register which scan the common display signal. The combination among the Display data, COM scan signal and FR signal define the LCD driving output voltage. The output wave form is mentioned in the Fig. 7.

(b) Display Data Latch Circuits
Display Data Latch stores 160-bit of one line display data for each common cycle which read out from the Display Data RAM temporary and transfer this data to the LCD Driver. The Display On/Off and Static Drive On/Off controls the latched data only, therefore, the data in the Display Data RAM is no change and keep on remaining.

(c) Line Counter and Latch signal of Latch Circuits
The clock for Line Counter and latch signal for the Latch circuits are generated from display clock(CL). The line address is renewed by synchronizing with display clock and 160 bits display data are latched into display latch circuits synchronizing with display clock then output to the LCD driving circuits. The display data transfer to the LCD driving circuits is executed independently with RAM access by the MPU.

(d) Display Timing Generator
This Generator generates the timing signal for the display system by combination of the master clock and Driving Signal FR. The Frame Signal FR has a function to generate the 2 frame alternative driving method wave form for the LCD panel, and synchronizing the line counter and common timing generator to the master LSI. Therefore, the FR signal must be 50% duty ratio clock signal which synchronized with the frame signal. When NJU6455 use as a slave, the FR terminal change to the input terminal.

(e) Common Timing Generation
The common timing and Common synchronizing signal(DYO) is generated by display clock. And the divided signal of oscillation signal is output from CLO terminal. The DYO output "H" pulse just one display clock before to the synchronized signal (FR) changing(refer to Fig.2). The DYO outputs regardless the Master or Slave. When the Slave selection, the duty setting must be adjust to the Master. In case of the Multi-chip application, the FR signal must supply from Master chip. The status of FR, CLO, and DYO are as follows;

Table 2

Ope. Mode	FR	CLO	DYO
Master	Output	CL Out	Output
Slave	Input	HZ	Output

* HZ indicate High impedance state.

· Waveform of Display Timing

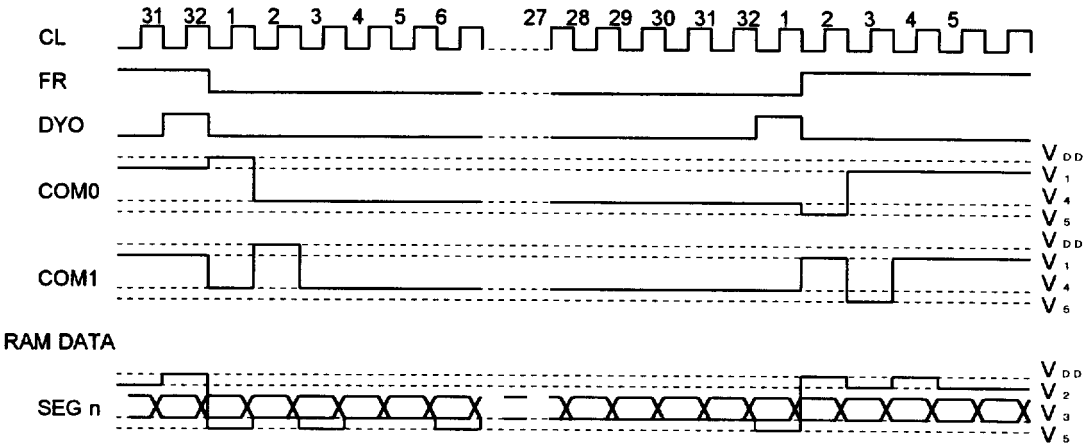


Fig. 2

(f) Oscillation Circuits

The Oscillation Circuits which required external oscillating resistance Rf, is a low power CR oscillator and it is used for display timing signal source, the clock for step up circuits for LCD driving. The oscillation is available only for the Master operation. When the oscillation signal use for the display clock, connect the CL terminal to V_{SS}. In case of the oscillation circuits do not use, connect the OSC_1 to V_{DD}, OSC_2 to the V_{SS}. The oscillation circuits output divided by 8 and output from CLO terminal as a display clock.

5

(g) Power Supply Circuits

Internal Power Supply Circuits generate the High voltage and Bias voltage which required by the LCD. The power Supply Circuits consist of Step up(Tripler or Doubler) Circuits, Regulation Circuits, and Voltage Follower. Though the internal Power Supply designed for small size LCD panel, therefore it will not use for the multi-chip or large size LCD panel application. If the contrast is no good in those application, please use external power supply supplied more high current.

The suitable values of the capacitors connecting to the V1 to V5 terminals, the step up circuit and the feedback resistors for V5 operational amplifier depend on the LCD panel. And the power consumption in the LCD panel is changeable with the display patarn. Therefore a trial with actual module should be practiced.

The operation of internal Power Supply Circuits is controlled by the Internal Power Supply On/Off Instruction. When the Internal Power Supply Off Instruction is executed, all of the step up circuits, regulation circuits, voltage follower circuits are off. In this time, the bias voltage of V_1, V_2, V_3, V_4, and V_5 for the LCD supply from outside, terminals $C1^+$, $C1^-$, $C2^+$, $C2^-$,and VR are open. The status of internal power supply can select by T_1 and T_2 terminal. The external power supply can be used together with some of internal power supply function.

Table 3. (※ Don't Care)

T1	T2	Step up	Voltage Adj.	Buffer (V/F)	Ext. Pow Supply	C1+,C1-,C2+,C2-	VR Term
L	※	O	O	O	-		
H	L	×	O	O	V_{OUT}	OPEN	
H	H	×	×	O	$V_5=V_{OUT}$	OPEN	OPEN

When (T_1, T_2)=(H, L), the terminal for step up circuits of $C1^+$,$C1^-$ $C2^+$,$C2^-$ are open due to the step up circuits doesn't work and supply the LCD driving voltage to the V_{OUT} terminal from outside. And in case of (T_1, T_2)=(H, H), terminals for step up circuits and VR are open, and supply the LCD driving voltage from outside due to the Step up circuits and Voltage adjust circuits are stop its operation.

(2) Instruction

The NJU6455 distinguish the signal on the data bus by combination of A0 and R/W($\overline{RD}$,$\overline{WR}$). Normally, the busy check is not required as the NJU6455 is operating so first because of the decode of the instruction and execution are performs only depend on the internal timing which not depend on the external clock. In case of serial interface, the data input from D_7 terminal serially.

The Table. 4 shows the instruction codes of the NJU6455.

Table 4. Instruction Code

	Instruction	Code A0	$\overline{RD}$	$\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Description
(1)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD Display ON/OFF 0:OFF 1:ON
(2)	Display Start Line Set	0	1	0	0	1	Display Start Address						Determine the Display Line Correspond to the COM_0
(3)	Page Address Set	0	1	0	1	0	1	1	Page Address				Set the page of DD RAM to the Page Add. Register
(4)	Column Address Set High Order 4bit	0	1	0	0	0	0	1	High Order Column Add.				Set the Higher order 4 bits Column Address to the Reg.
(5)	Column Address Set Lower Order 4bit	0	1	0	0	0	0	0	Lower order Column Add.				Set the Lower order 4 bits Column Address to the Reg.
(6)	Status Read	0	0	1	Status				0	0	0	0	Read out the internal Status
(7)	Write Display Data	1	1	0	Write Data								Write the data into the Display Data RAM
(8)	Read Display Data	1	0	1	Read Data								Read the Data from the Display Data RAM
(9)	ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	Set the DD RAM vs Segment 0:Normal 1:Inverse
(10)	Normal or Inverse of On/Off Set	0	1	0	1	0	1	0	0	1	1	0 1	Inverse the On and Off Display 0:Normal 1:Inverse
(11)	Whole Display On	0	1	0	1	0	1	0	0	1	0	0 1	Whole Display Turns On 0:Normal 1:Whole Disp. On
(12)	Icon Display	0	1	0	1	0	1	0	1	0	1	0 1	Set the Duty Ratio 0:No Icon 1:With Icon
(13)	Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increment the Column Add. Register when writing but no-change when reading
(14)	End	0	1	0	1	1	1	0	1	1	1	0	Release from the Read Modify Write Mode
(15)	Reset	0	1	0	1	1	1	0	0	0	1	0	Initialize the internal Circuits
(16)	Output Assignment Register Set	0	1	0	1	1	0	0	Assignment Data				Set the COM and SEG driver assignment to the Register
(17)	Internal Power Supply On/Off	0	1	0	0	0	1	0	0	1	0	0 1	0:Int. Power Supply Off 1:Int. Power Supply On
(18)	LCD Driving Voltage Set	0	1	0	1	1	1	0	1	1	0	1	Set LCD Driving Voltage after the internal(external) power supply is turned on
(19)	EVR Register Set	0	1	0	1	0	0	0	Setting Data				Set the V5 output level to the EVR register
(20)	Power Save (Dual Command)	0 0	1 1	0 0	1 1	0 0	1 1	0 0	1 0	1 1	1 0	0 1	Set the Power save Mode

5

(3) Explanation of Instruction Code

(a) Display On/Off

This instruction executes whole display On/Off no relation with the data in the Display Data RAM and internal c onditions.

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	0	1	0	1	1	1	D

D 0: Display Off
1: Display On

(b) Display Start Line

This instruction set the line address as shown Fig. 1. The selected line in the Display Data RAM correspo nd to the COM_0 which display at the top of LCD panel The display area is set automatically from the selecte d line to the line which increase the number of duty ratio. Therefore, the smooth scroll for vertical direction by changing the start line address on by one or page switching are available by this instruction.

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	0	1	A_5	A_4	A_3	A_2	A_1	A_0

A_5	A_4	A_3	A_2	A_1	A_0	Line Address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
		.				.
		.				.
1	1	1	1	1	0	3E
1	1	1	1	1	1	3F

(c) Page Address Set

When MPU access the Display Data RAM, the page address corresponded to the row address must be select ed. The access in the Display Data RAM is available by setting the page and column address(Refer the Fig. 1.). The display is no influence by changing the page addressed. Page 8 is a Icon display data area which a vailable only for the D_0.

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	0	1	1	A_3	A_2	A_1	A_0

A_3	A_2	A_1	A_0	Page
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

(d) Column Address

When MPU access the Display Data RAM, page address set(refer(c) in front page) and column address set are required before the data writing. The column address set performs twice address setting of higher order 4 bits and lower order 4 bits. When the MPU access the Display Data RAM continuously, the col umn address increase "1" automatically, therefore, the MPU can access the data only without address setting. After writing 1page data ,page address setting is required due to page address doesn't increase automatically.

The increment of the column address is stopped by the address of $(A0)_H$ automatically, but the page address is no change even if the column address increase to $(A0)_H$ and stop. In this time the page address i s no change.

	A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
Higher Order	0	1	0	0	0	0	1	A_7	A_6	A_5	A_4
Lower Order	0	1	0	0	0	0	0	A_3	A_2	A_1	A_0

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Column Address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
				.				.
				.				.
1	0	0	1	1	1	1	1	9F

(e) Status Read

This instruction read out the internal status of "BUSY", "ADC", "ON/OFF" and "RESET".

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY : BUSY=1 indicate the operating or the Reset cycle.
The instruction can be input after the BUSY status change to "0".

ADC : Indicate the output correspondence of column(segment) address and segment driver.
0 :Counterclockwise Output(Inverse) Column Address 160-n ←→ Segment Driver n
1 :Clockwise Output (Normal) Column Address n ←→ Segment Driver n
(Note) The data "0=Inverse" and "1=Normal" of ADC is inverted with the ADC select Instruction of "1=Inverse" and "0=Normal".

ON/OFF : Indicate the whole display On/Off status.
0 : Whole Display "On"
1 : Whole Display "Off"
(Note) The data "0=On" and "1=Off" of Display On/Off status read out is inverted with the Display On/Off instruction data of "1=On" and "0=OFf".

RESET : Indicate the initialization period by RST signal or reset instruction.
0 : —
1 : Initialization Period

(f) Write Display Data

This instruction write the 8-bit data on the data bus into the Display Data RAM. The column address increase "1" automatically when writing, therefore, the MPU can write the 8-bit data into the Display Data RAM without any address setting after the start address setting.

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	WRITE DATA							

(g) Read Display Data

This instruction read out the 8-bit data from Display Data RAM which addressed by the column and page addr ess. The column address increase "1" automatically when reading, therefore, the MPU can read the 8-bit data from the Display Data RAM without any address setting after the start address setting. One time of dummy r ead is required after column address set as explain in "(5-5) Access to the Display Data RAM and Internal Reg ister". In the serial interface mode, the display data can not be readout.

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	READ DATA							

(h) ADC Select

This instruction set the correspondence of column address in the Display Data RAM and segment driver outp ut. (See Fig. 1.) By this instruction, the order of segment output can be changed by the software, and no res triction of the LSI placement against the LCD panel.

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	0	1	0	0	0	0	D

D 0: Clockwise Output (Normal)
1: Counterclockwise Output (Inverse)

(i) Normal or Inverse On/Off Set

This instruction set the normal or inverse turn on and turn off for whole display. The contents of Display Data RAM is no changed by this instruction execution.

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	0	1	0	0	1	1	D

D 0: Normal RAM data "1" correspond to "On"
1: Inverse RAM data "0" correspond to "On"

(j) Whole Display On

This instruction executes the all pixel terns on regardless the contents of the Display Data RAM. In this time, t he contents of Display Data RAM is no change and is kept. This instruction takes over precedence over the " Normal or Inverse On/Off Set Instruction".

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	0	1	0	0	1	0	D

D 0: Normal Display
1: Whole Display turns on

When Whole Display On Instruction is executed in the Display Off status, the internal circuits put on the power save mode(refer to the (s) Power Save) .

(k) Icon Display

This instruction set the 1/33 duty for the Icon Display. The COMI terminal operate as COM $_{32}$ and output the icon display data stored in D $_0$ of Display Data RAM page 8(refer to the Fig. 4). The icon display in the multi -chip operation of NJU6455, both of master and slave chip must be set this instruction.

A0	$\overline{RD}$	R/$\overline{W}$	D $_7$						D $_0$
0	1	0	1	0	1	0	1	0	1	D

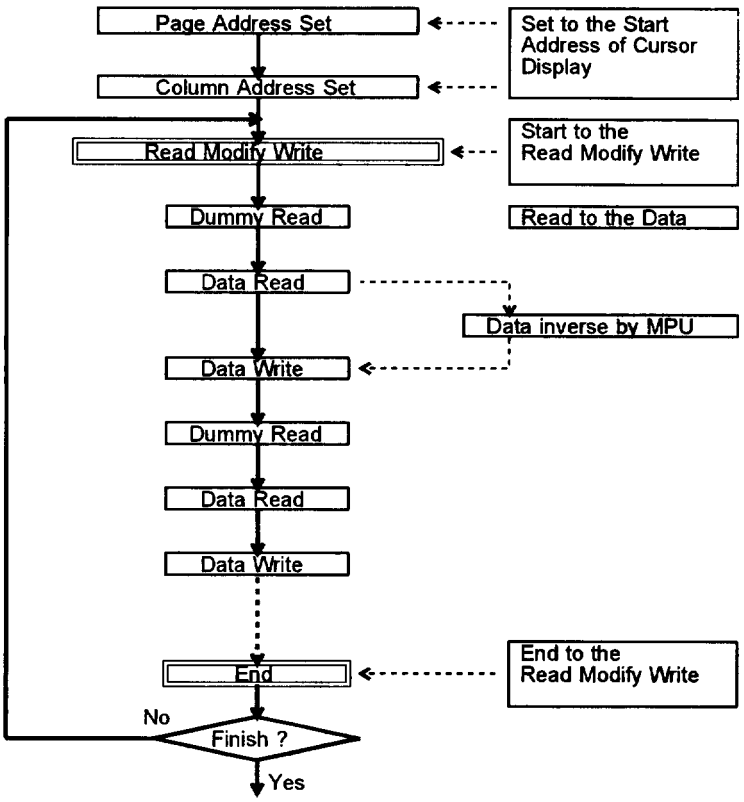
(l) Read Modify Write

This instruction set the Read Modify Write Mode which performs the column address increment. During the R ead Modify Mode, the column address increase "1" automatically when the Display Data Write Instruction is e xecuted, but the address is no change when the Display Data Read Instruction is executed. This status is co ntinued during End instruction execution. When the End instruction is entered the column address back to the address where the Read Modify Write instruction entering. By this function, the load of MPU for example cyc lic data writing operation like as cursor blink etc., can be reduced.

A0	$\overline{RD}$	R/$\overline{W}$	D $_7$						D $_0$
0	1	0	1	1	1	0	0	0	0	0

Note) During the Read Modify Write mode, any instruction except Column Address Set can be executed.

(m) Sequence of inverse display

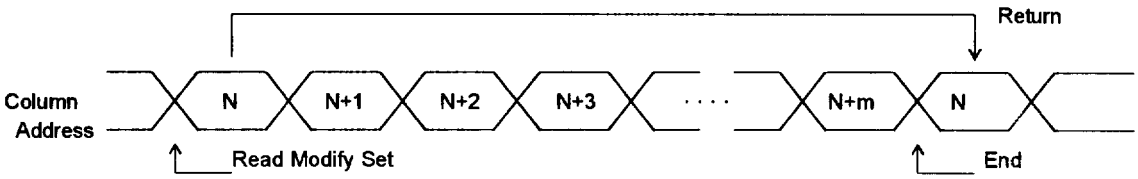


5

(n) End

This instruction release the Read Modify Write mode and the column address back to the address where the r ead modify write mode setting.

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	1	1	0	1	1	1	0



(o) Reset

This instruction executes the following initialization.

Initialization

① Set the 1st line in the Display Start Line Register.
② Set the Address $(00)_H$ to the Column Address Counter.
③ Set the page 0 to the Page Register.
④ Set the case 4 of Output Assignment
⑤ Set $(00)_H$ to the EVR Register for the contrast control

In this time, there are no influence to the Display Data RAM.

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	1	1	0	0	0	1	0

The reset signal input to the $\overline{RES}$ terminal must be required for the initialization when the power terns on. Su bstitution of Reset Instruction for the reset signal input to the $\overline{RES}$ terminal is not allowed.

(p) Output Assignment Register

This instruction set the function both of common and segment terminal and its assignment by the A_0 and A_1. And the bit A_3 set the Common Driver scanning order as explain in "(1-7) Common and Segment Driver As signment" of Functional Description.

A0	$\overline{RD}$	R/$\overline{W}$	D_7							D_0
0	1	0	1	1	0	0	A_3	A_2	A_1	A_0

A_3 : Set the Common Driver scanning order

A_2	A_1	A_0	Status	Number of COM and SEG
*	0	0	Case4	SEG $_{160}$
*	0	1	Case3	SEG $_{128}$,COM $_{32}$
*	1	0	Case2	
*	1	1	Case1	

(*:Don't Care)

For more detail, Please refert o the explanation of (1-7) "Common and Segment output assignment.

(q) Internal Power Supply

This instruction set the internal Power Supply On/Off. Step up circuits, Voltage Regulator and Voltage Followe r are activated when set the On. To operate the step up circuits, the operation of oscillation circuits is require d.

A0	$\overline{RD}$	R/$\overline{W}$	D_7						D_0
0	1	0	0	0	1	0	0	1	0	D

D 0: Internal Power Supply Off
1: Internal Power Supply On

The internal Power Supply must be Off when external power supply using. In case of the multi-chip applicatio n of the NJU6455, external power supply is recommended due to the heavy LCD capacitive load.
When the NJU6455 set to the slave chip, the Internal Power Supply should be Off.

(r)LCD Driving Voltage Set

This instruction sets LCD driving voltage V1 ~ V4 and output LCD driving waveform through the COM/SEG termi nals.

A0	$\overline{RD}$	R/$\overline{W}$	D_7						D_0
0	1	0	1	1	1	0	1	1	0	1

(s) EVR Register Set

This instruction set the LCD Display contrast which is controlled by the voltage adjust circuits. When this instr uction execute, the internal Electrical Variable Resistor(EVR) to change the V5 output voltage generate one vol tage state from 16 voltage state. The range of V5 output level can be adjusted by the external resistance. F or more detail, please refer to the "(4)(b) Voltage Adjust Circuits".

A0	$\overline{RD}$	R/$\overline{W}$	D_7						D_0
0	1	0	1	0	0	0	A_3	A_2	A_1	A_0

A_3	A_2	A_1	A_0	V_{LCD}
0	0	0	0	Low
		:		
		:		
1	1	1	1	High

$V_{LCD}=V_{DD}-V_5$

When EVR don't use, set the EVR register to (0, 0, 0, 0).

(t) Power Save(Dual Command)

When both of Display Off and Whole Display On are executed, the internal circuits put on the power save mod e and the operating current is reduced as same as stand by current.
The internal status in the Power Save Mode is as follows;

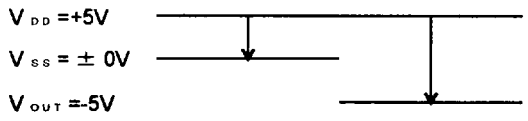
① Stop the Oscillation Circuits and Internal Power Supply Circuits operation.
② Stop the LCD driving. Segment and Common drivers output V_{DD} level.
③ Stop the external clock input. Then the terminal OSC_2 becomes floating status.
④ Keeping the display data and operating mode as before the power save mode.
⑤ All of LCD driving bias voltage fixed to the V_{DD} level.

*1 Power save mode requires dual-instruction. After the second instruction" whole Display ON", the power save mode starts.
*2 In the power save release sequence, the Display ON instruction should be performed after the Normal Display instruction. The power save mode is released after the Normal Display instruction.
*3 Until "LCD driving voltage set" execution, NJU6455 operating current is higher than usual state and all COM/SEG terminals output V_{DD} level continuously except the LCD driving waveform.
*4 In case of external bleeder resistors, cut current on these resistors electrically and fix them to V_{DD} or float them before the power save mode or at the same time. At this time V_{OUT} terminal should be floated or connected to the lowest voltage level of the system.
*5 In case of the external power supply, it should be turned off before the power save mode or at the same time, and V_{OUT} terminal should be floated or connected to the lowest voltage of the system.

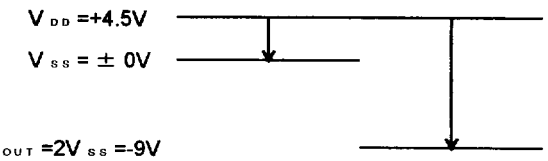
(4) Internal Power Supply

(a) Voltage tripler

Three times negative voltage(V_{DD} common) of the voltage V_{DD} -V_{SS} is output from V_{OUT} terminal when connecting three capacitor between C1 $^{+}$ and C1 $^{-}$, C2 $^{+}$ and C2 $^{-}$, V_{SS} and V_{OUT}. In case of the voltage doubler operation, connect the two capacitor between C2 $^{+}$ and C2 $^{-}$, V_{SS} and V_{OUT}, then connect the C1 $^{+}$ and C2 $^{+}$ terminals. Step up circuits like as Voltage Tripler or Doubler using a oscillation circuits output as its clock signal, therefore, the oscillation circuits operation is required when step up operation. The voltage relation regarding the step up circuits is shown in below. When voltage tripler operation, the operation voltage V_{DD} should be less than 4.5V.



Voltage Relation in Doubler



Voltage relation in Tripler

(b) Voltage Adjust Circuits

The step up voltage of V_{OUT} output from V_5 through the voltage adjust circuits. The output voltage of V_5 is adjusted by changing the Ra and Rb within the range of $|V_5| < |V_{OUT}|$. The output voltage can calculated by the following formula.

$$V_5 = V_{DD} - (1 + Rb/Ra) \cdot V_{REG} \quad \cdots\cdots ①$$

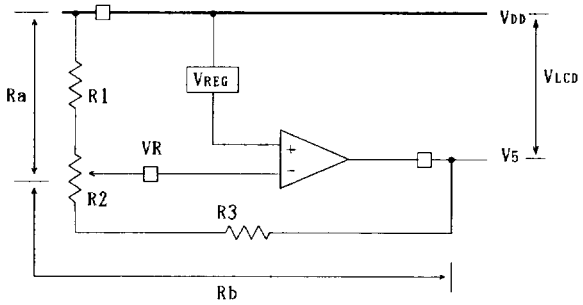


Fig. 3

Where, the V_{REG} is a constant voltage in the NJU6455 like as $V_{REG} \fallingdotseq 2.5$.

To adjust the output voltage from V_5, connect the variable resistance among VR, V_{DD} and V_5 as shown in Fig. 3. When fine tuning for V_5 is needed, combine with the fixed resistance of R1, R3 and variable resistance of R2 is recommended as shown in Fig. 3.

Design example for R1, R2 and R3

- R1+R2+R3=5M Ω (Determined by the current flown between V_{DD} -V_5)
- Variable voltage range by the R2. -2.5 ~ -4.5V (V_{DD} -V_5 → 7V ~ 9V)
  (Determined by the LCD electrical characteristics)

R1, R2 and R3 are calculated by above conditions and the formula of ① to mentioned below;(reference)

R1=1.388M Ω
R2=0.388M Ω
R3=3.214M Ω

The voltage adjust circuits has a temperature coefficient against the V_{REG} output. If necessary, please connect the thermistor to the voltage adjust circuits serially.

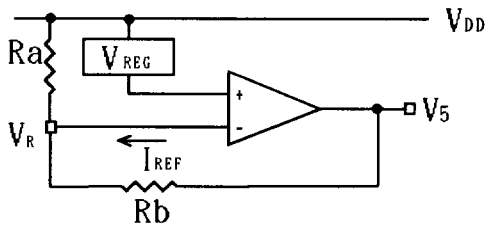
To avoid the noise trouble, short wiring or sealed wiring is required for VR terminal input due to the VR terminal is high impedance.

(c) Contrast Adjustment by using the EVR function

To use EVR function, the LCD driving voltage of V_5 which controls LCD display contrast can adjust by the ins truction. The EVR function is executed to set the 4 bits data into the EVR resistor and determine the one out put voltage status out of 16 prefixed voltage status.

When execute the EVR function, set the T1 and T2 except the "H, H" and execute the Internal Power Supply On instruction.

[External parts constants setting example when EVR function using / reference]



(1) Determine the V_5 voltage range controlled by EVR.

LCD Driving Voltage	V_{DD}-V_5	7～9V
The range of V_5		2V

(2) Determine the Rb.

Rb = [The range of V_5]/I_{REF} (16 status I_{REF} ≒ 2.5 μA constant current)

Rb = 2V/2.5 μA = 0.8M Ω *Ta=25 ℃ V_{DD}-V_{OUT} =9V

(3) Adjust the Ra

$$Ra = \frac{V_{REG}}{([\text{LCD Driving Voltage}]-V_{REG})/Rb}$$

$$Ra = \frac{2.5\ V}{(7V-2.5V)/0.8M\ \Omega} = 0.44M\ \Omega$$

(4) Adjust the Ra

Adjust the Ra to good contrast of LCD display after the (D_3 ,D_2 ,D_1 ,D_0) of EVR register set to (1, 0, 0, 0) or (0, 1, 1, 1). When the EVR using, Ra use a variable resistance and contrast adjustment mentioned in (4) f or each chip is required due to the I_{REF} is simple constant current source.

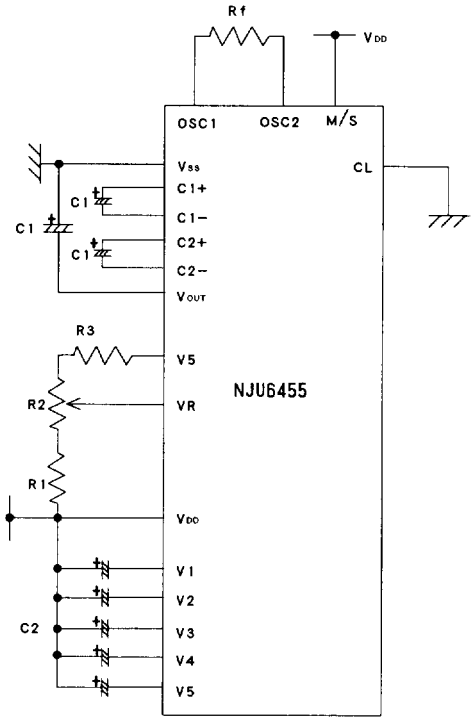
When the EVR function does not use, the (D_3 ,D_2 ,D_1 ,D_0) of EVR register set to (0, 0, 0, 0) by the RES sig nal or the EVR Register Set instruction.

(d) LCD Driving Voltage Generation Circuits

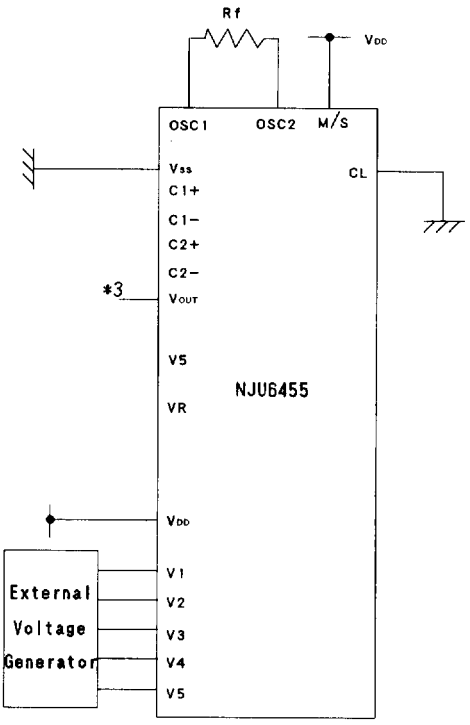
The LCD driving bias voltage of V_1, V_2, V_3, V_4 are generated internally to divide the V5 voltage by the blee der resistance. And its supply to the LCD driving circuits after convert the impedance.

As shown in Fig. 4, five capacitor are required for each LCD driving voltage terminal as a voltage stabilizing. And the value of capacitor C2 determine by combine with the actual LCD panel.

Using the internal Power Supply



Using the external Power Supply



Reference set up value

$V_{LCD}=V_{DD}-V5 \fallingdotseq 7 \sim 9$ V

C1	4.7~10μF
C2	0.1 ~ 0.47μF
R1	1. 388MΩ
R2	388KΩ
R3	3. 214MΩ

Fig. 4

*1 To avoid the malfunction, use a short wiring for the feed back resistance Rf of oscillation circuits.

*2 Short wiring or sealed wiring is required for the VR terminal due to the high impedance of VR terminal.

*3 Following connection of VOUT is required when external power supply using.

When $V_{SS} > V_5$ -- $V_{OUT} = V_5$

When $V_{SS} \leqq V_5$ -- $V_{OUT} = V_{SS}$

(5) MPU Interface

(5-1) Interface type selection

NJU6455 can interface by using both of 8 bit bilateral data bus (D_7 to D_0) or serial interface (SI). The 8 bit parallel or serial interface is determined the P/S terminal connected to "H" or "L" level as shown in Table 5. In case of the serial interface, status and RAM data read out is impossible.

Table 5

P/S	Type	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	SI	SCL	$D_0 \sim D_7$
H	Parallel	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	-	-	$D_0 \sim D_7$
L	Serial	$\overline{CS1}$	CS2	A0	-	-	-	SI	SCL	-

(5-2) Parallel Interface

The NJU6455 can interface both of 68 or 80 type MPU directly by setting the parallel interface (P/S="H") and "H" or "L" of the C86 terminal as shown in table 6.

Table 6

C86	Type	$\overline{CS1}$	CS2	0	$\overline{RD}$	$\overline{WR}$	$D_0 \sim D_7$
H	68 type MPU	$\overline{CS1}$	CS2	0	E	R/W	$D_0 \sim D_7$
L	80 type MPU	$\overline{CS1}$	CS2	0	$\overline{RD}$	$\overline{WR}$	$D_0 \sim D_7$

(5-3) Discrimination of Data Bus Signal

The NJU6455 discriminate the signal on the data bus by the combination of A0, E, R/W, and ($\overline{RD}$,$\overline{WR}$) signals as shown in Table 7.

Table 7

Common	68 type	80 type		Function
A0	R/W	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Read Display Data
1	0	1	0	Write Display Data
0	1	0	1	Status Read
0	0	1	0	Write into the Register(Instruction)

(5-4) Serial Interface.(P/S="L")

Serial interface circuits consist of 8 bits shift register and 3 bits counter. SI and SCL input are activated when the chip select terminals set to $\overline{CS1}$="L" and CS2="H", and P/S terminal set to "L". The 8 bits shift register and 3 bits counter are reset to the initial condition in no chip selection period. The data input from SI terminal is MSB first like as the order of D_7 to D_0. and the data is entered into the shift register synchronized at the rise edge of the serial clock SCL. The data in the shift register converted to parallel data at the 8th serial clock rise edge input. Discrimination of the display data or instruction for the serial input data is executed by the A0 input which take into the LSI at the 8th serial clock rise edge, or, A0="H" is display data and A0="L" is instruction. The time chart for the serial interface is shown in Fig. 5. To avoid the noise trouble, the short wiring is required for the SCL input.

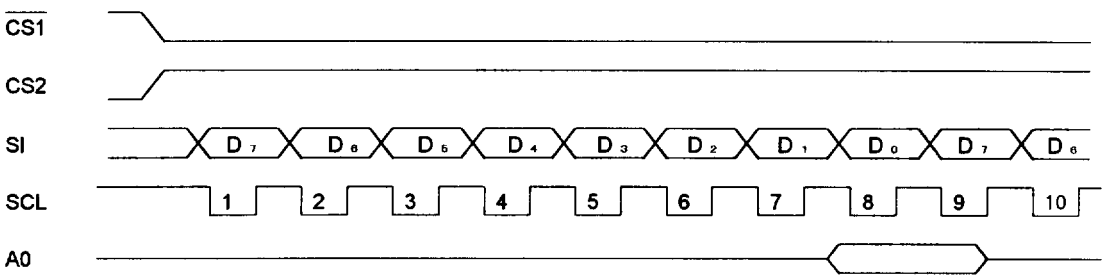


Fig. 5

(5 – 5) Access to the Display Data RAM and Internal Register.

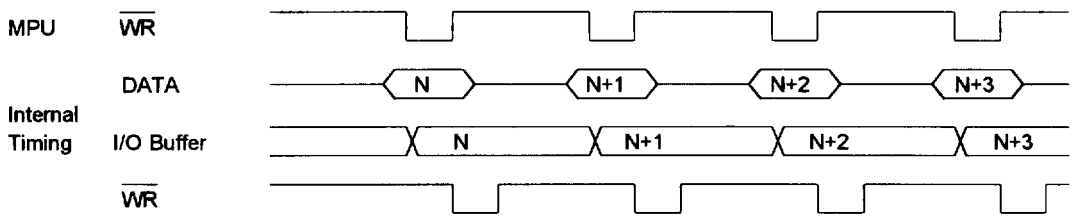
The NJU6455 is operating as one of pipe-line processor by the bus-holder connecting to the internal data bus t o adjust the operation frequency between MPU and the Display Data RAM or Internal Register.

For example, when the MPU read out the data from the Display Data RAM, the data read out in the data read cycle(dummy read) is held in the bus-holder at once then read out from the bus-holder to the system bus at ne xt data read cycle. And when write the data into the Display Data RAM, the data is held in the bus-holder at once then write into the Display Data RAM by next data write cycle.

Therefore high speed data transmission between MPU and NJU6455 is available because of the limitation of a ccess time of NJU6455 locking from MPU is just determined by the cycle time only which ignored the access ti me of t_{ACC} and t_{DS} of Display Data RAM. If the cycle time can not be kept in the MPU operation, NOP oper ation cycle which equivalent to the waiting operation is useful.

Please note that the read out data is a address data when the read out execution just after the address setting. Therefore, one dummy read is required after address setting or write cycle as shown in Fig. 6.

● Write Operation



● Read Operation

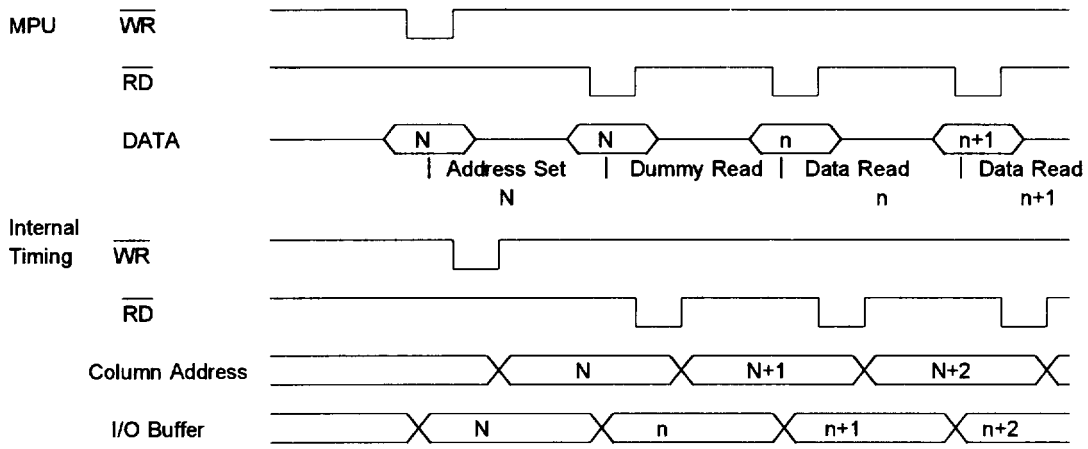


Fig.6

(5-6) Chip Select

CS1,CS2 are Chip Select terminals. The Chip Select is executed by the setting of $\overline{CS1}$="L" and CS2="H". O nly the select mode, the interface with MPU is available. In the non select period, the $D_0 \sim D_7$ are high im pedance and A0, $\overline{RD}$, $\overline{WR}$, SI and SCL input are put on the disable state. If the serial interface is selected in the non select period, the shift register and counter are reset. The reset input is regardless with the condition of $\overline{CS1}$ and CS2.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25 ℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (1)	V_{DD}	- 0.3 ~ + 7.0 - 0.3 ~ + 4.5 (used Tripler)	V
Supply Voltage (2)	V_5	V_{DD} -13.5 ~ V_{DD} +0.3	V
Supply Voltage (3)	V_1 ~ V_4	V_5 ~ V_{DD} +0.3	V
Input Voltage	V_{IN}	- 0.3 ~ V_{DD} +0.3	V
Operating Temperature	Topr	- 30 ~ + 80	℃
Storage Temperature	Tstg	- 55 ~ + 125(Chip) - 55 ~ + 100(TCP)	℃

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 2) All voltage values are specified as V_{SS} = 0 V.

Note 3) The relation : $V_{DD} \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_5$; $V_{DD} > V_{SS} \geqq V_{OUT}$ must be maintained.

Note 4) Decoupling capacitor should be connected between VDD and VSS due to the stabilized operation for voltage converter.

■ ELECTRICAL CHARACTERISTICS (1)

(V_{DD} =5V ± 10%, V_{SS} =0V, Ta=-20 ~ +75 ℃)

PARAMETER		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	Note
Operating Voltage(1)	Recommend	V_{DD}			4.5	5.0	5.5	V	5
	Available				2.4		5.5		
Operating Voltage(2)	Recommend	V_5			V_{DD}-13.5		V_{DD} -3.5	V	
	Available				V_{DD}-13.5				
	Available	V_1, V_2	V_{LCD} =V_{DD} -V_5		V_{DD}-0.6xV_{LCD}		V_{DD}		
	Available	V_3, V_4			V_5		V_{DD}-0.4xV_{LCD}		
Input Voltage	1	V_{IHC1}	A0, D_0~D_7, RD,WR,CS_1, CS_2,CL,FR, M/S,RES,C86 SI,SCL,P/S Terminals		0.7xV_{DD}		V_{DD}	V	
		V_{IHC2}		V_{DD}=2.7V	0.8xV_{DD}		V_{DD}		
	2	V_{ILC1}			V_{SS}		0.3xV_{DD}		
		V_{ILC2}		V_{DD}=2.7V	V_{SS}		0.2xV_{DD}		
Output Voltage	1	V_{OHC11}	D_0~D_7,FR CLO,DYO Terminals	I_{OH} =-1mA	0.8xV_{DD}		V_{DD}	V	
		V_{OHC12}		I_{OH}=-120uA V_{DD}=2.7V	0.8xV_{DD}		V_{DD}		
		V_{OHC21}	OSC_2 Terminal	I_{OH}=-0.5mA	0.8xV_{DD}		V_{DD}		
		V_{OHC22}		I_{OH} =-50uA V_{DD}=2.7V	0.8xV_{DD}		V_{DD}		
	2	V_{OLC11}	D_0~D_7,FR CLO,DYO Terminals	I_{OL} = 1mA	V_{SS}		0.2xV_{DD}		
		V_{OLC12}		I_{OL}= 120uA V_{DD}=2.7V	V_{SS}		0.2xV_{DD}		
		V_{OLC21}	OSC_2 Terminal	I_{OL}= 0.5mA	V_{SS}		0.2xV_{DD}		
		V_{OLC22}		I_{OL} = 50uA V_{DD}=2.7V	V_{SS}		0.2xV_{DD}		

5

■ ELECTRICAL CHARACTERISTICS (2)

PARAMETER		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	Note
Input Leakage Current		I_{LI}	A0, $\overline{RD}$, $\overline{WR}$, $\overline{CS_1}$, CS_2, CL, M/S RES,C86,SI,SCL,P/S,T1,T2 Terminals		-1.0		1.0	uA	
		I_{LO}	D_0～D_7, FR Terminals		-3.0		3.0		6
Driver On-resistance		R_{ON1}	Ta=25 ℃	V_{LCD} =13.5V		2.0	3.0	kΩ	7
		R_{ON2}		V_{LCD} = 8.0V		3.0	4.5		
Stand-by Current		I_{DDQ}	M/S=V_{SS}, OSC_2=FR=V_{DD}			0.05	5.0	uA	8
Operating Current		I_{DD11}	Display V_{LCD} = 8.0V	f_{CL} =4kHz		13	20	uA	9
		I_{DD12}		Rf=1M Ω		28	45		10
		I_{DD13}	Display V_{LCD} = 8.0V V_{DD} =2.7V	f_{CL} =4kHz		12	18		9
		I_{DD14}		Rf=1M Ω		16	25		10
		I_{DD21}	Accessing fcyc=200kHz			350	500		11
		I_{DD22}		V_{DD}=2. 7V		170	240		11
Input Terminal Capacitance		C_{IN}	Ta=25℃ A0, $\overline{RD}$, $\overline{WR}$, $\overline{CS_1}$, CS_2 CL,M/S,RES,C86,SI,SCL P/S,T1,T2,D_1 to D_7			10		pF	
Oscillation Frequency		fosc	Rf=1MΩ ±2%	V_{DD}=5. 0V	15	18	21	kHz	
			Ta=25 ℃	V_{DD}=2. 7V	11	16	21		
Voltage Tripler	Input Voltage	V_{DD1}	V_{DD}-V_{SS}		2.4		5.5	V	
		V_{DD2}	V_{DD}-V_{SS}. used Tripler		2.4		4.5		12
	Output Volt.	V_{OUT}	V_{SS}-V_{LCD} ,used Tripler		-9.0			V	
	On -resistance	R_{TRI}	V_{DD} =3V;C=4.7uF used Tripler			650	1000	Ω	
	Adjustment range of LCD Driving Volt	V_{OUT}	Tripler Circuit "OFF"		V_{DD}−13. 5		V_{DD} -5.0	V	13
	Voltage Follower	V_5	Voltage Adjustment Circuit "OFF"		V_{DD}−13. 5		V_{DD} -5.0	V	13
	Operating Current	I_{OUT1}	V_{DD} =4.5V,V_{LCD} =8V			58	2.0	mA	14
		I_{OUT2}	COM/SEG Term.Open, No Access			23	1.0		
		I_{OUT3}	Display check. pattern			21	0.8		
	Voltage Reg.	V_{REG}	V_{DD}-V_{out} =9V;Ta=25 ℃		T.B.D	2.5	T.B.D	V	15
	Reference Current	I_{REF}	V_{DD}-V_{out} =9V;Ta=25 ℃		T.B.D	2.5	T.B.D	uA	

Note 5) NJU6455 can operate wide operating range, but it is not guarantee immediate voltage changing during the accessing of the MPU.

Note 6) Apply to the High-impedance state of D_0 to D_7 and FR terminals.

Note 7) R_{ON} is the resistance values between power supply terminals(V_1,V_2,V_3,V_4) and each output terminals of common and segment supplied by 0.1V. This is specified within the range of supply voltage (2).

Note 8,9,10,11,14) Apply to current after "LCD Driving Voltage Set".

Note 9) Apply to the external display clock operation in no access from the MPU and no use inter-nal power supply circuits.

Note 10) Apply to the internal CR oscillator operation in no access from the MPU and no use inter-nal power supply circuits.

Note 11) Apply to the condition of cyclic (tcyc) inverted data input continuously in no use internal power supply circuits. The operating current during the accessing is proportionate to the access frequency. In the no accessing period, it is as same as I_{DD1X}.

Note 12) Supply voltage (V_{DD}) range for internal Voltage Tripler operation.

Note 13) LCD driving voltage V_5 can be adjusted within the voltage follower operating range.

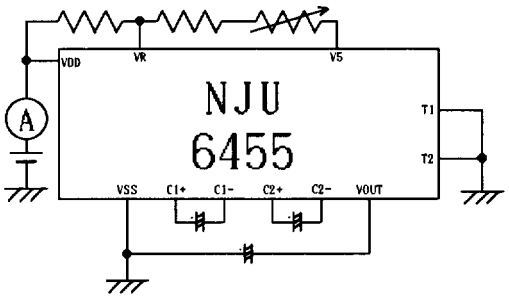
Note 14) Each operating current of voltage supply circuits block is specified under below table conditions.

SYMBOL	Status		Operating Condition				External Voltage Supply (Input Terminal)
	T1	T2	Internal Oscillator	Voltage Tripler	Voltage Adjustment	Voltage Follower	
I_{OUT1}	L	*	Validity	Validity	Validity	Validity	Unuse
I_{OUT2}	H	L	Validity	Invalidity	Validity	Validity	Use(V_{OUT})
I_{OUT3}	H	H	Validity	Invalidity	Invalidity	Validity	Use (V_{OUT}, V_5)

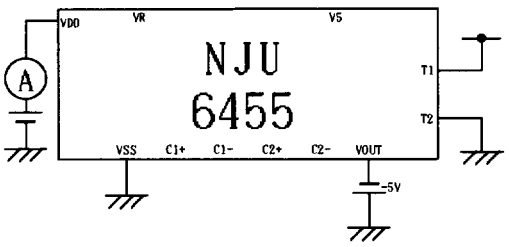
* = Don't Care

Note 15) Apply to the precision of Voltage on each EVR steps.

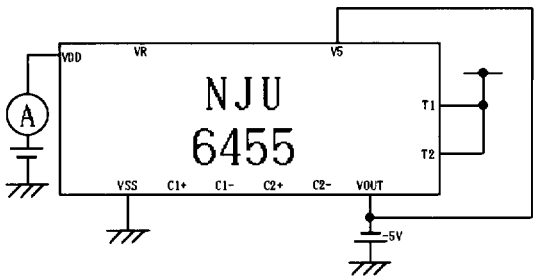
MEASUREMENT BLOCK DIAGRAM : I_{OUT1}



: I_{OUT2}



: I_{OUT3}



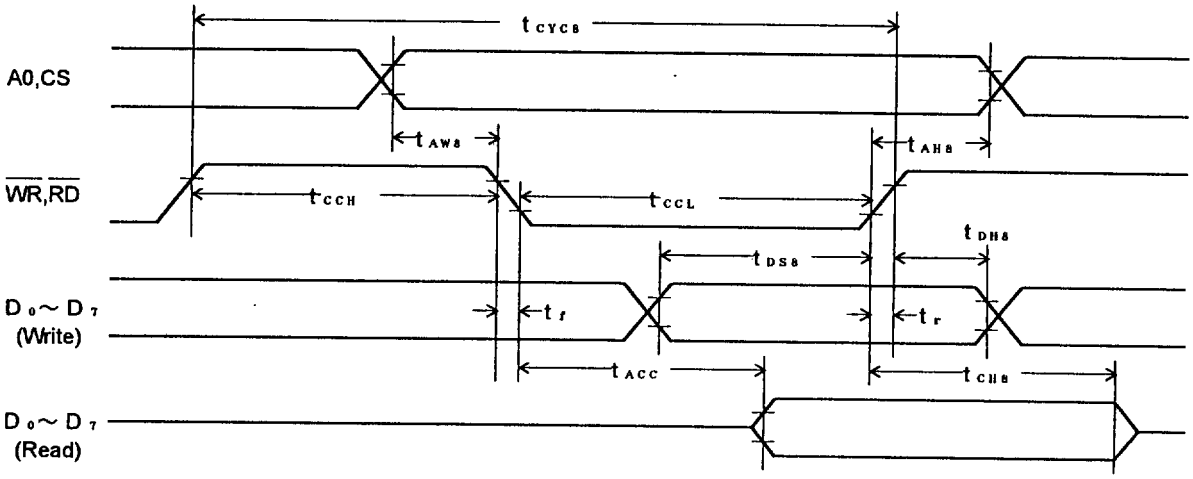
■ ELECTRICAL CHARACTERISTICS (3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
Reset time	t_R	$\overline{RES}$ Terminal	1.0			us	16
Reset "L" Level Pulse Width	t_{RW}		10			us	17

Note 16) Specified from the rising edge of $\overline{RES}$ to finish the internal circuit reset.
Note 17) Specified minimum pulse width of $\overline{RES}$ signal. Over than t_{RW} "L" input should be required for correct reset operation.

■ BUS TIMING CHARACTERISTICS

• Read/Write operation sequence (80 Type MPU)



(V_{DD} =5.0V ± 10%, Ta=-20 ～ 75 ℃)

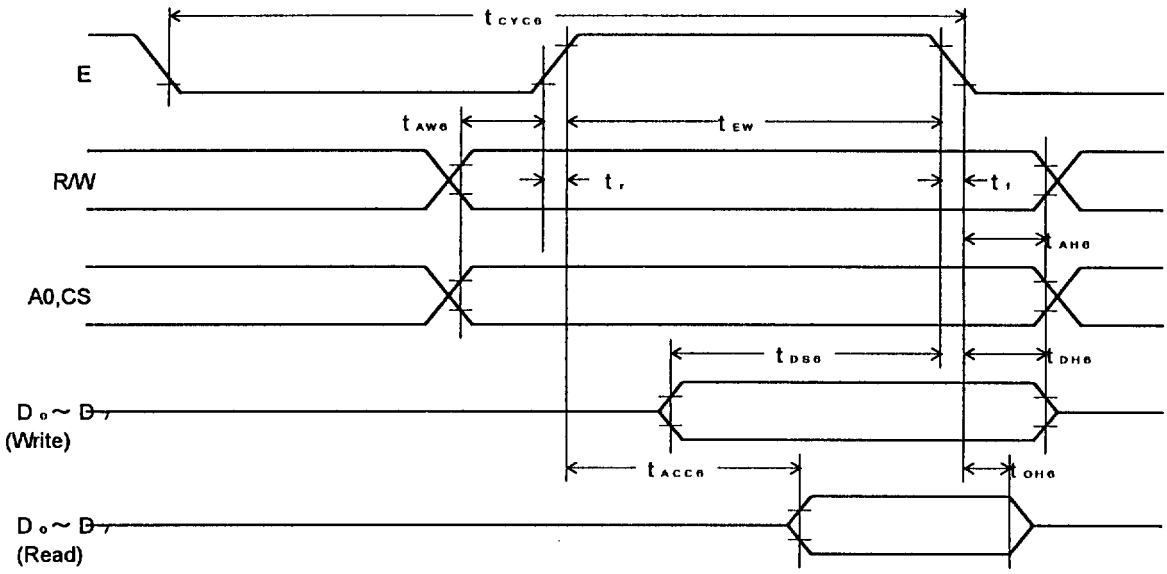
PARAMETER			SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time		A0, $\overline{CS_1}$, CS_2 Terminals	t_{AH8}	10			ns
Address Set Up Time			t_{AW8}	10			
System Cycle Time		$\overline{WR}$, $\overline{RD}$ Terminals	t_{CYC8}	180			
Control Pulse Width	$\overline{WR}$,"L"		t_{CCL} (W)	25			
	$\overline{RD}$,"L"		t_{CCL} (R)	80			
	"H"		t_{CCH}	70			
Data Set Up Time		D_0～D_7 Terminals	t_{DS8}	60			
Data Hold Time			t_{DH8}	10			
RD Access Time			t_{ACC8}		70	CL=100pF	
Output Disable Time			t_{OH8}	0	30		
Rise Time, Fall Time		$\overline{CS_1}$, CS_2, $\overline{WR}$, $\overline{RD}$, A0, D_0～D_7 Terminals	t_r, t_f		15		

(V_{DD} =2.7V ～ 4.5V, Ta=-20 ～ 75 ℃)

PARAMETER			SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time		A0, $\overline{CS_1}$, CS_2 Terminals	t_{AH8}	25			ns
Address Set Up Time			t_{AW8}	25			
System Cycle Time		$\overline{WR}$, $\overline{RD}$ Terminals	t_{CYC8}	450			
Control Pulse Width	$\overline{WR}$,"L"		t_{CCL} (W)	50			
	$\overline{RD}$,"L"		t_{CCL} (R)	200			
	"H"		t_{CCH}	220			
Data Set Up Time		D_0～D_7 Terminals	t_{DS8}	120			
Data Hold Time			t_{DH8}	35			
RD Access Time			t_{ACC8}		140	CL=100pF	
Output Disable Time			t_{OH8}	0	35		
Rise Time, Fall Time		$\overline{CS_1}$, CS_2, $\overline{WR}$, $\overline{RD}$, A0, D_0～D_7 Terminals	t_r, t_f		15		

Note 18) Rise time(tr) and fall time(tf) of input signal should be less than 15ns.
Note 19) Each timing is specified bas ed on 0.2xV_{DD} and 0.8xV_{DD}.

• Read/Write operation sequence (68 Type MPU)



(VDD =5.0V ± 10%, Ta=-20 ~ 75 °C)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time	A0, $\overline{CS_1}$, CS_2, R/W Terminals	t_{AH6}	10			ns
Address Set Up Time		t_{AW6}	10			
System Cycle Time		t_{CYC6}	180			
Enable Pulse Width (Read)	E Terminal	t_{EW}	100			
Enable Pulse Width (Write)			25			
Data Set Up Time	D0~D7 Terminals	t_{DS6}	60			
Data Hold Time		t_{DH6}	20			
Access Time		t_{ACC6}		70	CL=100pF	
Output Disable Time		t_{OH6}	0	25		
Rise Time, Fall Time	A0, $\overline{CS_1}$, CS_2, R/W, E, D0~D7 Terminals	t_r, t_f		15		

(VDD =2.7V ~ 4.5V, Ta=-20 ~ 75 °C)

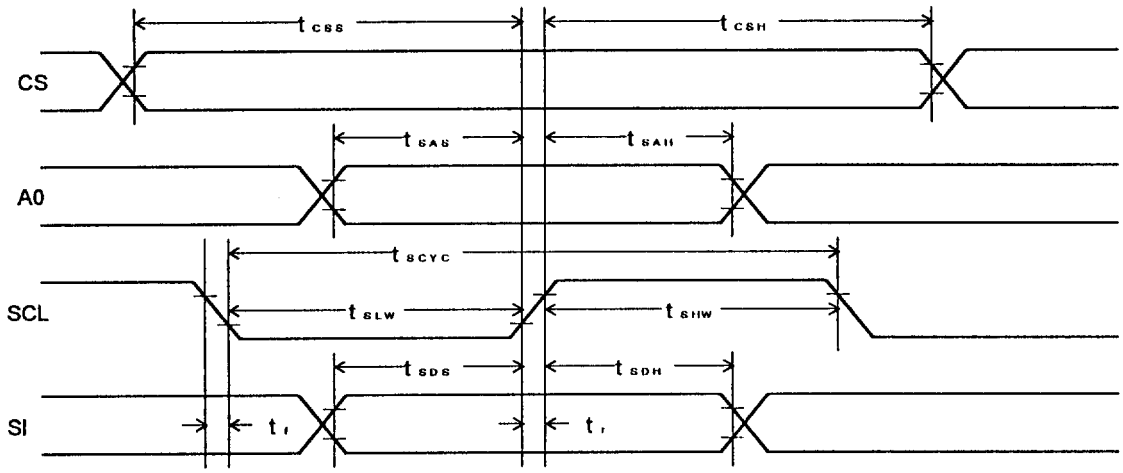
PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Address Hold Time	A0, $\overline{CS_1}$, CS_2, R/W Terminals	t_{AH6}	25			ns
Address Set Up Time		t_{AW6}	25			
System Cycle Time		t_{CYC6}	450			
Enable Pulse Width (Read)	E Terminal	t_{EW}	200			
Enable Pulse Width (Write)			50			
Data Set Up Time	D0~D7 Terminals	t_{DS6}	120			
Data Hold Time		t_{DH6}	40			
Access Time		t_{ACC6}		140	CL=100pF	
Output Disable Time		t_{OH6}	0	45		
Rise Time, Fall Time	A0, $\overline{CS_1}$, CS_2, R/W, E, D0~D7 Terminals	t_r, t_f		15		

Note 20) t_{CYC6} indicates the E signal cycle during the CS activation period. The System Cycle Time must be required after CS becomes active.

Note 21) Rise time(tr) and fall time(tf) of input signal should be less than 15ns.

Note 22) Each timing is specified based on 0.2xV_{DD} and 0.8xV_{DD} .

- Read/Write operation sequence (Serial Interface)



(V_{DD} =5.0V ± 10%, Ta=-20 ~ 75 °C)

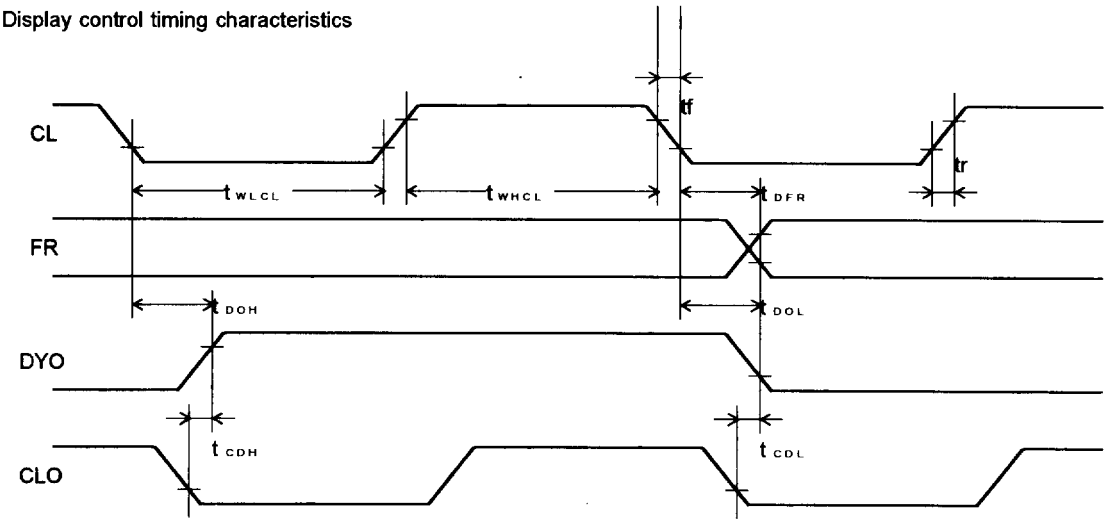
PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Serial Clock cycle	SCL Terminal	t_{SCYC}	500			ns
SCL "H" pulse width		t_{SHW}	150			
SCL "L" pulse width		t_{SLW}	150			
Address Set Up Time	A0 Terminal	t_{SAS}	120			
Address Hold Time		t_{SAH}	200			
Data Set Up Time	SI Terminal	t_{SDS}	120			
Data hold Time		t_{SDH}	50			
$\overline{CS}$-SCL Time	$\overline{CS_1}$, CS_2 Terminals	t_{CSS}	30			
		t_{CSH}	400			
Rise Time, Fall Time	SCL, A0, $\overline{CS_1}$, CS_2, SI, Terminals	t_r, t_f		15		

(V_{DD} =2.7V ~ 4.5V, Ta=-20 ~ 75 °C)

PARAMETER		SYMBOL	MIN	MAX	CONDITION	UNIT
Serial Clock cycle	SCL Terminal	t_{SCYC}	1000			ns
SCL "H" pulse width		t_{SHW}	300			
SCL "L" pulse width		t_{SLW}	300			
Address Set Up Time	A0 Terminal	t_{SAS}	250			
Address Hold Time		t_{SAH}	400			
Data Set Up Time	SI Terminal	t_{SDS}	250			
Data hold Time		t_{SDH}	100			
$\overline{CS}$-SCL Time	$\overline{CS_1}$, CS_2 Terminals	t_{CSS}	60			
		t_{CSH}	800			
Rise Time, Fall Time	SCL, A0, $\overline{CS_1}$, CS_2, SI, Terminals	t_r, t_f		15		

Note 23) Rise time(tr) and fall time(tf) of input signal should be less than 15ns.
Note 24) Each timing is specified based on 0.2xV_{DD} and 0.8xV_{DD}.

- Display control timing characteristics



Input Timing

(V_{DD} =5.0V ± 10%, Ta=-20 ~ 75 ℃)

PARAMETER		SYMBOL	MIN	TYP	MAX	CONDITION	UNIT
"L" level Pulse Width	CL Terminal	t_{WLCL}	35				μs
"H" level Pulse Width		t_{WHCL}	35				
Rise Time		tr		30			ns
Fall Time		tf		30			
FR Delay Time	FR Terminal	t_{DFR}	-1.0		1.0		μs

(V_{DD} =2.7V ~ 4.5V, Ta=-20 ~ 75 ℃)

PARAMETER		SYMBOL	MIN	TYP	MAX	CONDITION	UNIT
"L" level Pulse Width	CL Terminal	t_{WLCL}	35				μs
"H" level Pulse Width		t_{WHCL}	35				
Rise Time		tr		40			ns
Fall Time		tf		40			
FR Delay Time	FR Terminal	t_{DFR}	-1.0		1.0		μs

Output Timing

(V_{DD} =5.0V ± 10%, Ta=-20 ~ 75 ℃)

PARAMETER		SYMBOL	MIN	TYP	MAX	CONDITION	UNIT
FR Delay Time	FR Terminal	t_{DFR}		60	150	CL=50pF	ns
DY0 "H" Delay Time	DY0 Terminal	t_{DOH}		70	160		
DY0 "L" Delay Time		t_{DOL}		70	160		
CL0-DY0 "H" Delay Time	CL0 Terminal	t_{CDH}		40	100	Note 26	
CL0-DY0 "L" Delay Time		t_{CDL}		40	100		

(V_{DD} =2.7V ~ 4.5V, Ta=-20 ~ 75 ℃)

PARAMETER		SYMBOL	MIN	TYP	MAX	CONDITION	UNIT
FR Delay Time	FR Terminal	t_{DFR}		120	240	CL=50pF	ns
DY0 "H" Delay Time	DY0 Terminal	t_{DOH}		140	250		
DY0 "L" Delay Time		t_{DOL}		140	250		
CL0-DY0 "H" Delay Time	CL0 Terminal	t_{CDH}		100	200	Note 26	
CL0-DY0 "L" Delay Time		t_{CDL}		100	200		

Note 25) The FR Delay Time of input timing is applied to the slave operation.
The FR Delay Time of output timing is applied to the master operation.
Note 26) The CLO "H,L" Delay Time are applied to the master operation only.
Note 27) Each timing is specified based on 0.2xV_{DD} and 0.8xV_{DD} .

■ LCD DRIVING WAVEFORM

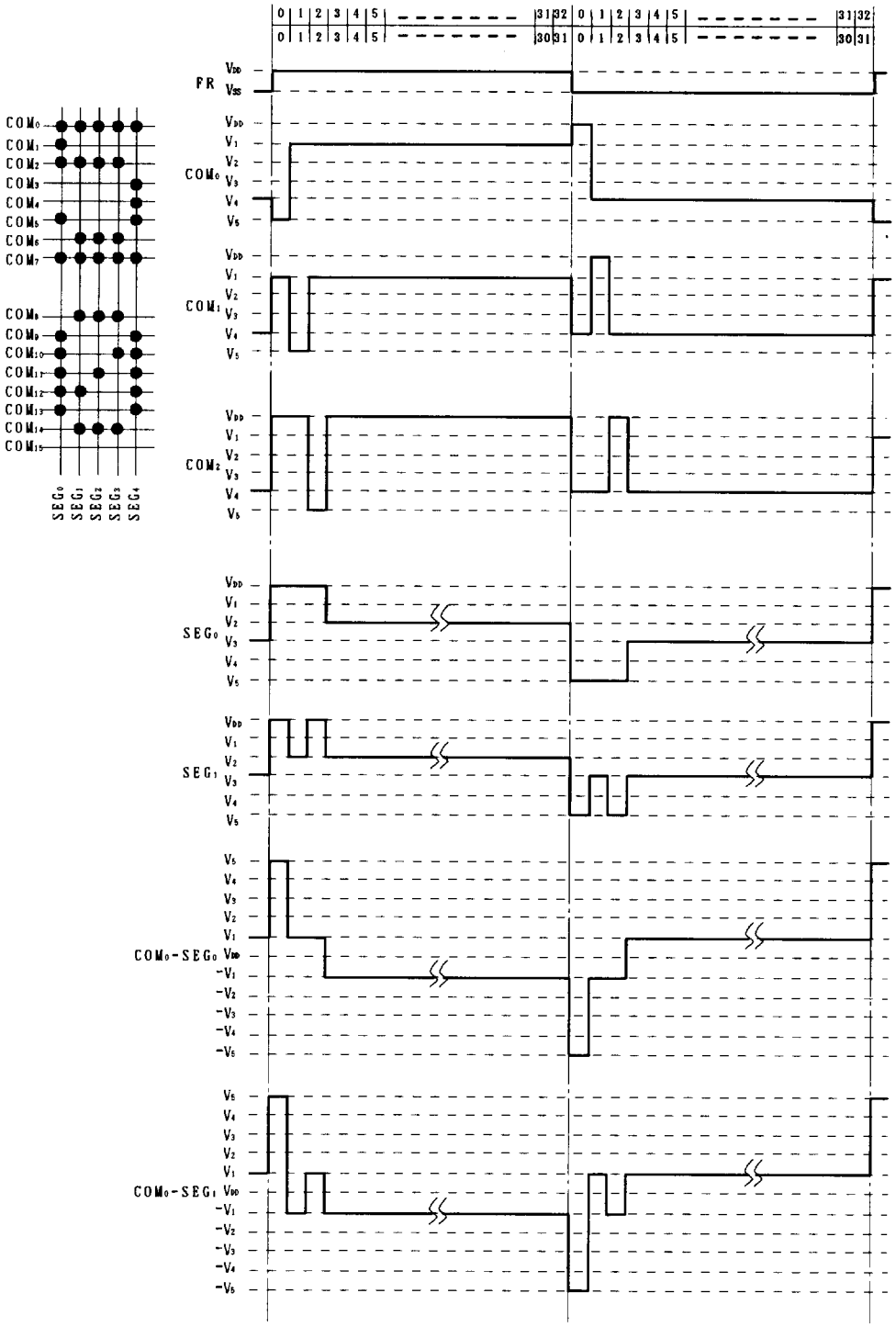


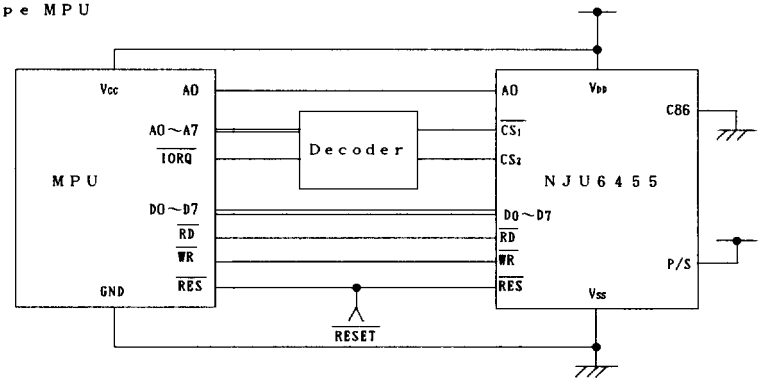
Fig.7

■ APPLICATION CIRCUIT

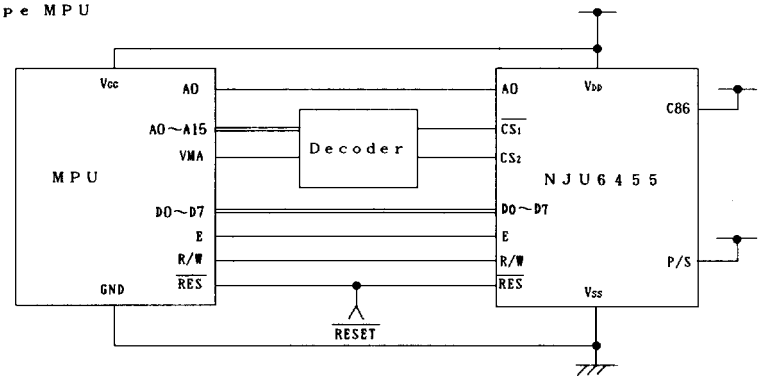
(1)Microprocessor Interface Examples

The NJU6455 can interface both of 80 type and 68 type MPU by the serial format directly. Therefore minimum wiring for the MPU interface is available. In case of multi-chip application, these can connect with MPU respectively and select the each chip by the chip select signal.

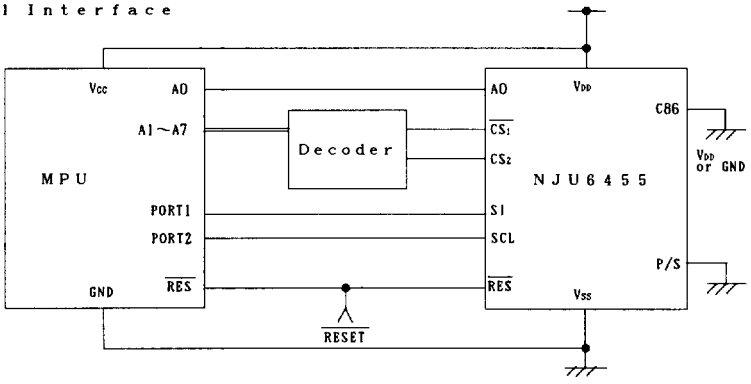
●80 Type MPU



●68 Type MPU



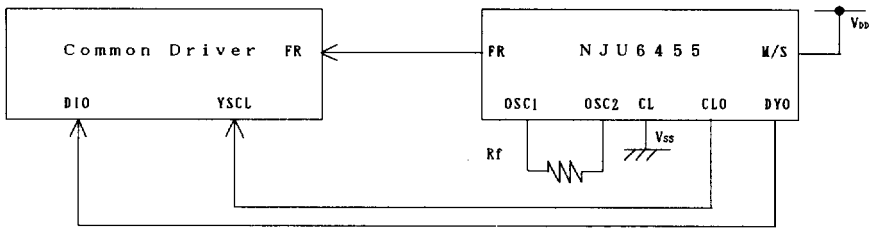
●Serial Interface



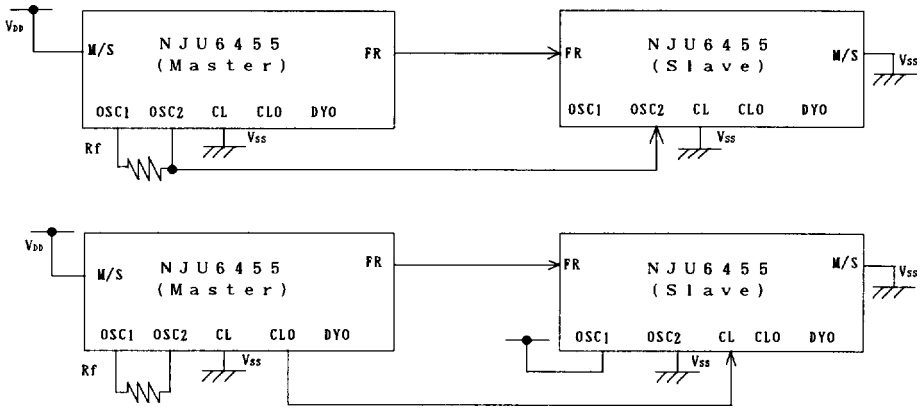
(2)Connection between LCD Drivers

By the multi-chip application, NJU6455 can expand total display capacity. And common exclusive driver also can connect with the NJU6455

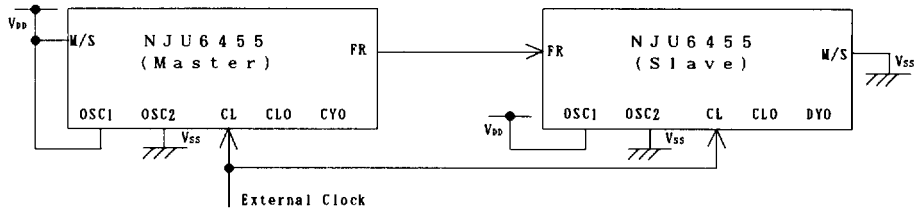
●NJU6455 – Common Driver



●NJU6455–NJU6455
(Using OSC Circuit)



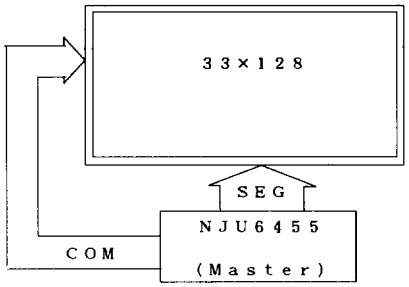
●NJU6455–NJU6455
(External Clock)



5

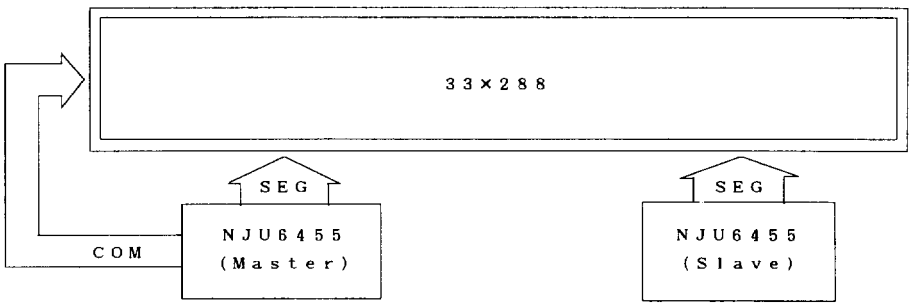
(3)LCD Panel Interface Examples

●1 Chip Construction



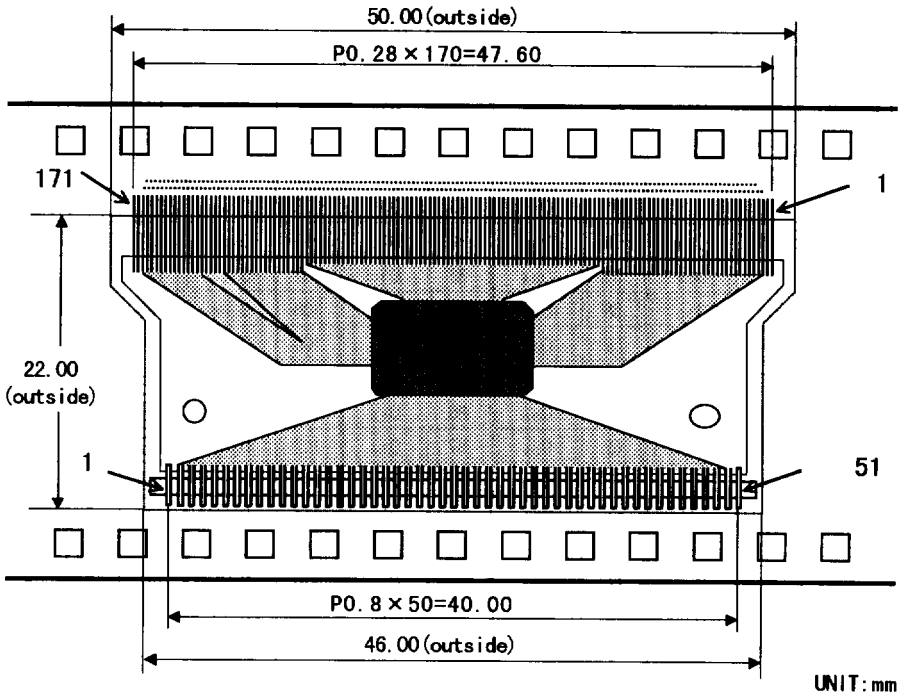
Output Condition:Case2

●2 Chip Construction



Output Condition:Case2　　Output Condition:Case4

■ PACKAGE INFORMATION (NJU6455H01)



■ SPECIFICATION

Name	Material	Thickness
Base Film	UPILEX	75±8um
Adhesive	Epoxi type	19±4um
Conductor Layer	Electrolysis Copper Foil	35±5um
Plating	Sn	0.3±0.1um
Resist	Epoxi type	20±15um
Sealing Material	Epoxi type	—
Bump	Au(Gold)	—
Thickness of TCP		0.8mm(Max)

■ PIN CONFIGURATION (NJU6455H01)

OUTPUT TERMINALS

No.	Name	No.	Name	No.	Name	No.	Name	No.	Name	No.	Name	No.	Name
1	DUMMY	26	O_{23}	51	O_{48}	76	O_{73}	101	O_{98}	126	O_{123}	151	DUMMY
2	DUMMY	27	O_{24}	52	O_{49}	77	O_{74}	102	O_{99}	127	O_{124}	152	DUMMY
3	O_0	28	O_{25}	53	O_{50}	78	O_{75}	103	O_{100}	128	O_{125}	153	O_{144}
4	O_1	29	O_{26}	54	O_{51}	79	O_{76}	104	O_{101}	129	O_{126}	154	O_{145}
5	O_2	30	O_{27}	55	O_{52}	80	O_{77}	105	O_{102}	130	O_{127}	155	O_{146}
6	O_3	31	O_{28}	56	O_{53}	81	O_{78}	106	O_{103}	131	O_{128}	156	O_{147}
7	O_4	32	O_{29}	57	O_{54}	82	O_{79}	107	O_{104}	132	O_{129}	157	O_{148}
8	O_5	33	O_{30}	58	O_{55}	83	O_{80}	108	O_{105}	133	O_{130}	158	O_{149}
9	O_6	34	O_{31}	59	O_{56}	84	O_{81}	109	O_{106}	134	O_{131}	159	O_{150}
10	O_7	35	O_{32}	60	O_{57}	85	O_{82}	110	O_{107}	135	O_{132}	160	O_{151}
11	O_8	36	O_{33}	61	O_{58}	86	O_{83}	111	O_{108}	136	O_{133}	161	O_{152}
12	O_9	37	O_{34}	62	O_{59}	87	O_{84}	112	O_{109}	137	O_{134}	162	O_{153}
13	O_{10}	38	O_{35}	63	O_{60}	88	O_{85}	113	O_{110}	138	O_{135}	163	O_{154}
14	O_{11}	39	O_{36}	64	O_{61}	89	O_{86}	114	O_{111}	139	O_{136}	164	O_{155}
15	O_{12}	40	O_{37}	65	O_{62}	90	O_{87}	115	O_{112}	140	O_{137}	165	O_{156}
16	O_{13}	41	O_{38}	66	O_{63}	91	O_{88}	116	O_{113}	141	O_{138}	166	O_{157}
17	O_{14}	42	O_{39}	67	O_{64}	92	O_{89}	117	O_{114}	142	O_{139}	167	O_{158}
18	O_{15}	43	O_{40}	68	O_{65}	93	O_{90}	118	O_{115}	143	O_{140}	168	O_{159}
19	O_{16}	44	O_{41}	69	O_{66}	94	O_{91}	119	O_{116}	144	O_{141}	169	COM1
20	O_{17}	45	O_{42}	70	O_{67}	95	O_{92}	120	O_{117}	145	O_{142}	170	DUMMY
21	O_{18}	46	O_{43}	71	O_{68}	96	O_{93}	121	O_{118}	146	O_{143}	171	DUMMY
22	O_{19}	47	O_{44}	72	O_{69}	97	O_{94}	122	O_{119}	147	DUMMY		
23	O_{20}	48	O_{45}	73	O_{70}	98	O_{95}	123	O_{120}	148	DUMMY		
24	O_{21}	49	O_{46}	74	O_{71}	99	O_{96}	124	O_{121}	149	DUMMY		
25	O_{22}	50	O_{47}	75	O_{72}	100	O_{97}	125	O_{122}	150	DUMMY		

INPUT TEMINALS

No.	Name	No.	Name	No.	Name	No.	Name	No.	Name	No.	Name	No.	Name
1	DUMMY	11	SI	21	D_1	31	FR	41	$C2^-$	51	DUMMY		
2	V_5	12	P/S	22	D_2	32	CL	42	V_{OUT}				
3	V_4	13	CS_1	23	D_3	33	OSC_2	43	V_5				
4	V_3	14	CS_2	24	D_4	34	OSC_1	44	VR				
5	V_2	15	C86	25	D_5	35	T2	45	V_{DD}				
6	V_1	16	AO	26	D_6	36	T1	46	V_1				
7	V_{DD}	17	WR	27	D_7	37	V_{SS}	47	V_2				
8	M/S	18	RD	28	DY0	38	$C1^+$	48	V_3				
9	RES	19	V_{SS}	29	CL0	39	$C1^-$	49	V_4				
10	SCL	20	D_0	30	DUMMY	40	$C2^+$	50	V_5				