OKI semiconductor

MSM5840

CMOS 4-BIT SINGLE CHIP MICROCONTROLLER

GENERAL DESCRIPTION

The OKI MSM5840 microcontroller is a low-power, high-performance single chip device implemented in complementary metal oxide semiconductor technology. Integrated within this one chip are 16K bits of mask program ROM, 512 bits of data RAM, 30 Input/Output lines, a programmable timer/counter, and oscillator. Program memory is byte wide and data-paths are organized in 4 bit nibbles. RAM and I/O lines are bit addressable. Up to 4K of external ROM interfaces to the 8 bit bidirectional bus. 98 instructions include binary, BCD, logical operations; bit set, reset, test, 8 bit I/O; relative jumps; multifunctional instructions (increment, modify, skip); 8 bit wide table output; subroutine call and return. 94% of instructions are single byte, single cycle operations.

FEATURES

- Low Power Consumption – 8mW Typical
- 100% Static Logic – 50μW Standby, Typical
- 2K × 8 Internal ROM
- Up to 4K × 8 External ROM
- 128 × 4 Internal RAM
- 30 I/O Lines Incl. 8 Bit Data Bus
- Programmable 8 Bit Timer/Counter
- Self-contained Oscillator
- 98 Instructions
- Expandable Memory and I/O
- 2 Interrupt Levels
- 4 Stack Levels
- Operating Temperature
  −40° to +85°C
- 3V to 6V Operating V_{DD}
- Battery Powered or Battery Backup
- TTL Compatible (with pullups)
- 7.6μs Cycle Time @4.2MHz (V_{DD} 5V± 10%)

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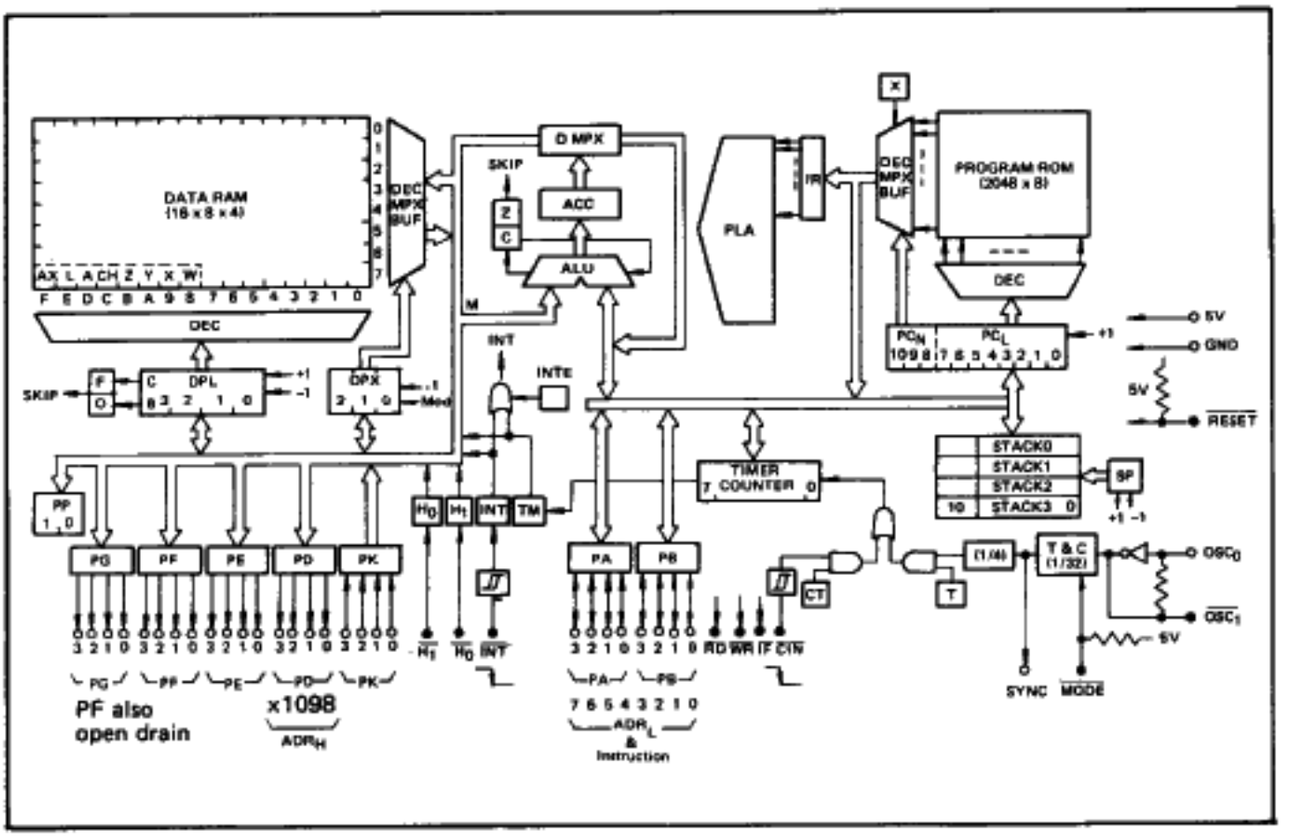
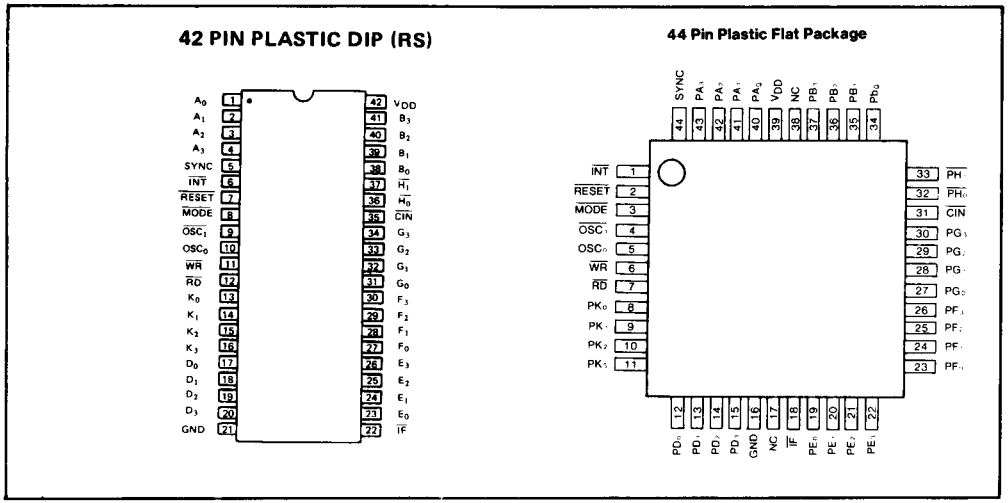
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



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PIN DESCRIPTION

Designation	Pin No.	Function
GND	21	Circuit GND potential
V_{DD}	42	Main power source (+5V)
OSC_0	10	Crystal OSC input, external clock input
$\overline{OSC_1}$	9	Crystal OSC input, external clock output (not TTL compatible)
PA, PB	1 to 4 38 to 41	Pseudo-bidirectional ports for 4-bit parallel I/O. Used as a pair for 8-bit I/O. Used to output 8 LSBs of address in external ROM mode. Used to read external instruction during IF.
PD, PE, PE, PG	17 to 20 23 to 34	Output ports for 4-bit parallel output and bit set/reset. Specified by internal port pointer, Bit position specified by set/reset instruction. PD also used for instruction address MSBs in external ROM mode during IF.
PK	13 to 16	4-bit parallel or bit test input port (unlatched)
$\overline{PH}$	36 and 37	2-bit input port with latched memory (negative level sensitive)
$\overline{RESET}$	7	RESET has priority over every other signal. (see MSM5840 user's manual for initialization sequence)
$\overline{MODE}$	8	Used to enable external ROM mode during RESET and also to enable STOP mode during execution (for stepping program)
$\overline{INT}$	6	Negative edge sensitive external interrupt signal associated with EI and DI instructions. Vectors to location 200H.
$\overline{CIN}$	35	Negative edge sensitive external input for counter associated with ECT and DCT instructions. Vectors to location 100H. (same as timer)
SYNC	5	General purpose synchronizing signal output at the beginning of each machine cycle. Used for address strobe during external ROM mode.
$\overline{RD}$	12	Read strobe pulse occuring when port A or B is read (1A, 1B, 1AB)
$\overline{WR}$	11	Write strobe pulse occurring when port A or B is written (OA, OB, OAB, OBS, OTD)
$\overline{IF}$	22	Read strobe pulse occurring during an instruction fetch from external ROM.

FUNCTIONAL DESCRIPTION

Program ROM

The MSM5840 will address up to 4K bytes of program ROM and can have 2K bytes of internal masked ROM, or all ROM may be located externally. External EPROM may be used for program development with conversion to internal ROM occurring after program debug and system checkout and verification. All instructions are byte wide. Only three of the 98 instructions require two bytes of program code. The instructions are routed to a programmed logic array which generates the necessary internal control signals.

Data RAM

Data is organized in 4 bit nibbles. Internal data RAM consists of 128 nibbles, 8 nibbles of which are dedicated registers accessible directly under program control. These are the general purpose registers, W, X, Y and Z, and the 4 save (exchange) registers, CH, A, L, and AX. All other DATA RAM must be addressed indirectly through the DP (data pointer) registers, a seven bit pointer (directly accessible by numerous instructions) consisting of 4 bit DPL register and a 3 bit DP_H register. Any nibble of internal data RAM can be accessed through the DP registers. Some instructions automatically change the contents of the DP registers allowing efficient array processing.

Input/Output Ports

PA, PB – These two ports are pseudo-bidirectional ports which can be used as simple I/O lines or used as either a 4-bit or 8-bit parallel bus. An instruction fetches the external ROM data through these ports by outputting the 8 low order bits of address during SYNC followed by an IF (instruction fetch) cycle. In addition, synchronized data transfers are possible through these ports with the I/O pin signals $\overline{RD}$ and $\overline{WR}$ associated with certain input/output instructions dedicated to these ports. In short, PA and PB can be used as a multiplexed address/instruction/data bus.

PD, PE, PF, PG – These four output ports are addressed indirectly through the TWO BIT port pointer whose contents are changed through certain instructions. These ports are bit (set/reset) addressable. PD is also used for the high order bits of address during an external instruction fetch. PF and PG are open drain outputs and PG is set high by a hardware RESET.

PK is an input port without memory, addressable either as a nibble or bit level input.

PH is a two-bit input port with memory, which can be tested and reset under program control.

External Interrupt

The $\overline{INT}$ pin can be tested under program control or enabled to cause a vectored interrupt to location 200H. It is negative edge sensitive.

Timer/Counter

The timer/counter is an 8-bit counter whose input is selected under program control to be either an external signal (CIN) or an internal square wave of 1/128 the frequency of the OSC_O input (2 MHz/128 = 15.625 kHz). The timer/counter can be enabled or disabled under program control as can be associated internal interrupt which vectors to location 100H and has higher priority than the external interrupt.

Stack

The stack is an LIFO queue for storing return-from-interrupt and return-from-subroutine address information. It is eleven bits wide and 4 levels deep.

Program Counter (PC)

The program counter is 11 bits wide and loaded under program control.

Accumulator

The accumulator register is the data path focal point of the CPU. Approximately one-half of the instructions involve the accumulator. Its contents are the source and destination for many ALU operations and port operations. CASE statements (computed GOTOs) are possible by using the Jump with Accumulator (JA) instruction.

Flags

The MSM5840 is endowed with the following set of flags.

Z – zero flag	: Indicates that the result of the previous operation was zero
F – all ones	: Indicates a carry from the DP_L register
O – all zeros	: Indicates a borrow from the DP_L register
C – carry	: Indicates a carry from the previous operation
T – timer	: Indicates that the timer/counter is specified as a timer
CT – counter	: Indicates that the timer/counter is specified as a counter
TM – timer flag	: Indicates an overflow of the timer/counter register
INT – interrupt	: Latching memory flag for the external interrupt
INTE – interrupt enable	: Indicates that interrupts have been enabled
H_O – H_O memory	: Indicates that an input has been detected on the H_O input
H_1	: same as H_O except H_1 input
X	: 0 indicates internal ROM, 1 indicates external ROM. If all external ROM, 0 indicates first bank of 2K.

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INSTRUCTION SET

	Mnemonic	Description	Instruction Code 7	6	5	4	3	2	1	0	Byte	Cycle
Load, Store, Read, Clear	CLA	Clear Accumulator	0	0	0	1	0	0	0	0	1	1
	CLL	Clear DP_L	0	0	1	0	0	0	0	0	1	1
	CLH	Clear DP_H	0	1	1	0	0	0	0	0	1	1
	LAI	Load Accumulator with Immediate	0	0	0	1	I_3	I_2	I_1	I_0	1	1
	LLI	Load DP_L with Immediate	0	0	1	0	I_3	I_2	I_1	I_0	1	1
	LHI	Load DP_H with Immediate	0	1	1	0	0	I_2	I_1	I_0	1	1
	L	Load Accumulator with Memory	1	0	0	1	0	1	0	0	1	1
	LM	Load Accumulator with Memory then Modify DP_H	1	0	0	1	0	1	I_1	I_0	1	1
	LAL	Load Accumulator with DP_L	0	1	0	1	0	1	0	1	1	1
	LLA	Load DP_L with Accumulator	0	1	0	1	0	1	0	0	1	1
	LAW	Load Accumulator with W Register	1	0	0	0	0	1	0	0	1	1
	LAX	Load Accumulator with X Register	1	0	0	0	0	1	0	1	1	1
	LAY	Load Accumulator with Y Register	1	0	0	0	0	1	1	0	1	1
	LAZ	Load Accumulator with Z Register	1	0	0	0	0	1	1	1	1	1
	SI	Store Accumulator to Memory then Increment DP_L	1	0	0	1	0	0	0	0	1	1
	SMI	Store Accumulator to Memory then Modify DP_H and Increment DP_L	1	0	0	1	0	0	I_1	I_0	1	1
	LWA	Load W Register with Accumulator	1	0	0	0	0	0	0	0	1	1
	LXA	Load X Register with Accumulator	1	0	0	0	0	0	0	1	1	1
	LYA	Load Y Register with Accumulator	1	0	0	0	0	0	1	0	1	1
	LZA	Load Z Register with Accumulator	1	0	0	0	0	0	1	1	1	1
	LPA	Load Port Pointer with Accumulator	0	1	0	1	1	0	0	0	1	1
	LTI	Load Timer with Immediate	0 I_7	1 I_6	1 I_5	0 I_4	1 I_3	0 I_2	0 I_1	0 I_0	2	2
	RTH	Read Timer H	0	1	1	0	1	0	1	0	1	1
	RTL	Read timer L	0	1	1	0	1	0	1	1	1	1
Exchange	XA	Exchange Accumulator with Save Register A	0	1	0	0	1	0	0	1	1	1
	XL	Exchange DP_L with Save Register L	0	1	0	0	1	0	1	0	1	1
	XCH	Exchange DP_H and Carry with Save Register CH	0	1	0	0	1	0	0	0	1	1
	X	Exchange Accumulator with Memory	1	0	0	1	1	0	0	0	1	1
	XM	Exchange Accumulator with Memory then Modify DP_H	1	0	0	1	1	0	I_1	I_0	1	1
	XAX	Exchange Accumulator with Save Register AX	0	1	0	0	1	0	1	1	1	1
Increment/Decrement	INA	Increment Accumulator (Skip if Zero)	0	0	0	0	0	0	0	1	1	1
	INL	Increment DP_L (Skip if Zero)	0	1	0	1	0	1	1	1	1	1
	INM	Increment Memory (Skip if Zero)	0	1	0	1	1	1	0	1	1	1
	INW	Increment W Register (Skip if Zero)	1	0	0	0	1	0	0	0	1	1
	INX	Increment X Register (Skip if Zero)	1	0	0	0	1	0	0	1	1	1
	INY	Increment Y Register (Skip if Zero)	1	0	0	0	1	0	1	0	1	1
	INZ	Increment Z Register (Skip if Zero)	1	0	0	0	1	0	1	1	1	1

INSTRUCTION SET (CONT.)

	Mnemonic	Description	Instruction Code 7	6	5	4	3	2	1	0	Byte	Cycle
Increment/Decrement	DCA	Decrement Accumulator – Skip if Not All Ones	0	0	0	0	1	1	1	1	1	1
	DCL	Decrement DP_L	0	1	0	1	0	1	1	0	1	1
	DCM	Decrement Memory	0	1	0	1	1	1	0	0	1	1
	DCW	Decrement W Register (Skip if All Ones)	1	0	0	0	1	1	0	0	1	1
	DCX	Decrement X Register	1	0	0	0	1	1	0	1	1	1
	DCY	Decrement Y Register	1	0	0	0	1	1	1	0	1	1
	DCZ	Decrement Z Register	1	0	0	0	1	1	1	1	1	1
	DCH	Decrement DP_H – Skip if All Ones and C = Zero	0	1	0	1	1	1	1	1	1	1
Logical	CAO	Complement Accumulator of One	0	1	0	1	0	0	0	0	1	1
	AND	And Accumulator with Memory	0	1	0	0	0	1	0	0	1	1
	OR	Or Accumulator with Memory	0	1	0	0	0	1	0	1	1	1
	EOR	Exclusive or Accumulator with Memory	0	1	0	0	0	1	1	0	1	1
	RAL	Rotate Accumulator Left through Carry	0	1	0	0	0	1	1	1	1	1
Arithmetic	AC	Add Memory to Accumulator with Carry	0	1	0	0	1	1	0	0	1	1
	ACS	Add Memory to Accumulator with Carry, Skip if Carry	0	1	0	0	1	1	0	1	1	1
	AS	Add Memory to Accumulator, Skip if Carry	0	1	0	0	1	1	1	0	1	1
	AIS	Add Immediate to Accumulator, Skip if Carry	0	0	0	0	I_3	I_2	I_1	I_0	1	1
	DAS	Decimal adjust Accumulator in Subtraction	0	1	0	1	1	0	1	0	1	1
	CM	Compare Accumulator with Memory, Skip if Equal	0	1	0	1	1	1	1	0	1	1
	AWS	Add W Register to Accumulator, Skip if Carry	1	0	0	1	1	1	0	0	1	1
	AXS	Add X Register to Accumulator, Skip if Carry	1	0	0	1	1	1	0	1	1	1
	AYS	And Y Register to Accumulator, Skip if Carry	1	0	0	1	1	1	1	0	1	1
	AZS	Add Z Register to Accumulator, Skip if Carry	1	0	0	1	1	1	1	1	1	1
Bit Set/Reset/Test	SPB	Set Port Bit	1	0	1	1	0	0	I_1	I_0	1	1
	RPB	Reset Port Bit	1	0	1	1	0	1	I_1	I_0	1	1
	SMB	Set Memory Bit	1	0	1	1	1	0	I_1	I_0	1	1
	RMB	Reset Memory Bit	1	0	1	1	1	1	I_1	I_0	1	1
	TAB	Test Accumulator Bit (Skip if One)	1	0	1	0	0	0	I_1	I_0	1	1
	TMB	Test Memory Bit	1	0	1	0	0	1	I_1	I_0	1	1
	TKB	Test K Port Bit	1	0	1	0	1	0	I_1	I_0	1	1
	THB	Test H Port Bit	1	0	1	0	1	1	0	I_0	1	1
	TI	Test Interrupt flag	1	0	1	0	1	1	1	1	1	1
	TTM	Test Time flag	1	0	1	0	1	1	1	0	1	1
	TC	Test Carry flag	0	1	0	0	0	0	1	0	1	1
	SC	Set Carry flag	0	1	0	0	0	0	0	0	1	1
	RC	Reset Carry flag	0	1	0	0	0	0	0	1	1	1

INSTRUCTION SET (CONT.)

	Mnemonic	Description	Instruction Code 7	6	5	4	3	2	1	0	Byte	Cycle
Branch/Subroutine	J	Jump	0	0	1	1	0	I_{10}	I_9	I_8	2	2
			I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
	JC	Jump in Current Page	1	1	I_5	I_4	I_3	I_2	I_1	I_0	1	1
	JA	Jump with Accumulator	0	1	0	0	0	0	1	1	1	1
	CAL	Call Subroutine	0	0	1	1	1	I_{10}	I_9	I_8	2	2
			I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
	RT	Return from Subroutine	0	1	0	1	1	0	0	1	1	2
Input/Output	OBS	Output Byte String	0	1	1	1	0	0	0	0	1	2~17
	OTD	Output Table Data	0	1	1	1	0	0	0	1	1	2
	OA	Output Accumulator to Port A	0	1	1	1	0	0	1	0	1	1
	OB	Output Accumulator to Port B	0	1	1	1	0	0	1	1	1	1
	OP	Output Accumulator to Port P designated Port Pointer	0	1	1	1	0	1	0	0	1	1
	OAB	Output Memory and Accumulator to Ports A and B	0	1	1	1	0	1	0	1	1	1
	OPM	Output Memory to Port P designated Port Pointer	0	1	1	1	0	1	1	0	1	1
	IA	Input Port A in Accumulator	0	1	1	1	1	0	1	0	1	1
	IB	Input Port B in Accumulator	0	1	1	1	1	0	1	1	1	1
	IK	Input Port K in Accumulator	0	1	1	1	1	1	0	0	1	1
	IAB	Input Ports A and B in Memory and Accumulator	0	1	1	1	1	1	0	1	1	1
Control	EI	Enable Interrupt	0	1	0	1	0	0	1	1	1	1
	DI	Disable Interrupt	0	1	0	1	0	0	1	0	1	1
	ET	Enable Timer	0	1	1	0	1	1	1	1	1	1
	DT	Disable Timer	0	1	1	0	1	1	1	0	1	1
	ECT	Enable Counter	0	1	1	1	1	1	1	1	1	1
	DCT	Disable Counter	0	1	1	1	1	1	1	0	1	1
	HLT	Halt	0	1	1	0	1	1	0	1	1	1
	EXP	Exchange Program	0	1	1	0	1	0	0	1	1	1
	NOP	No Operation	0	0	0	0	0	0	0	0	1	1

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage	V_{DD}	Ta = 25°C	−0.3 to 7	V
Input Voltage	V_I	Ta = 25°C	−0.3 to VDD	V
Operating Voltage PF PG	V_O	Ta = 25°C	−0.3 to 25	V
Storage Temperature	T_{stg}		−55 to +150	°C

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage	V_{DD}	@1 MHz	3 to 6	V
		@4.2 MHz	4.5 to 5.5	V
Operating Temperature	T_{op}		−40 to +85	°C
Fan Out	N	MOS Load	15	
		TTL Load	1	

D.C. CHARACTERISTICS

(V_{DD} = 5V±10%, Ta = −20° to +70°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
High Input Voltage	V_{IH}	–	3.6			V
Low Input Voltage	V_{IL}	–			0.8	V
High Output Voltage (1)	V_{OH}	I_O = −40μA	4.2			V
Low Output Voltage	V_{OL}	I_O = 1.6mA			0.4	V
OSC_o Input Leak Current	I_{IH}	$V_I = V_{DD}/0V$			25	μA
	I_{IL}				−25	
$\overline{RESET}$, $\overline{MODE}$ Leak Current	I_{IH}	$V_I = V_{DD}/0V$			1	μA
	I_{IL}				−50	
Input Leak Current(2)	I_{IH}	$V_I = V_{DD}/0V$			1	μA
	I_{IL}				−1	
PA, PB High Output Current	I_{OH}	V_{OH} = 0.4V			−1	mA
High Output Current(1)	I_{OH}	V_{OH} = 2.5V	−0.25			mA
Low Output Current	I_{OL}	V_{OL} = 0.4V	1.6			mA
PF, PG Output Breakdown Voltage	BV_{OH}	I_O = 10μA	20			V
Input Capacitance	C_I	f = 1MHz Ta = 25°C		5		pF
Output Capacitance	C_O	f = 1MHz Ta = 25°C		7		pF
Current Consumption(3)	I_{DD}	$V_I = V_{DD}/0V$		10	200	μA
	I_{DD}	$V_I = V_{DD}/0V$ f = 4.2MHz		1.6	4	mA

Notes: (1) Except PA, PB (see graphs)
(2) Except OSC_o, $\overline{RESET}$, $\overline{MODE}$
(3) Typical Value of V_{DD} is 5V

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A.C. CHARACTERISTICS (INTERNAL ROM MODE)

(V_{DD} = 5V±10%, Ta = −40° to +85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Cycle Time	t_{CY}		7.6			μS
Sync Pulse Width	t_{SW}		0.95			μS
$\overline{RD}$ Pulse Width	t_{RW}		1.9			μS
Sync ↑ to $\overline{RD}$ ↓	t_{RD}	C_L = 50pF	1/2 t_{CY} + 0.5			μS
$\overline{WR}$ Pulse Width	t_{WW}		0.95			μS
Sync ↑ to $\overline{WR}$ ↓	t_{WD}	C_L = 50pF	13/16 t_{CY} + 0.5			μS
Port Input Setup Time	t_{DSR}		4/16 t_{CY}			μS
Port Input Hold Time	t_{DHR}		0		0.8	μS
$\overline{WR}$ ↓ to New Data Valid	t_{DDW}	PA, PB C_L = 50pF			0.8	μS
Sync ↑ to New Data Valid	t_{DDS}	PD, PE, PF, PG C_L = 50pF			13/16 t_{CY}+0.5	μS
PH_0, PH_1 Input Pulse Width	t_{HW}	(1)	500			nS
$\overline{CIN}$ Input Pulse Width	t_{CW}		250			nS
INT Input Pulse Width	t_{INTW}	(1)	500			nS

Note: (1) The processor logic will ignore the following events:
1. An INT falling edge occurring during T_{INH} of a T_I instruction.
2. A PH_0 or PH_1 low level occurring only during T_{INH} of a T_{HB} instruction.

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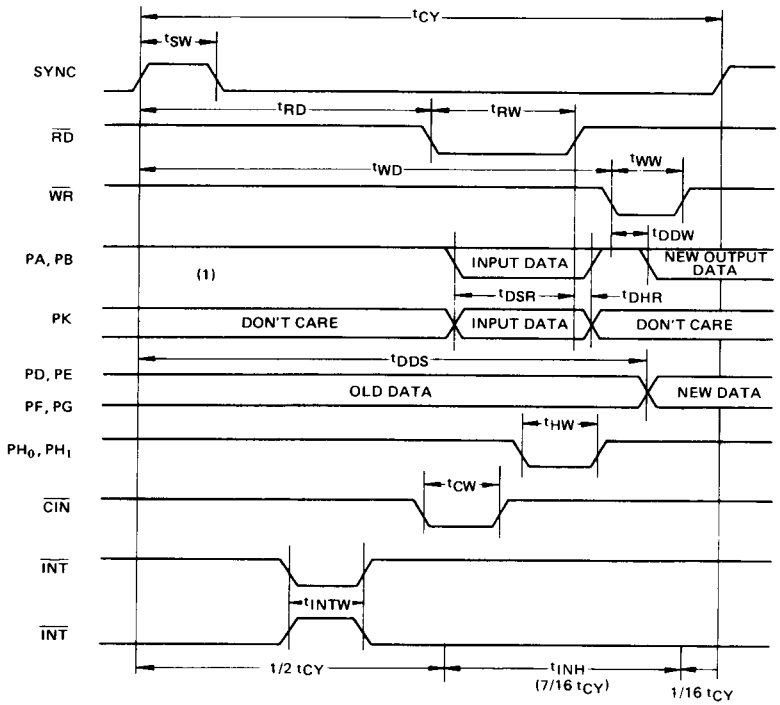
TIMING CHARTS

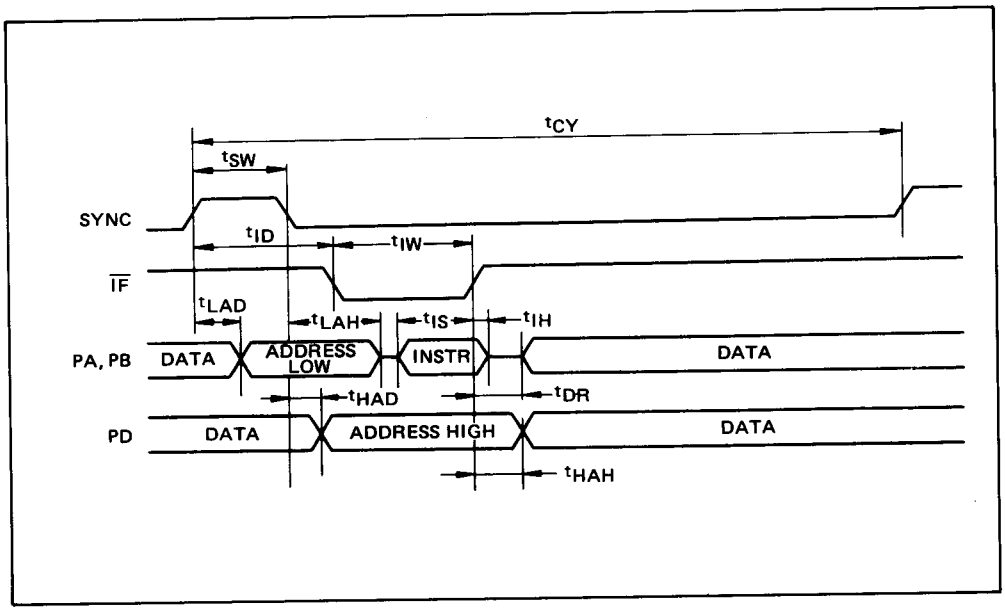


Note: (1) All 'ONES' must be output before reading port A or B.

A.C. CHARACTERISTICS (EXTERNAL ROM MODE)

(V_{DD} = 5V±10%, Ta = −40° to +85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Cycle Time	t_{CY}		7.6			μS
Sync Pulse Width	t_{SW}		0.95			μS
$\overline{IF}$ Pulse Width	t_{IW}		1.425			μS
Sync ↑ to $\overline{IF}$ ↓	t_{ID}	C_L = 50pF	3/16 t_{CY} + 1			μS
Address Low Delay	t_{LAD}	C_L = 50pF			0.8	μS
Address Low Hold	t_{LAH}		1/16 t_{CY}		1/16 t_{CY}+1	μS
Instruction Setup	t_{IS}		1/16 t_{CY}			μS
Instruction Hold	t_{IH}				20	nS
Data Recovery	t_{DR}	C_L = 50pF	0		0.8	μS
Address High Delay	t_{HAD}	C_L = 50pF			0.5	μS
Address High Hold	t_{HAH}		0		0.5	μS

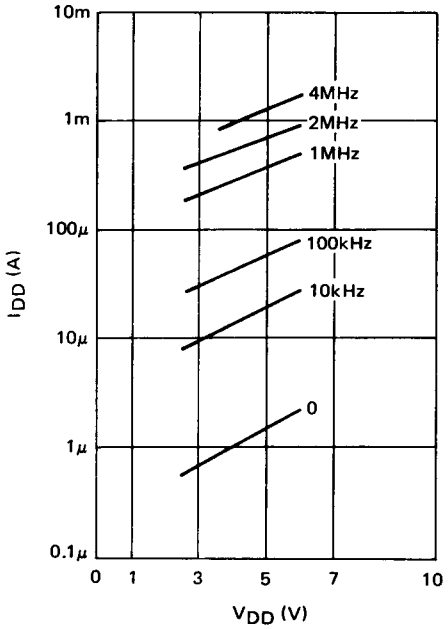


Cycle Dependent Timings	4MHz	2MHz	1MHz	500kHz
1/16t_{CY}	0.5μS	1μS	2μS	4μS
1/16t_{CY}+1	1.5μS	2μS	3μS	5μS
3/16t_{CY}+1	2.5μS	4μS	7μS	13μS
4/16t_{CY}−1	1μS	3μS	7μS	15μS
1/2t_{CY}+1	5μS	9μS	17μS	33μS
7/16t_{CY}	3.5μS	7μS	14μS	28μS
13/16t_{CY}+1	7.5μS	14μS	27μS	53μS

TYPICAL PERFORMANCE CURVES

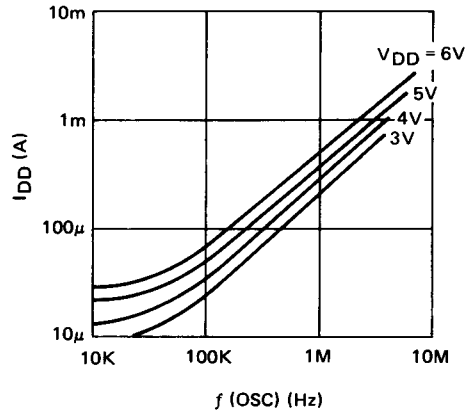
Supply Current vs Supply Voltage

(Ta = 25°C, No Load)



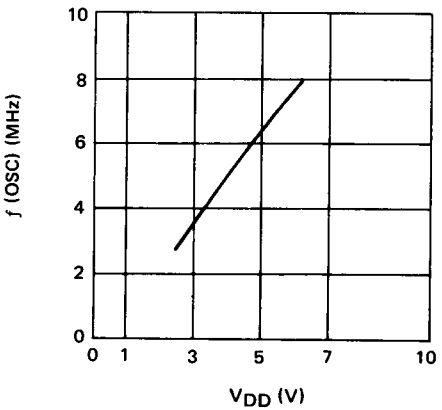
Supply Current vs Oscillator Frequency

(Ta = 25°C, No Load)



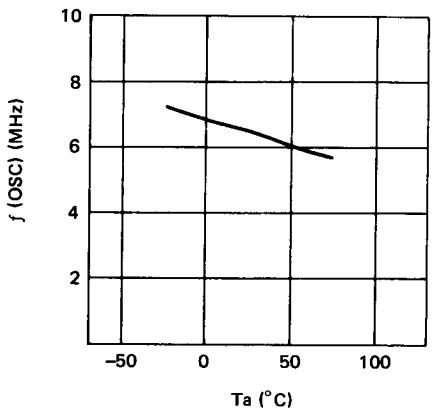
Oscillator Frequency vs Supply Voltage

(Ta = 25°C, C_L = 50pF)

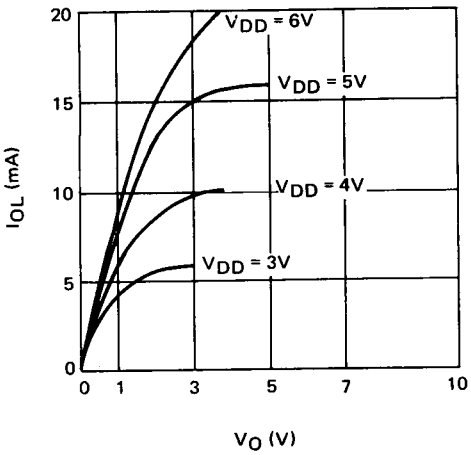


Oscillator Frequency vs Temperature

(C_L = 50pF)

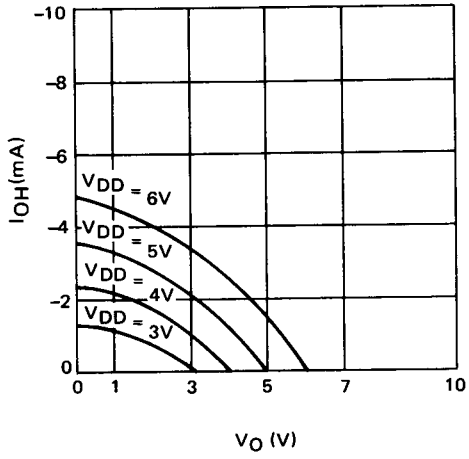


Low Current Out vs Voltage



High Current Out vs Voltage

(Ta = 25°C, Except PA, PB)



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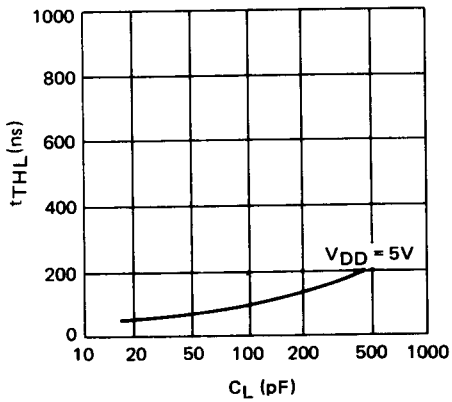
Fall Time vs Load

(Ta = 25°C, PA, PB, PD, PE, $\overline{RD}$, $\overline{WR}$, $\overline{IF}$, SYNC)



Rise Time vs Load

(Ta = 25°C, PD, PE, $\overline{RD}$, $\overline{WR}$, $\overline{IF}$, SYNC)