# MOS DIGITAL INTEGRATED CIRCUIT
# μPD1703C-011

## PHASE LOCKED LOOP FREQUENCY SYNTHESIZER
## FM/AM DIGITAL TUNING SYSTEM CONTROLLER
## CMOS LSI

The μPD1703C-011 is a CMOS LSI designed for using as a PLL Frequency Synthesizer Digital Tuning System Controller. The μPD1703C 011 provides a set of fluorescent indicator panel (FIP) segment drivers, a clock generator and a power-on clear circuit. The μPD1703C-011 is packaged in a 28 pin slim dual in-line package (DIP).

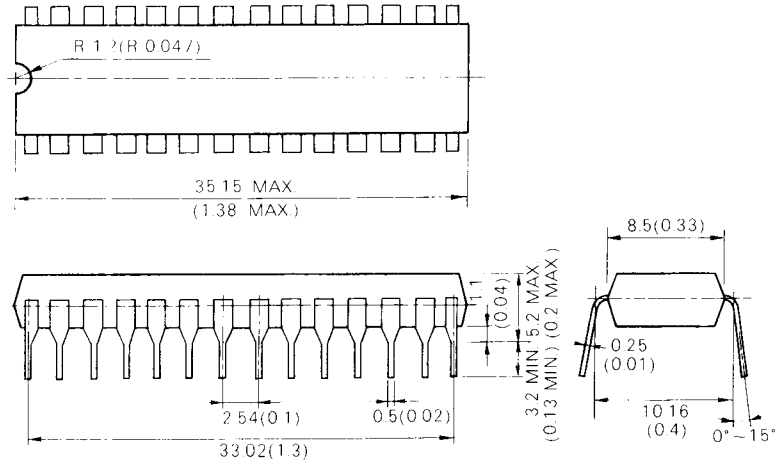
### FEATURES

- PLL, swallow counter and system controller are realized in a single chip.
- Fluorescent indicator panel driver incorporated (segment outputs)
- Internal display decorder for 4.5 digit multiplexed display
- Very low stand-by current···less than 10 μA
- High speed and low power consumption due to CMOS
- High reference frequency due to pulse swallowing (FM band: 25 kHz)
  It results in a high carrier-to-noise ratio.
- Internal clock oscillator and divider circuit.
- Automatic power-on clear without any external components.
- Preset memory address display (External latch/decorder is required.)
- Display brightness control (DIMMER) · · · · · Duty ratio 1 : 4
- FM/AM tuner · · · · · U.S., Europe and Japan bands
- External programmable IF offset for FM band (10.650 MHz, 10.675 MHz, 10.700 MHz, 10.725 MHz)

### FUNCTION OF TUNER

- Automatic up or down search (SEEK)
- Manual up or down search
- Preset station memory call
  Preset station memory . . . . . .FM: 6 stations, AM: 6 stations
- Last station memory . . . . . FM: 1 station, AM: 1 station

### PACKAGE DIMENSIONS Unit: mm (inches)



## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | −0.3 to +6.0 | V |
| Input Voltage | $V_I$ | −0.3 to $V_{DD}$ | V |
| Output Voltage | $V_O$ | −0.3 to $V_{DD}$ | V |
| Output Breakdown Voltage * | $V_{BDS}$ | −35 | V |
| Output Current | $I_{OH}$ | −10 | mA |
| Storage Temperature | Tstg | −55 to +125 | °C |
| Operating Temperature | Topt | −35 to +75 | °C |

* : Segment Output Terminals (P-ch open drain)

## ELECTRICAL CHARACTERISTICS (Ta=−35 to +75 °C, $V_{DD}$=4.5 to 5.5 V)

| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| High Level Input Voltage | $V_{IH1}$ | 0.8$V_{DD}$ | | $V_{DD}$ | V | SD terminal |
| | $V_{IH2}$ | 0.7$V_{DD}$ | | $V_{DD}$ | V | CE terminal |
| | $V_{IH3}$ | 0.6$V_{DD}$ | | $V_{DD}$ | V | K0 to K3 terminals |
| Low Level Input Voltage | $V_{IL1}$ | 0 | | 0.3$V_{DD}$ | V | CE terminal |
| | $V_{IL2}$ | 0 | | 0.2$V_{DD}$ | V | SD, K0 to K3 terminals |
| High Level Output Voltage | $V_{OH1}$ | 4.0 | | | V | EO, D, MUTE: $I_{OH}$=−0.5 mA |
| | $V_{OH2}$ | 3.0 | | | V | SEG: $I_{OH}$=−0.5 mA |
| | $V_{OH3}$ | 4.0 | | | V | PSC: $I_{OH}$=−0.2 mA |
| Low Level Output Voltage | $V_{OL1}$ | | | 0.5 | V | EO: $I_{OL}$=0.5 mA |
| | $V_{OL2}$ | | | 0.5 | V | D, MUTE, PSC: $I_{OL}$=0.2 mA |
| High Level Input Current | $I_{IH}$ | 5.0 | 25 | 100 | μA | K: $V_I$=$V_{DD}$=5.0 V |
| Frequency Response | fin1 | 0.5 | | 2.5 | MHz | AM: vi=1.0Vp-p, DC cut sine wave |
| | fin2 | 0.5 | | 8.8 | MHz | FM: vi=0.8Vp-p, DC cut square wave |
| Supply Voltage Rise Time | Tr | | | 0.5 | s | $V_{DD}$: 0 → 4.5 V |
| Supply Current | $I_{DD}$ | | | 10 | μA | CE: Low Level |
| Output Off Leak Current | $I_{OFF}$ | | | −5.0 | μA | SEG: $V_{DS}$=−30 V |

## SYSTEM DESCRIPTION

NEC's Digital Tuning System provides full electronic control of a vari-cap tuned FM/AM radio receiver and stereo. The block diagram of the system is shown in Fig. 1. This is a Phase Locked Loop Digital Tuning System which consists of two integrated circuits; controller plus PLL in a single chip, and two-modulus prescaler.

The controller chip (μPD1703C-011) provides Phase Locked Loop capability with on-chip frequency division, a reference oscillator whose frequency is controlled by an external crystal of 4.5 MHz, and phase comparator circuitry. It accepts directly an AM local oscillator signal and an FM signal from two-modulus prescaler (μPB553AC), and outputs control signals for closed loop operation of these oscillators. The outputs drives filters for supplying analog voltages to the vari-cap tuners. The controller also provides the signals to drive the display. The frequency of the tuned station is displayed on a 4.5 digit multiplexed display. Six favorite stations on each band can be stored as well as "last stations tuned" information.

The two-modulus prescaler (μPB553AC) is suitable for pulse swallowing in this system.

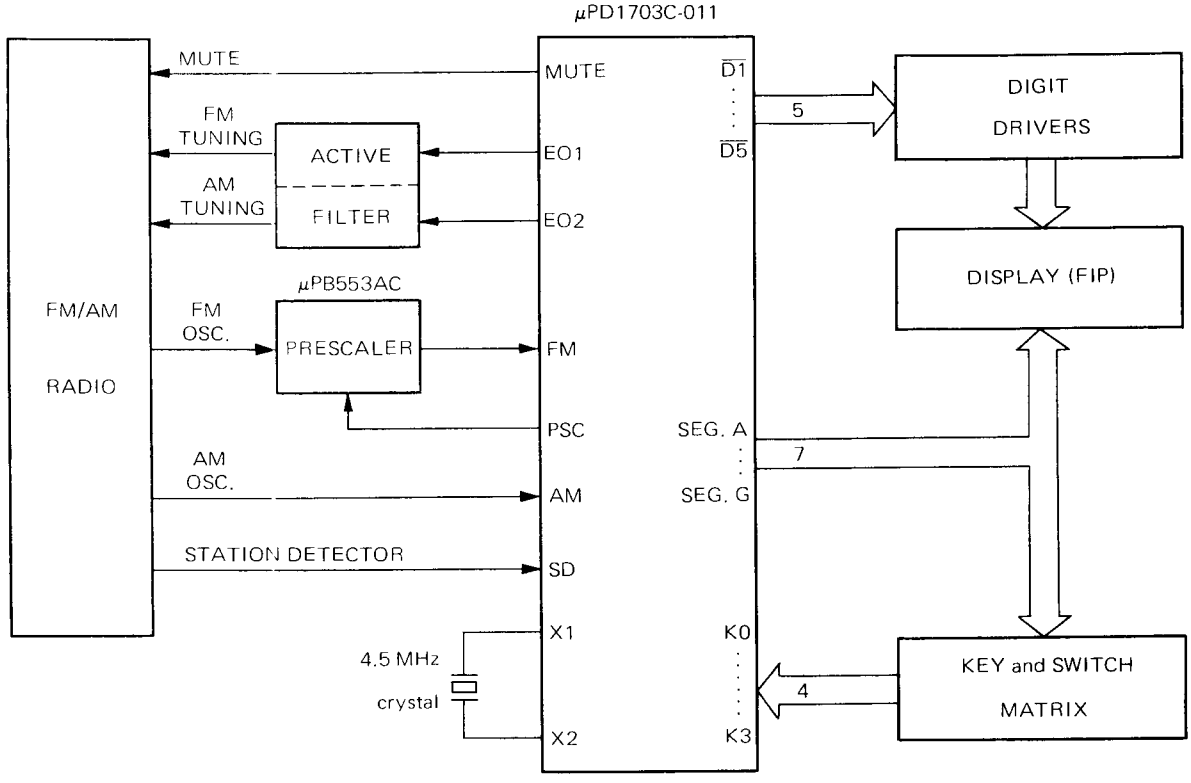
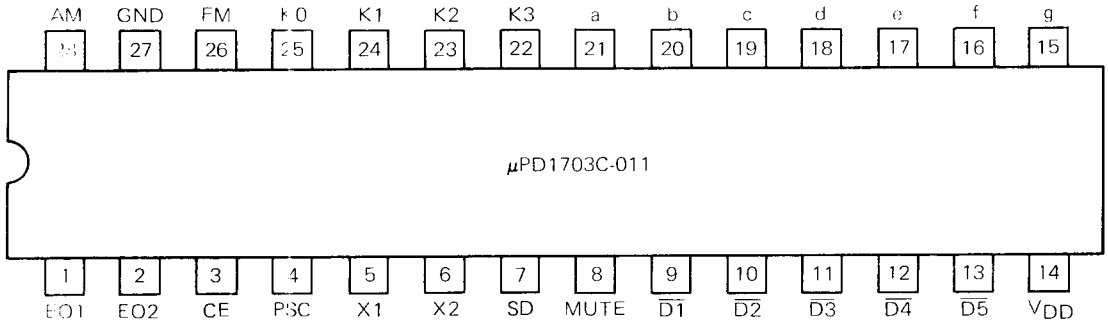



Fig. 1 BLOCK DIAGRAM

## PIN CONNECTION (Top View)




## EXPLANATION OF INPUT AND OUTPUT TERMINALS

| | |
|---|---|
| EO1<br>EO2 | These three-state outputs are used (via active filters) to supply analog voltages to the tuner vari-cap for controlling the local oscillators. |
| CE | This input is used to designate the stand-by mode to the chip.<br>It is low to designate the stand-by mode. (PLL: disable, display: off, clock generator: stop) |
| PSC | This output is used to control the division ratio of the FM two-modulus prescaler (μPB553AC). |
| X1, X2 | These inputs are for connection to a 4.5 MHz crystal. |
| SD | This input is used to control the station searching operation (AU/AD). It is high to indicate the presence of a station and the operation is terminated. |
| MUTE | This output line is high to mute the radio in the case of station change, band change, and so on. |
| $\overline{D1}$ to $\overline{D5}$ | These outputs are used as digit drivers for the display. (Active low) |
| $V_{DD}$ | This is a 4.5 to 5.5 volt supply for the chip. |
| a to g | These outputs are p-ch open drain used as segment drivers for the display. They are also used as vertical drive for the control key and mode switch matrix. |
| K0 to K3 | These inputs are from seven by four matrix. Various functions are entered through the matrix. See Fig. 2 for the matrix assignments. |
| FM | This is the FM band local oscillator input. The frequency is divided by 16/17 using a two-modulus prescaler (μPB553AC). |
| GND | System ground. |
| AM | This is the AM band local oscillator input. |

## CONTROL KEY AND MODE SWITCH MATRIX

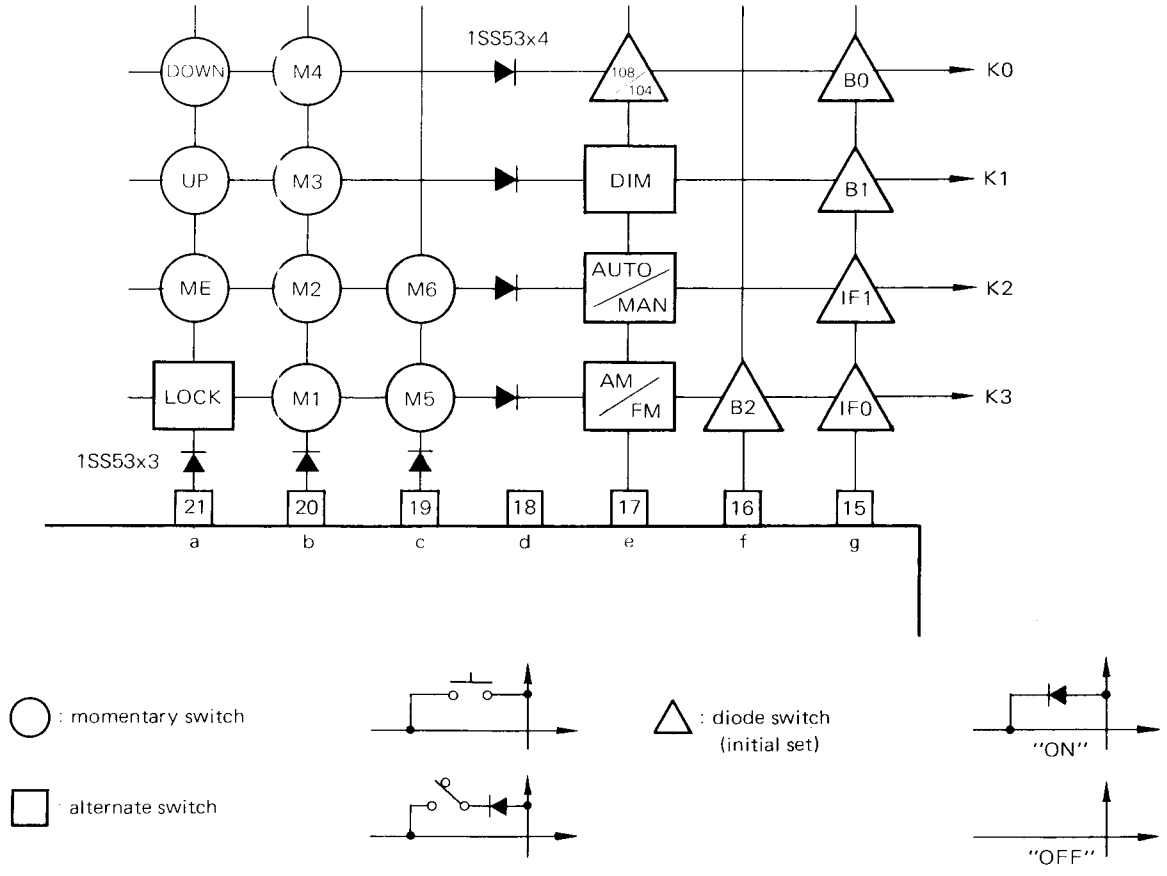



Fig. 2

- **Searching of the station**

  UP, DOWN
  * AUTO/MANUAL switch: ON (SEEK)
    A momentary depression causes automatic up or down searching by the speed of 80 ms/ch until SD terminal is activated (active high) or any key is depressed.
  * AUTO/MANUAL switch: OFF (Manual searching)
    A momentary depression will tune to next channel, and continuous depression more than 0.5 second allows traversing up or down the entire band by the speed of 80 ms until the key is released.

- **Preset of the station**

  ME — The tuning information is stored into internal RAM by depressing ME key and then desired memory key within 5 seconds from the time ME key was initially depressed. If any key is depressed in this period, the ME function is cancelled.

  M1 to M6 — Six favorite stations can be recalled from internal RAM for each band. When it is switched from one band to the other band, it will tune to "Last-tuned to station" on that band. Each time a station is changed, the controller provides a signal to mute the tuner.

- **Selection of the radio band**

  B0, B1 These switches are for selection of the district.

  AM/FM This switch is for selection of the radio band.

  B2 This switch is for selection of the receiving band and channel spacing of AM radio for U.S. band.

| B0 | B1 | B2 | AM/FM | Selected Band | | | |
|---|---|---|---|---|---|---|---|
| | | | | District | Receiving Frequency | Channel Spacing | IF |
| off | off | X | off | FM Japan | 76.1 to 89.9 MHz | 100 kHz | *1 |
| | | | on | AM Japan | 522 to 1611 kHz | 9 kHz | 450 kHz |
| on | off | X | off | FM Europe | 87.5 to 108.0 MHz *2 | 50 kHz | *1 |
| | | | on | AM Europe | 522 to 1611 kHz | 9 kHz | 450 kHz |
| off | on | X | off | FM U.S. | 87.9 to 107.9 MHz | 200 kHz | *1 |
| | | on | on | AM U.S. | 522 to 1611 kHz | 9 kHz | 450 kHz |
| | | off | on | AM U.S. | 530 to 1620 kHz | 10 kHz | 450 kHz |

X : Don't care.

Table 1.

*1 FM band IF offset

IF0, IF1 These switches program the chip to accept 4 different intermediate frequencies for each band in 25 kHz steps.

| IF0 | IF1 | Intermediate Frequency (MHz) | | |
|---|---|---|---|---|
| | | Japan | U.S. | Europe |
| off | on | 10.750 | 10.650 | 10.650 |
| on | on | 10.725 | 10.675 | 10.675 |
| off | off | 10.700 | 10.700 | 10.700 |
| on | off | 10.675 | 10.725 | 10.725 |

Table 2.

*2 108/104 This switch is for selection of receiving frequency of FM radio for Europe band.

| 108/104 | Receiving Frequency |
|---|---|
| on | 87.50 to 108.00 MHz |
| off | 87.50 to 104.00 MHz |

Table 3.

- **Display interface**

  The center frequency of tuned station is displayed on a 4.5 digit FIP. The μPD1703C-011 provides direct interface to the FIP. The μPD1703C-011 interfaces with all the devices requiring up to 30 V levels. The segment outputs go directly to the segments (anodes) of the multi-digit 7 segment FIP. The digit outputs go to PNP transistor array to drive the digits (grids) of the FIP. The LED display can be driven by using appropriate interface circuits.

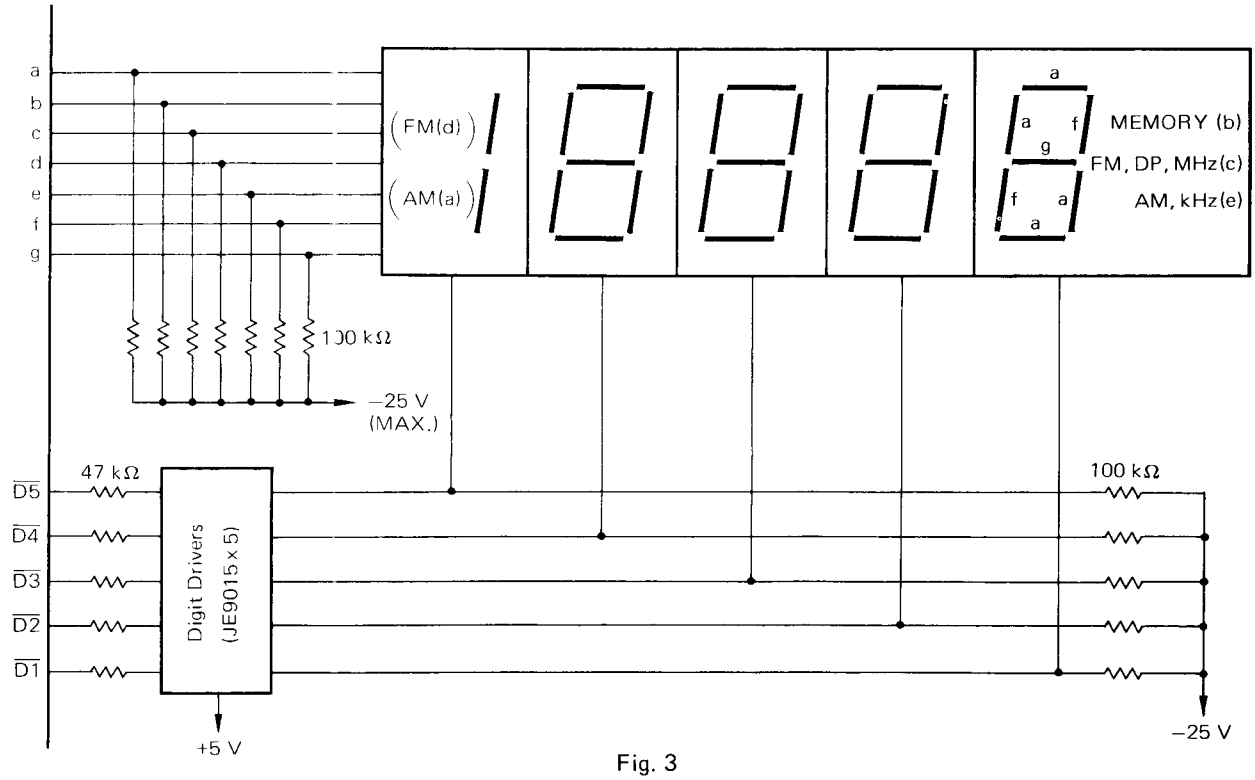
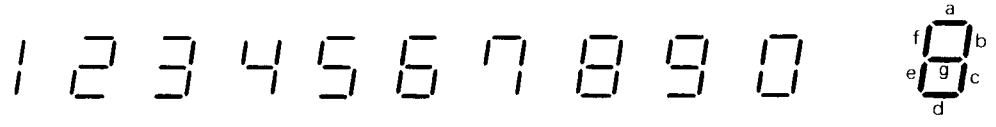



Fig. 3

- **Display format**

  ○ Segment Pattern




- **Display brightness control (DIMMER)**

  DIM — This switch is for selection of display brightness.

  ON . . . . . Display brightness is reduced. (Duty factor: 1/28)

  OFF . . . . . Display brightness is ordinary. (Duty factor: 1/7)

- **Protection from the miss key input**

  LOCK — This switch is for protection from miss key input.

  ON . . . . . All of the momentary keys input are disabled.

  OFF . . . . . All of the momentary keys input are enabled.

- **Protection of the key chattering**

  * Key make time . . . . . less than 15 ms
  * Key break time . . . . . less than 15 ms

- **Preset memory address display**

  In the case of memorizing the displayed frequency or recalling a preset memory, the chip provides the data to display preset memory address corresponded to the disired memory key.

  At the timing T2 of digit output D5, the data of memory address are provided segment output e, f and g. The data are binary coded decimal (BCD).

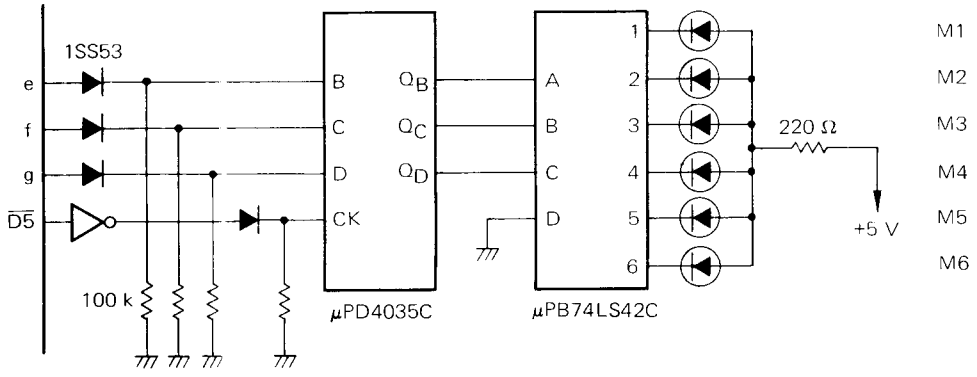



Fig. 4

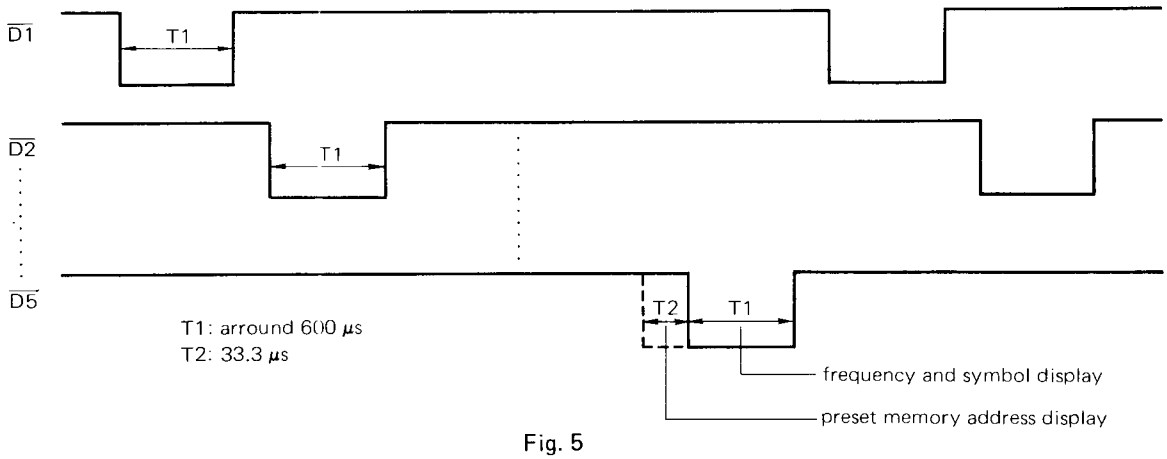



Fig. 5

* The segment output at the timing T1, T2 of digit output $\overline{D5}$ is as follows.

| Segment / Timing | a | b | c | d | e | f | g |
|---|---|---|---|---|---|---|---|
| T1 | (AM) | (1) | (1) | (FM/DP) | blank | | |
| T2 | blank | | | | BCD output | | |

Table 4.

* Segment output and preset memory address.

| g | f | e | Address |
|---|---|---|---|
| 0 | 0 | 1 | M1 |
| 0 | 1 | 0 | M2 |
| 0 | 1 | 1 | M3 |
| 1 | 0 | 0 | M4 |
| 1 | 0 | 1 | M5 |
| 1 | 1 | 0 | M6 |

Table 5.

## APPLICATION CIRCUIT