

# TMC 93LC46/56/57/66/86

## 1K/2K/2K/4K/16K-Bit Microwire Serial EEPROM

### FEATURES

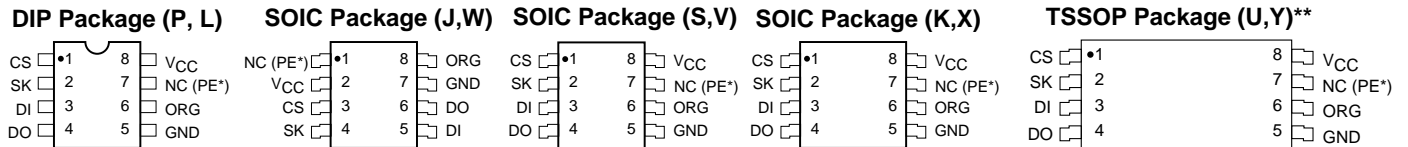
- High speed operation:
  - 93LC46/56/57/66 : 1MHz
  - 93LC86 : 3MHz
- Low power CMOS technology
- 1.8 to 6.0 volt operation
- Selectable x8 or x16 memory organization
- Self-timed write cycle with auto-clear
- Hardware and software write protection
- Power-up inadvertant write protection
- 1,000,000 Program/erase cycles
- 100 year data retention
- Commercial, industrial and automotive temperature ranges
- Sequential read (except TMC93LC46)
- Program enable (PE) pin (TMC93LC86 only)

### DESCRIPTION

The 93LC46/56/57/66/86 are 1K/2K/2K/4K/16K-bit Serial EEPROM memory devices which are configured as either registers of 16 bits (ORG pin at V<sub>CC</sub>) or 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The 93LC46/56/57/66/86 are manufactured using TMC's advanced

CMOS EEPROM floating gate technology. The devices are designed to endure 1,000,000 program/erase cycles and have a data retention of 100 years. The devices are available in 8-pin DIP, 8-pin SOIC or 8-pin TSSOP packages.

### PIN CONFIGURATION

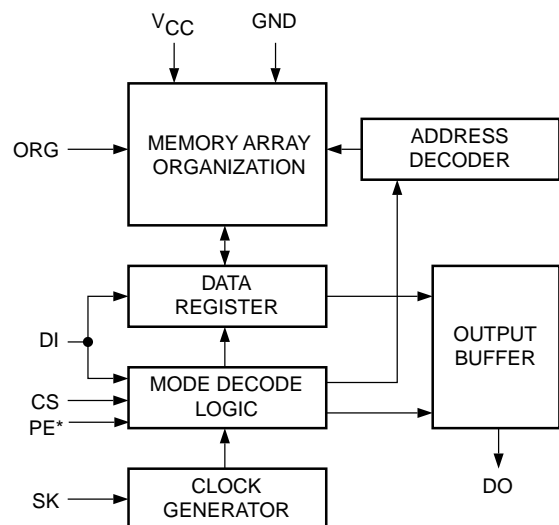


### PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V <sub>CC</sub>	+1.8 to 6.0V Power Supply
GND	Ground
ORG	Memory Organization
NC	No Connection
PE*	Program Enable

Note: When the ORG pin is connected to V<sub>CC</sub>, the x16 organization is selected. When it is connected to ground, the x8 pin is selected. If the ORG pin is left unconnected, then an internal pullup device will select the x16 organization.

### BLOCK DIAGRAM



93LC46/56/57/66/86 F02

**ABSOLUTE MAXIMUM RATINGS\***

Temperature Under Bias .....	-55°C to +125°C
Storage Temperature .....	-65°C to +150°C
Voltage on any Pin with Respect to Ground <sup>(1)</sup> .....	-2.0V to +V <sub>CC</sub> +2.0V
V <sub>CC</sub> with Respect to Ground .....	-2.0V to +7.0V
Package Power Dissipation Capability (T <sub>A</sub> = 25°C) .....	1.0W
Lead Soldering Temperature (10 secs) .....	300°C
Output Short Circuit Current <sup>(2)</sup> .....	100 mA

**\*COMMENT**

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

**RELIABILITY CHARACTERISTICS**

Symbol	Parameter	Reference Test Method	Min	Typ	Max	Units
N <sub>END</sub> <sup>(3)</sup>	Endurance	MIL-STD-883, Test Method 1033	1,000,000			Cycles/Byte
T <sub>DR</sub> <sup>(3)</sup>	Data Retention	MIL-STD-883, Test Method 1008	100			Years
V <sub>ZAP</sub> <sup>(3)</sup>	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000			Volts
I <sub>LTH</sub> <sup>(3)(4)</sup>	Latch-Up	JEDEC Standard 17	100			mA

**D.C. OPERATING CHARACTERISTICS**

V<sub>CC</sub> = +1.8V to +6.0V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I <sub>CC1</sub>	Power Supply Current (Operating Write)	f <sub>SK</sub> = 1MHz V <sub>CC</sub> = 5.0V			3	mA
I <sub>CC2</sub>	Power Supply Current (Operating Read)	f <sub>SK</sub> = 1MHz V <sub>CC</sub> = 5.0V			500	μA
I <sub>SB1</sub>	Power Supply Current (Standby) (x8 Mode)	CS = 0V ORG=GND			10	μA
I <sub>SB2</sub> <sup>(5)</sup>	Power Supply Current (Standby) (x16Mode)	CS=0V ORG=Float or V <sub>CC</sub>			0	μA
I <sub>LI</sub>	Input Leakage Current	V <sub>IN</sub> = 0V to V <sub>CC</sub>			1	μA
I <sub>LO</sub>	Output Leakage Current (Including ORG pin)	V <sub>OUT</sub> = 0V to V <sub>CC</sub> , CS = 0V			1	μA
V <sub>IL1</sub>	Input Low Voltage	4.5V ≤ V <sub>CC</sub> < 5.5V	-0.1		0.8	V
V <sub>IH1</sub>	Input High Voltage	4.5V ≤ V <sub>CC</sub> < 5.5V	2		V <sub>CC</sub> + 1	V
V <sub>IL2</sub>	Input Low Voltage	1.8V ≤ V <sub>CC</sub> < 4.5V	0		V <sub>CC</sub> x 0.2	V
V <sub>IH2</sub>	Input High Voltage	4.8V ≤ V <sub>CC</sub> < 4.5V	V <sub>CC</sub> x 0.7		V <sub>CC</sub> +1	V
V <sub>OL1</sub>	Output Low Voltage	4.5V ≤ V <sub>CC</sub> < 5.5V I <sub>OL</sub> = 2.1mA			0.4	V
V <sub>OH1</sub>	Output High Voltage	4.5V ≤ V <sub>CC</sub> < 5.5V I <sub>OH</sub> = -400μA	2.4			V
V <sub>OL2</sub>	Output Low Voltage	1.8V ≤ V <sub>CC</sub> < 4.5V I <sub>OL</sub> = 1mA			0.2	V
V <sub>OH2</sub>	Output High Voltage	1.8V ≤ V <sub>CC</sub> < 4.5V I <sub>OH</sub> = -100μA	V <sub>CC</sub> - 0.2			V

**Note:**

- (1) The minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V<sub>CC</sub> +0.5V, which may overshoot to V<sub>CC</sub> +2.0V for periods of less than 20 ns.
- (2) Output shorted for no more than one second. No more than one output shorted at a time.
- (3) This parameter is tested initially and after a design or process change that affects the parameter.
- (4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1V to V<sub>CC</sub> +1V.
- (5) Standby Current (I<sub>SB2</sub>)=0μA (<900nA) for 93LC46/56/57/66, (I<sub>SB2</sub>)=2μA for 93LC86.

## PIN CAPACITANCE

Symbol	Test	Conditions	Min	Typ	Max	Units
C <sub>OUT</sub> <sup>(3)</sup>	Output Capacitance (DO)	V <sub>OUT</sub> =0V			5	pF
C <sub>IN</sub> <sup>(3)</sup>	Input Capacitance (CS, SK, DI, ORG)	V <sub>IN</sub> =0V			5	pF

## INSTRUCTION SET

Instruction	Device Type	Start Bit	Opcode	Address		Data		Comments	PE <sup>(2)</sup>
				x8	x16	x8	x16		
READ	93LC46	1	10	A6-A0	A5-A0			Read Address AN-A0	X
	93LC56 <sup>(1)</sup>	1	10	A8-A0	A7-A0				
	93LC66	1	10	A8-A0	A7-A0				
	93LC57	1	10	A7-A0	A6-A0				
	93LC86	1	10	A10-A0	A9-A0				
ERASE	93LC46	1	11	A6-A0	A5-A0			Clear Address AN-A0	I
	93LC56 <sup>(1)</sup>	1	11	A8-A0	A7-A0				
	93LC66	1	11	A8-A0	A7-A0				
	93LC57	1	11	A7-A0	A6-A0				
	93LC86	1	11	A10-A0	A9-A0				
WRITE	93LC46	1	01	A6-A0	A5-A0	D7-D0	D15-D0	Write Address AN-A0	I
	93LC56 <sup>(1)</sup>	1	01	A8-A0	A7-A0	D7-D0	D15-D0		
	93LC66	1	01	A8-A0	A7-A0	D7-D0	D15-D0		
	93LC57	1	01	A7-A0	A6-A0	D7-D0	D15-D0		
	93LC86	1	01	A10-A0	A9-A0	D7-D0	D15-D0		
EWEN	93LC46	1	00	11XXXXX	11XXXX			Write Enable	X
	93LC56	1	00	11XXXXXXXX	11XXXXXXXX				
	93LC66	1	00	11XXXXXXXX	11XXXXXXXX				
	93LC57	1	00	11XXXXXX	11XXXXXX				
	93LC86	1	00	11XXXXXXXXXX	11XXXXXXXXXX				
EWDS	93LC46	1	00	00XXXXX	00XXXX			Write Disable	X
	93LC56	1	00	00XXXXXXXX	00XXXXXXXX				
	93LC66	1	00	00XXXXXXXX	00XXXXXXXX				
	93LC57	1	00	00XXXXXX	00XXXXXX				
	93LC86	1	00	00XXXXXXXXXX	00XXXXXXXXXX				
ERAL	93LC46	1	00	10XXXXX	10XXXX			Clear All Addresses	I
	93LC56	1	00	10XXXXXXXX	10XXXXXXXX				
	93LC66	1	00	10XXXXXXXX	10XXXXXXXX				
	93LC57	1	00	10XXXXXX	10XXXXXX				
	93LC86	1	00	10XXXXXXXXXX	10XXXXXXXXXX				
WRAL	93LC46	1	00	01XXXXX	01XXXX	D7-D0	D15-D0	Write All Addresses	I
	93LC56	1	00	01XXXXXXXX	01XXXXXXXX	D7-D0	D15-D0		
	93LC66	1	00	01XXXXXXXX	01XXXXXXXX	D7-D0	D15-D0		
	93LC57	1	00	01XXXXXX	01XXXXXX	D7-D0	D15-D0		
	93LC86	1	00	01XXXXXXXXXX	01XXXXXXXXXX	D7-D0	D15-D0		

Note:

- (1) Address bit A8 for 256x8 ORG and A7 for 128x16 ORG are "Don't Care" bits, but must be kept at either a "1" or "0" for READ, WRITE and ERASE commands.
- (2) Applicable only to 93LC86
- (3) This parameter is tested initially and after a design or process change that affects the parameter.

**A.C. CHARACTERISTICS (93LC46/56/57/66)**

SYMBOL	PARAMETER	Test Conditions	Limits						Units
			V <sub>CC</sub> = 1.8V-6V		V <sub>CC</sub> = 2.5V-6V		V <sub>CC</sub> = 4.5V-5.5V		
			Min	Max	Min	Max	Min	Max	
t <sub>CSS</sub>	CS Setup Time	C <sub>L</sub> = 100pF (3)	200		100		50		ns
t <sub>CSH</sub>	CS Hold Time		0		0		0		ns
t <sub>DIS</sub>	DI Setup Time		400		200		100		ns
t <sub>DIH</sub>	DI Hold Time		400		200		100		ns
t <sub>PD1</sub>	Output Delay to 1			1		0.5		0.25	μs
t <sub>PD0</sub>	Output Delay to 0			1		0.5		0.25	μs
t <sub>HZ</sub> <sup>(1)</sup>	Output Delay to High-Z			400		200		100	ns
t <sub>EW</sub>	Program/Erase Pulse Width			10		10		10	ms
t <sub>CSSMIN</sub>	Minimum CS Low Time		1		0.5		0.25		μs
t <sub>SKHI</sub>	Minimum SK High Time		1		0.5		0.25		μs
t <sub>SKLOW</sub>	Minimum SK Low Time		1		0.5		0.25		μs
t <sub>SV</sub>	Output Delay to Status Valid			1		0.5		0.25	μs
SK <sub>MAX</sub>	Maximum Clock Frequency		DC	250	DC	500	DC	1000	kHz

**A.C. CHARACTERISTICS (93LC86)**

SYMBOL	PARAMETER	Test Conditions	Limits						Units
			V <sub>CC</sub> = 1.8V-6V		V <sub>CC</sub> = 2.5V-6V		V <sub>CC</sub> = 4.5V-5.5V		
			Min	Max	Min	Max	Min	Max	
t <sub>CSS</sub>	CS Setup Time	C <sub>L</sub> = 100pF (3)	200		100		50		ns
t <sub>CSH</sub>	CS Hold Time		0		0		0		ns
t <sub>DIS</sub>	DI Setup Time		200		100		50		ns
t <sub>DIH</sub>	DI Hold Time		200		100		50		ns
t <sub>PD1</sub>	Output Delay to 1			1		0.5		0.15	μs
t <sub>PD0</sub>	Output Delay to 0			1		0.5		0.15	μs
t <sub>HZ</sub> <sup>(1)</sup>	Output Delay to High-Z			400		200		100	ns
t <sub>EW</sub>	Program/Erase Pulse Width			5		5		5	ms
t <sub>CSSMIN</sub>	Minimum CS Low Time		1		0.5		0.15		μs
t <sub>SKHI</sub>	Minimum SK High Time		1		0.5		0.15		μs
t <sub>SKLOW</sub>	Minimum SK Low Time		1		0.5		0.15		μs
t <sub>SV</sub>	Output Delay to Status Valid			1		0.5		0.1	μs
SK <sub>MAX</sub>	Maximum Clock Frequency		DC	500	DC	1000	DC	3000	kHz

NOTE:

(1) This parameter is tested initially and after a design or process change that affects the parameter.

**POWER-UP TIMING (1)(2)**

SYMBOL	PARAMETER	Max	Units
t <sub>PUR</sub>	Power-up to Read Operation	1	ms
t <sub>PUW</sub>	Power-up to Write Operation	1	ms

**NOTE:**

- (1) This parameter is tested initially and after a design or process change that affects the parameter.  
(2) t<sub>PUR</sub> and t<sub>PUW</sub> are the delays required from the time V<sub>CC</sub> is stable until the specified operation can be initiated.  
(3) The input levels and timing reference points are shown in "AC Test Conditions" table.

**A.C. TEST CONDITIONS**

Input Rise and Fall Times	≤ 50ns	
Input Pulse Voltages	0.4V to 2.4V	4.5V ≤ V <sub>CC</sub> ≤ 5.5V
Timing Reference Voltages	0.8V, 2.0V	4.5V ≤ V <sub>CC</sub> ≤ 5.5V
Input Pulse Voltages	0.2V <sub>CC</sub> to 0.7V <sub>CC</sub>	1.8V ≤ V <sub>CC</sub> ≤ 4.5V
Timing Reference Voltages	0.5V <sub>CC</sub>	1.8V ≤ V <sub>CC</sub> ≤ 4.5V

## DEVICE OPERATION

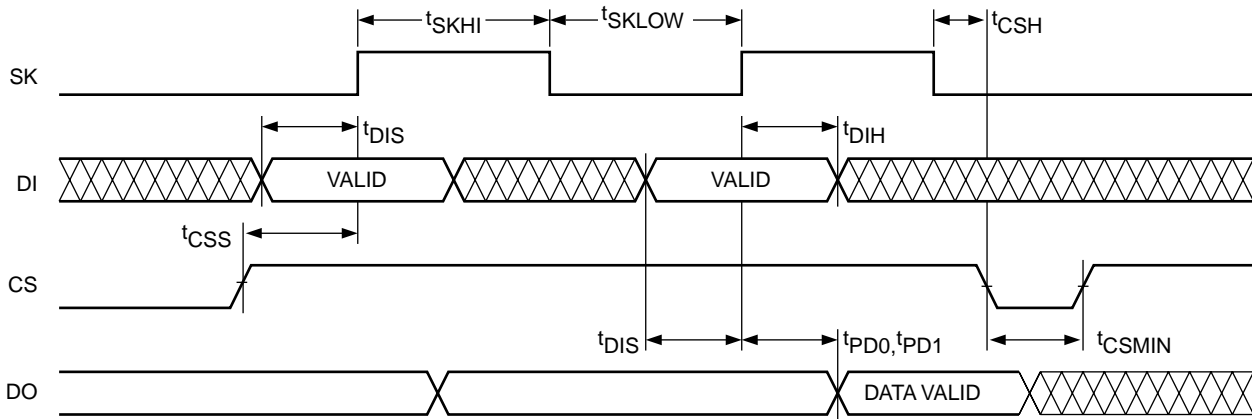
The 93LC46/56(57)66/86 is a 1024/2048/4096/16,384-bit nonvolatile memory intended for use with industry standard microprocessors. The 93LC46/56/57/66/86 can be organized as either registers of 16 bits or 8 bits. When organized as X16, seven 9-bit instructions for 93LC46; seven 10-bit instructions for 93LC57; seven 11-bit instructions for 93LC56 and 93LC66; seven 13-bit instructions for 93LC86; control the reading, writing and erase operations of the device. When organized as X8, seven 10-bit instructions for 93LC46; seven 11-bit instructions for 93LC57; seven 12-bit instructions for 93LC56 and 93LC66; seven 14-bit instructions for 93LC86; control the reading, writing and erase operations of the device. The 93LC46/56/57/66/86 operates on a single power supply and will generate on chip, the high voltage required during any write operation.

the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after the start of a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

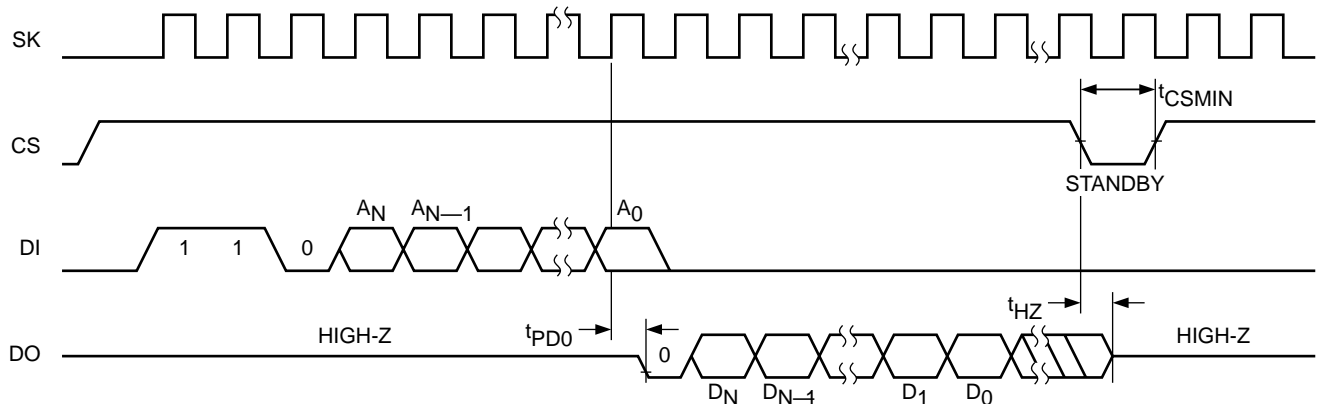
Instructions, addresses, and write data are clocked into

Figure 1. Synchronous Data Timing



93LC46/56/57/66/86 F03

Figure 2a. Read Instruction Timing (93LC46)



93LC46/56/57/66/86 F04

The format for all instructions sent to the device is a logical "1" start bit, a 2-bit (or 4-bit) opcode, 6-bit (93LC46)/7-bit (93LC57)/ 8-bit (93LC56 or 93LC66)/10-bit (93LC86) (an additional bit when organized X8) and for write operations a 16-bit data field (8-bit for X8 organizations).

*Note: This note is applicable only to 93LC86. The Write, Erase, Write all and Erase all instructions require PE=1. If PE is left floating, 93C86 is in Program Enabled mode. For Write Enable and Write Disable instruction PE=don't care.*

**Read**

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the 93LC46/56/57/66/86 will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay ( $t_{PD0}$  or  $t_{PD1}$ ).

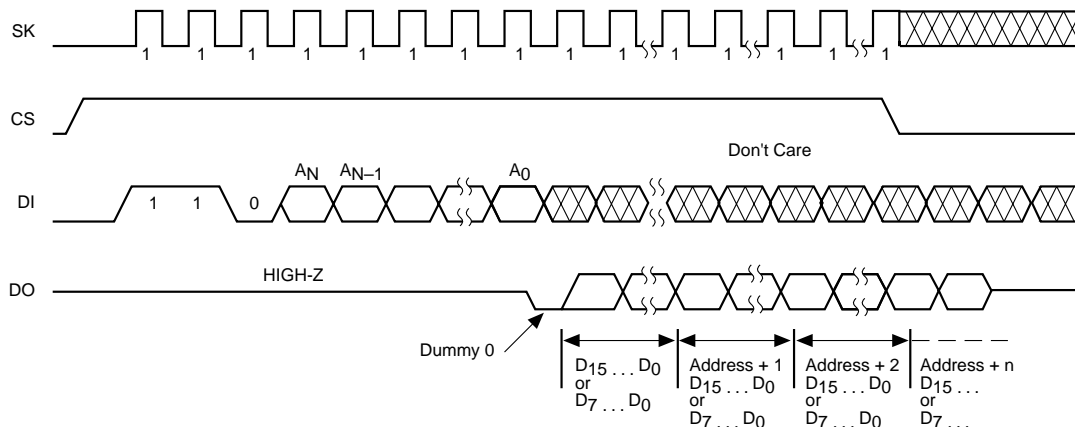
For the 93LC56/57/66/86, after the initial data word has been shifted out and CS remains asserted with the SK clock continuing to toggle, the device will automatically

increment to the next address and shift out the next data word in a sequential READ mode. As long as CS is continuously asserted and SK continues to toggle, the device will keep incrementing to the next address automatically until it reaches to the end of the address space, then loops back to address 0. In the sequential READ mode, only the initial data word is preceded by a dummy zero bit. All subsequent data words will follow without a dummy zero bit.

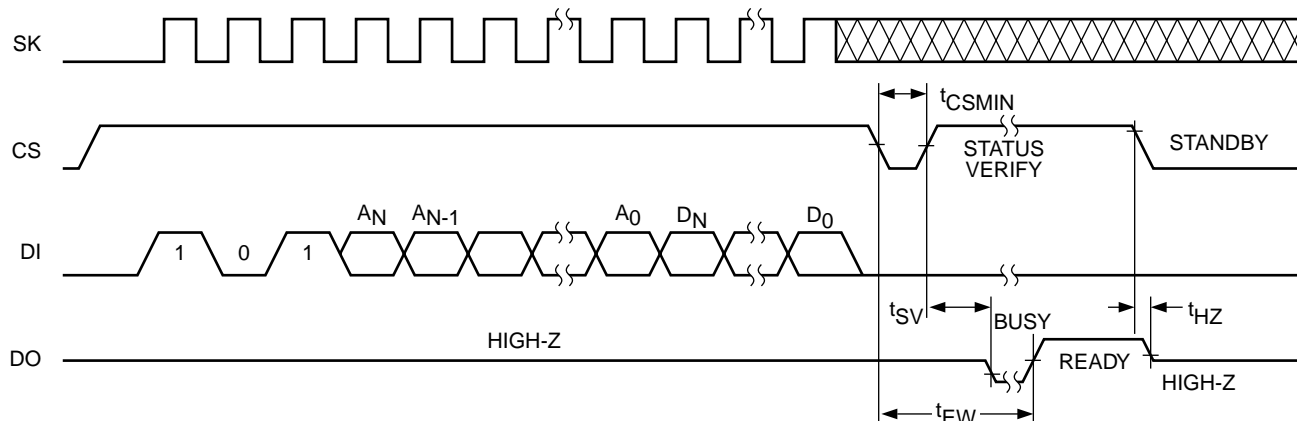
**Write**

After receiving a WRITE command, address and the data, the CS (Chip Select) pin must be deselected for a minimum of  $t_{CSMIN}$ . The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the 93LC46/56/57/66/86 can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before it is written into.

**Figure 2b. Read Instruction Timing (93LC56/57/66/86)**



**Figure 3. Write Instruction Timing**



**Erase**

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deasserted for a minimum of  $t_{CSMIN}$ . The falling edge of CS will start the self clocking clear cycle of the selected memory location. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the 93LC46/56/57/66/86 can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical “1” state.

**Erase/Write Enable and Disable**

The 93LC46/56/57/66/86 powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all 93LC46/56/57/66/86 write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

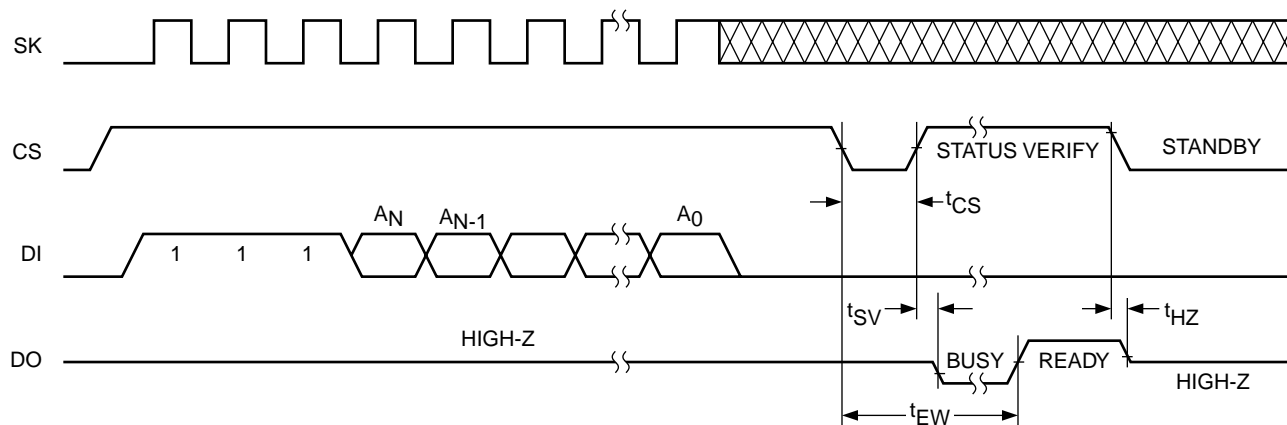
**Erase All**

Upon receiving an ERAL command, the CS (Chip Select) pin must be deselected for a minimum of  $t_{CSMIN}$ . The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the 93LC46/56/57/66/86 can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical “1” state.

**Write All**

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of  $t_{CSMIN}$ . The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. (Note 1.) The ready/busy status of the 93LC46/56/57/66/86 can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

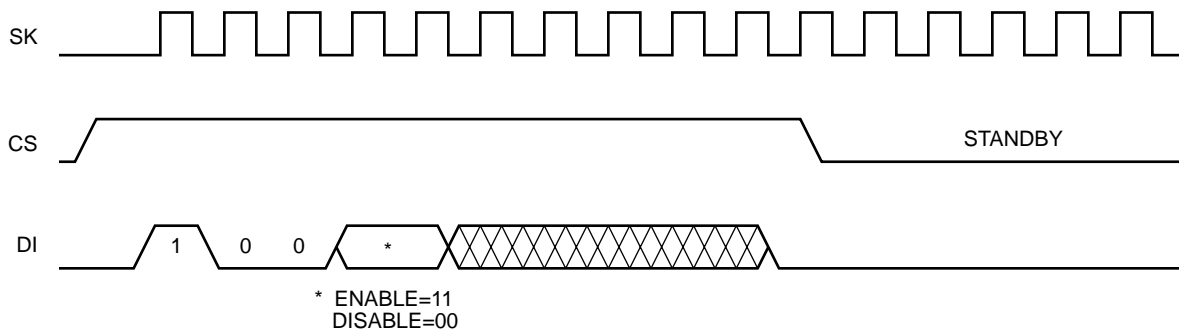
**Figure 4. Erase Instruction Timing**



93LC46/56/57/66/86 F06

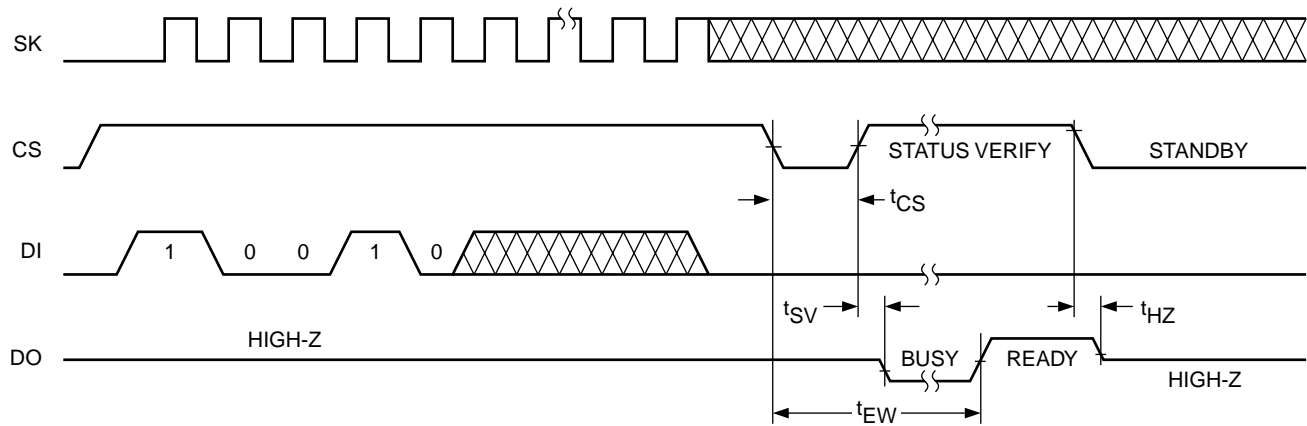


Figure 5. EWEN/EWDS Instruction Timing



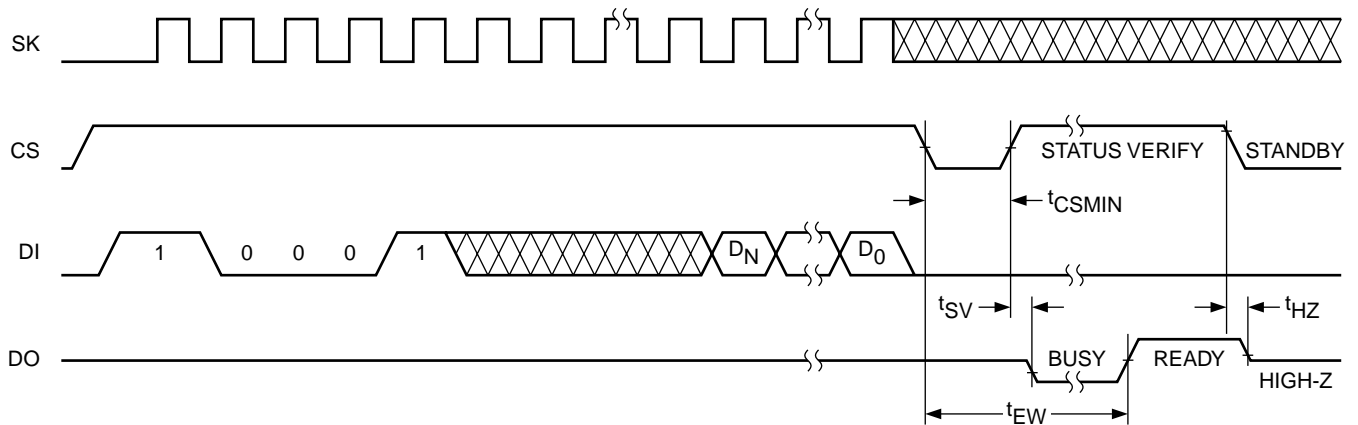
93LC46/56/57/66/86 F07

Figure 6. ERAL Instruction Timing



93LC46/56/57/66/86 F08

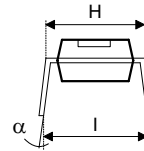
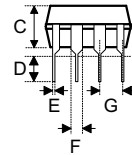
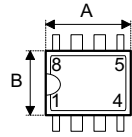
Figure 7. WRAL Instruction Timing



93LC46/56/57/66/86 F09

**Plastic DIP Outline Dimensions**

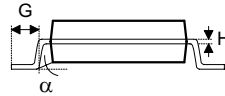
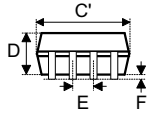
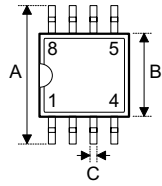
**8-pin DIP (300mil) Outline Dimensions**



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	355	—	375
B	240	—	260
C	125	—	135
D	125	—	145
E	16	—	20
F	50	—	70
G	—	100	—
H	295	—	315
I	335	—	375
$\alpha$	0°	—	15°

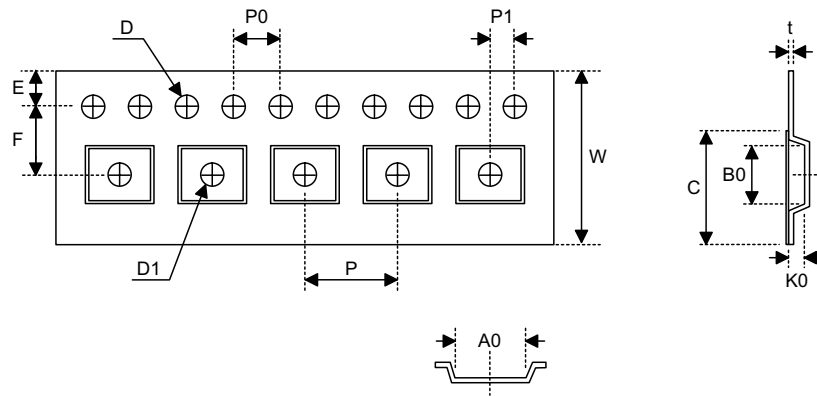
**SOP Outline Dimensions**

**8-pin SOP (150mil) Outline Dimensions**



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	228	—	244
B	149	—	157
C	14	—	20
C'	189	—	197
D	53	—	69
E	—	50	—
F	4	—	10
G	22	—	28
H	4	—	12
$\alpha$	0°	—	10°

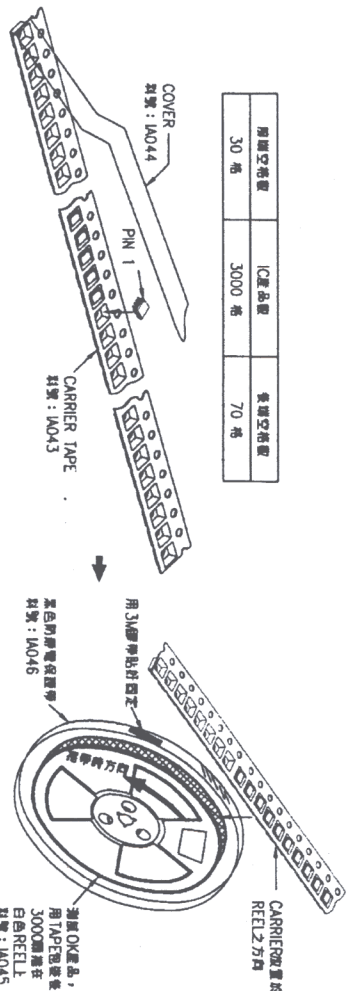
**Carrier Tape Dimensions**



**SOP 8N**

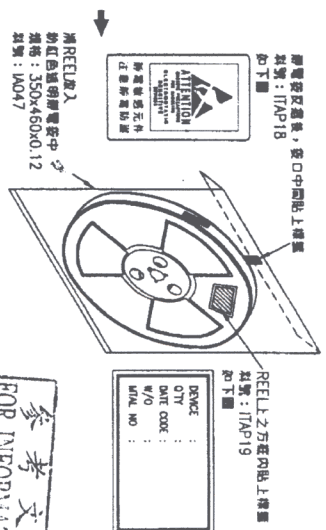
Symbol	Description	Dimensions in mm
W	Carrier Tape Width	12.0+0.3 -0.1
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	5.5±0.1
D	Perforation Diameter	1.55±0.1
D1	Cavity Hole Diameter	1.5+0.25
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	6.4±0.1
B0	Cavity Width	5.20±0.1
K0	Cavity Depth	2.1±0.1
t	Carrier Tape Thickness	0.3±0.05
C	Cover Tape Width	9.3

兩端空格數	IC邊空格數	卷端空格數
30 格	3000 格	70 格



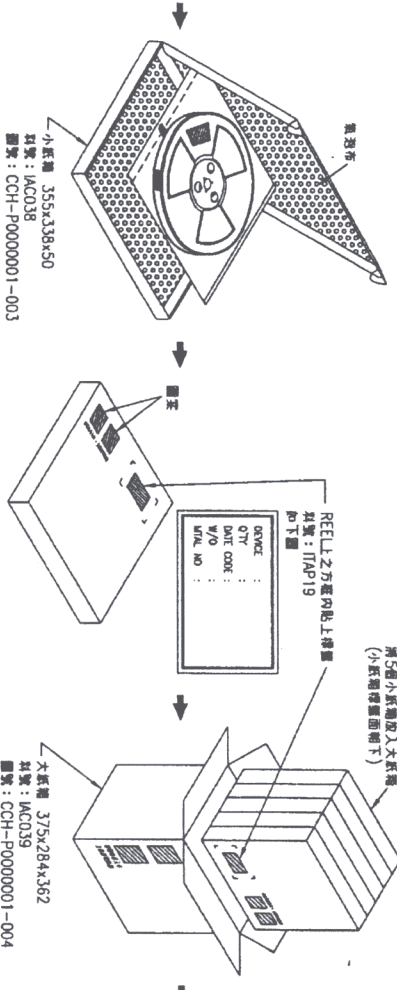
產品測試完成後與 TAPE 配置關係

將測試 OK 產品之 TAPE 捲到 REEL，  
外圍再加一黑色防靜電保護帶加以固定



將 REEL 上方框內貼上標籤，  
並放入防靜電袋內

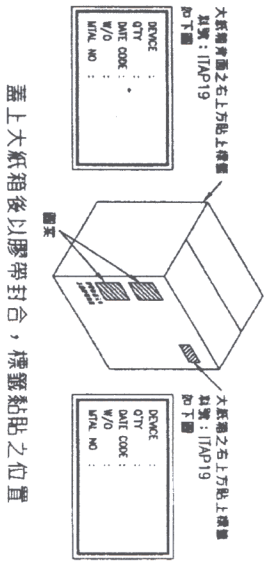
參考文件請  
FOR INFORMATION ONLY  
日期: 2003.5.15  
晶揚科技股份有限公司  
TMC Doc. Control Center



REEL 貼標籤面朝上，放入小紙箱內

蓋上小紙箱後，標籤黏貼之位置  
5 只小紙箱標籤面向下放入大紙箱  
不滿 5 只小紙箱者，仍需以大紙箱包裝，  
並以靜電海棉填滿

NOTES: 1. 每一紙箱只能裝同一批產品。  
2. 同一晶圓批，須同時出貨。  
3. 尾數箱不能與他批產品併批包裝出貨。  
4. 測試完不滿 3000 顆之產品，不以 REEL 包裝仍以 TUBE 裝管入庫。



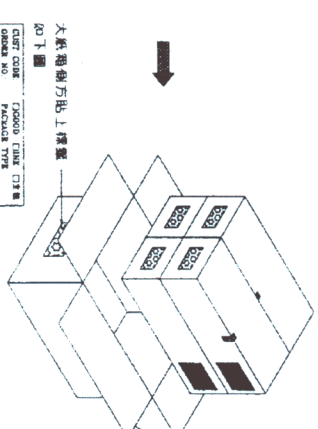
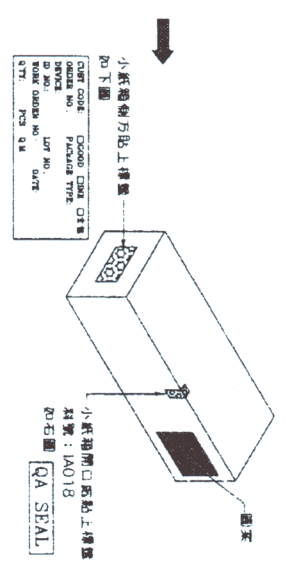
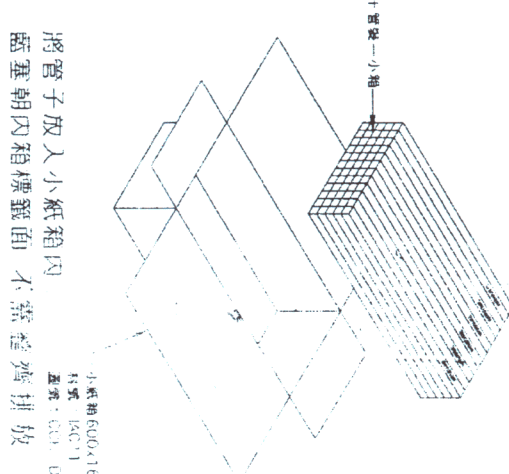
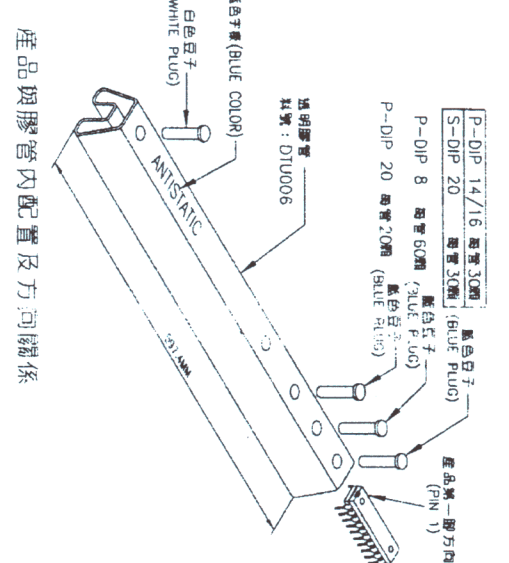
蓋上大紙箱後以膠帶封合，標籤黏貼之位置

REV	DESCRIPTION OF REVISION	TITLE
1	增加標券和空位用電壓標碼	晶揚科技 SOP 8L Tape REEL 標準包裝規範
2		
3		

DESIGNER	DATE	MATERIAL	SCALE	TITLE
AWR L001	9/11/06			晶揚科技 SOP 8L Tape REEL 標準包裝規範
CHECKER	DATE	PROCESSSES	SHEET NO	FILE
WJL	10/6/02		1 OF 1	E:\1\標準量具(量測設備)\PR-SOP TAPE.DWG
APPROVED	DATE	UNIT	QTY	THIRD ANGLE PROJECTION
Advison	10/6/02	MM	1	ALL DIMENSIONS IN MILLIMETERS





小紙箱標籤黏貼之位置  
 蓋上小紙箱盒蓋後，以透明膠帶封合

- 註：(1) 每一小箱只能裝同批產品。  
 (2) 不滿管時須反向放置於包裝箱內。  
 (3) 同一品圖批，須同時出貨。  
 (4) 尾數相同其包裝方式，箱內之間隙部份亦以防靜電泡綿填充至飽和為止。  
 (5) 小箱之尾數箱均需以大箱包裝出貨。

FORM EG00005C

4	修改管子標示	日期: 2002/07/29	製料員: [Signature]
3	修改管子標示	日期: 2002/07/29	製料員: [Signature]
2	ADD MODEL	日期: 2002/07/29	製料員: [Signature]
1	REV	日期: 2002/07/29	製料員: [Signature]

DESIGNER: H. A. SHEN

晶揚科技股份有限公司  
 Taiwan Micropay Corporation

晶揚科技標準包裝規範  
 FOR P-DIP 300MM'S

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