

6367254 MOTOROLA SC (XSTRS/R F)

96D 82498 D

**MPQ2906, 2907** For Specifications, See MHQ2906 Data.

**MAXIMUM RATINGS**

Rating	Symbol	Value	Unit	
Collector-Emitter Voltage	V <sub>CEO</sub>	12	Vdc	
Collector-Base Voltage	V <sub>CBO</sub>	25	Vdc	
Emitter-Base Voltage	V <sub>EBO</sub>	4.0	Vdc	
Collector Current — Continuous	I <sub>C</sub>	1.0	Adc	
Total Device Dissipation @ T <sub>A</sub> = 25°C Derate above 25°C	P <sub>D</sub>	Each Transistor	650	mW
		Four Transistors Equal Power	1250	mW
Total Device Dissipation @ T <sub>C</sub> = 25°C Derate above 25°C	P <sub>D</sub> '	Each Transistor	1.0	Watts
		Four Transistors Equal Power	3.0	Watts
Operating and Storage Junction Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C	

**THERMAL CHARACTERISTICS**

Characteristic	Each Die	Junction to Case	Junction to Ambient	Unit
Thermal Resistance	Each Die	125	193*	°C/W
	Effective, 4 Die	41.6	100*	°C/W
Coupling Factors	Q1-Q4 or Q2-Q3	30	60	%
	Q1-Q2 or Q3-Q4	2.0	25	%

(1) R<sub>θJA</sub> is measured with the device soldered into a typical printed circuit board.

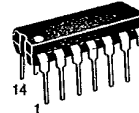
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted.)**

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector-Emitter Breakdown Voltage (I <sub>C</sub> = 10 mAdc, I <sub>B</sub> = 0)	V <sub>(BR)CEO</sub>	12	—	—	Vdc
Collector-Base Breakdown Voltage (I <sub>C</sub> = 100 μAdc, I <sub>E</sub> = 0)	V <sub>(BR)CBO</sub>	25	—	—	Vdc
Emitter-Base Breakdown Voltage (I <sub>E</sub> = 100 μAdc, I <sub>C</sub> = 0)	V <sub>(BR)EBO</sub>	4.0	—	—	Vdc
Collector Cutoff Current (V <sub>CE</sub> = 15 Vdc, V <sub>BE</sub> = 0)	I <sub>CES</sub>	—	—	100	μAdc
<b>ON CHARACTERISTICS</b>					
DC Current Gain (I <sub>C</sub> = 100 mAdc, V <sub>CE</sub> = 0.5 Vdc) (I <sub>C</sub> = 300 mAdc, V <sub>CE</sub> = 0.5 Vdc)	h <sub>FE</sub>	30 40	45 55	— 200	—
Collector-Emitter Saturation Voltage (I <sub>C</sub> = 300 mAdc, I <sub>B</sub> = 30 mAdc) (I <sub>C</sub> = 1.0 Adc, I <sub>B</sub> = 0.1 Adc)	V <sub>CE(sat)</sub>	—	0.22 0.52	0.33 0.7	Vdc
Base-Emitter Saturation Voltage (I <sub>C</sub> = 300 mAdc, I <sub>B</sub> = 30 mAdc) (I <sub>C</sub> = 1.0 Adc, I <sub>B</sub> = 0.1 Adc)	V <sub>BE(sat)</sub>	—	0.87 1.04	1.1 1.4	Vdc
<b>SMALL-SIGNAL CHARACTERISTICS</b>					
Current-Gain — Bandwidth Product (I <sub>C</sub> = 100 mAdc, V <sub>CE</sub> = 5.0 Vdc, f = 100 MHz)	f <sub>T</sub>	400	500	—	MHz
Output Capacitance (V <sub>CB</sub> = 5.0 Vdc, I <sub>E</sub> = 0, f = 1 MHz)	C <sub>obo</sub>	—	5.0	10	pF
Input Capacitance (V <sub>BE</sub> = 0.5 Vdc, I <sub>C</sub> = 0, f = 1 MHz)	C <sub>ibo</sub>	—	22	30	pF
<b>SWITCHING CHARACTERISTICS</b>					
Turn-On Time (V <sub>CC</sub> = 12 Vdc, I <sub>C</sub> = 1.0 Adc, V <sub>BE(off)</sub> = 4.0 Vdc, I <sub>B1</sub> = 100 mAdc)	t <sub>on</sub>	—	12	15	ns
Turn-Off Time (V <sub>CC</sub> = 12 Vdc, I <sub>C</sub> = 1.0 Adc, I <sub>B1</sub> = I <sub>B2</sub> = 100 mAdc)	t <sub>off</sub>	—	18	25	ns

T-43-a5

**MPQ3303**

CASE 646-06, STYLE 1  
TO-116



**QUAD  
SWITCHING TRANSISTOR**

NPN SILICON

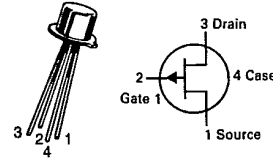
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6367254 MOTOROLA SC (XSTRS/R F)

96D 82543 D

T-35-25  
**2N3993,A**  
**2N3994**

CASE 20-03, STYLE 5  
 TO-72 (TO-206AF)



**JFET**  
**SWITCHING**  
 P-CHANNEL — DEPLETION

**MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	-25	Vdc
Drain-Gate Voltage	$V_{DG}$	-25	Vdc
Reverse Gate-Source Voltage	$V_{GSR}$	25	Vdc
Forward Gate Current	$I_{GF}$	10	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	300 2.0	mW mW/°C
Storage Temperature Range	$T_{stg}$	-65 to +200	°C

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Gate-Source Breakdown Voltage ( $I_G = 1.0 \mu\text{Adc}$ , $V_{DS} = 0$ )	$V_{(BR)GSS}$	25	—	Vdc
Drain Reverse Current ( $V_{DG} = -15 \text{ Vdc}$ , $I_S = 0$ ) ( $V_{DG} = -15 \text{ Vdc}$ , $I_S = 0$ , $T_A = 150^\circ\text{C}$ )	$I_{DGO}$	—	1.2 1.2	nAdc $\mu\text{Adc}$
Drain Cutoff Current ( $V_{DS} = -10 \text{ Vdc}$ , $V_{GS} = 10 \text{ Vdc}$ ) ( $V_{DS} = -10 \text{ Vdc}$ , $V_{GS} = 6.0 \text{ Vdc}$ ) ( $V_{DS} = -10 \text{ Vdc}$ , $V_{GS} = 10 \text{ Vdc}$ , $T_A = 150^\circ$ ) ( $V_{DS} = -10 \text{ Vdc}$ , $V_{GS} = 6.0 \text{ Vdc}$ , $T_A = 150^\circ$ )	$I_{D(off)}$	—	1.2 1.2 1.0 1.0	nAdc $\mu\text{Adc}$
Gate Source Voltage ( $V_{DS} = -10 \text{ Vdc}$ , $I_D = -1.0 \mu\text{Adc}$ )	$V_{GS}$	4.0 1.0	9.5 5.5	Vdc
<b>ON CHARACTERISTICS</b>				
Zero-Gate-Voltage Drain Current(1) ( $V_{DS} = -10 \text{ Vdc}$ , $V_{GS} = 0$ )	$I_{DSS}$	10 2.0	— —	mAdc
<b>SMALL-SIGNAL CHARACTERISTICS</b>				
Drain-Source "ON" Resistance ( $V_{GS} = 0$ , $I_D = 0$ , $f = 1.0 \text{ kHz}$ )	$r_{ds(on)}$	— —	150 300	Ohms
Forward Transfer Admittance(1) ( $V_{DS} = -10 \text{ Vdc}$ , $V_{GS} = 0$ , $f = 1.0 \text{ kHz}$ )	$ y_{fs} $	6.0 7.0 4.0	12 12 10	mmhos
Input Capacitance ( $V_{DS} = -10 \text{ Vdc}$ , $V_{GS} = 0$ , $f = 1.0 \text{ MHz}$ )	$C_{iss}$	— —	16 12	pF
Reverse Transfer Capacitance ( $V_{DS} = 0$ , $V_{GS} = 10 \text{ Vdc}$ , $f = 1.0 \text{ MHz}$ )  ( $V_{DS} = 0$ , $V_{GS} = 6.0 \text{ Vdc}$ , $f = 1.0 \text{ MHz}$ )	$C_{rss}$	— — —	4.5 3.0 5.0	pF

(1) Pulse Test: Pulse Width = 100 ms, Duty Cycle  $\leq 10\%$ .



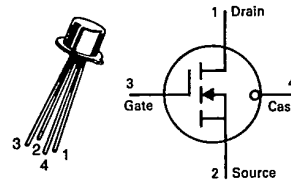
6367254 MOTOROLA SC (XSTRS/R F)

96D 82603 D

T-37-25

**3N157**  
**3N158**

CASE 20-03, STYLE 2  
TO-72 (TO-206AF)



**MOSFET**  
**AMPLIFIER AND SWITCHING**

P-CHANNEL — ENHANCEMENT

**MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Drain-Source Voltage*	V <sub>DS</sub>	±35	Vdc
Drain-Gate Voltage*	V <sub>DG</sub>	±50	Vdc
Gate-Source Voltage*	V <sub>GS</sub>	±50	Vdc
Drain Current*	I <sub>D</sub>	30	mAdc
Total Device Dissipation @ T <sub>A</sub> = 25°C Derate above 25°C*	P <sub>D</sub>	300 1.7	mW mW/°C
Junction Temperature Range*	T <sub>J</sub>	-65 to +175	°C
Storage Channel Temperature Range*	T <sub>stg</sub>	-65 to +175	°C

\*JEDEC Registered Limits

**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted.)**

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Drain-Source Breakdown Voltage (I <sub>D</sub> = -10 μAdc, V <sub>G</sub> = V <sub>S</sub> = 0)	V <sub>(BR)DSX</sub>	-35	—	—	Vdc
Zero-Gate-Voltage Drain Current (V <sub>DS</sub> = -15 Vdc, V <sub>GS</sub> = 0) (V <sub>DS</sub> = -35 Vdc, V <sub>GS</sub> = 0)	I <sub>DSS</sub>	—	—	-1.0 -10	nAdc μAdc
Gate Reverse Current* (V <sub>GS</sub> = +25 Vdc, V <sub>DS</sub> = 0) (V <sub>GS</sub> = +50 Vdc, V <sub>DS</sub> = 0)	I <sub>GSS</sub>	—	—	+10 +10	pAdc nAdc
Input Resistance (V <sub>GS</sub> = -25 Vdc)	R <sub>GS</sub>	—	1 x 10 <sup>12</sup>	—	Ohms
Gate Source Voltage* (V <sub>DS</sub> = -15 Vdc, I <sub>D</sub> = -0.5 mAdc)	V <sub>GS</sub>	-1.5 -3.0	—	-5.5 -7.0	Vdc
Gate Forward Current* (V <sub>GS</sub> = -25 Vdc, V <sub>DS</sub> = 0) (V <sub>GS</sub> = -50 Vdc, V <sub>DS</sub> = 0) (V <sub>GS</sub> = -25 Vdc, V <sub>DS</sub> = 0, T <sub>A</sub> = +55°C) (V <sub>GS</sub> = -50 Vdc, V <sub>DS</sub> = 0, T <sub>A</sub> = +55°C)	I <sub>G(f)</sub>	—	—	-10 -1.0 -1.0 -1.0	pAdc nAdc nAdc μAdc
<b>ON CHARACTERISTICS</b>					
Gate Threshold Voltage* (V <sub>DS</sub> = -15 Vdc, I <sub>D</sub> = -10 μAdc)	V <sub>GS(Th)</sub>	-1.5 -3.0	—	-3.2 -5.0	Vdc
On-State Drain Current* (V <sub>DS</sub> = -15 Vdc, V <sub>GS</sub> = -10 Vdc)	I <sub>D(on)</sub>	-5.0	—	—	mAdc
<b>SMALL-SIGNAL CHARACTERISTICS</b>					
Forward Transfer Admittance* (V <sub>DS</sub> = -15 Vdc, I <sub>D</sub> = -2.0 mAdc, f = 1.0 kHz)	y <sub>fs</sub>	1000	—	4000	μmhos
Output Admittance* (V <sub>DS</sub> = -15 Vdc, I <sub>D</sub> = -2.0 mAdc, f = 1.0 kHz)	y <sub>os</sub>	—	—	60	μmhos
Input Capacitance* (V <sub>DS</sub> = -15 Vdc, V <sub>GS</sub> = 0, f = 140 kHz)	C <sub>iss</sub>	—	—	5.0	pF
Reverse Transfer Capacitance* (V <sub>DS</sub> = -15 Vdc, V <sub>GS</sub> = 0, f = 140 kHz)	C <sub>rss</sub>	—	—	1.3	pF
Drain-Substrate Capacitance (V <sub>D(SUB)</sub> = -10 Vdc, f = 140 kHz)	C <sub>d(sub)</sub>	—	—	4.0	pF
Noise Voltage (R <sub>S</sub> = 0, BW = 1.0 Hz, V <sub>DS</sub> = -15 Vdc, I <sub>D</sub> = -2.0 mAdc, f = 100 Hz) (R <sub>S</sub> = 0, BW = 1.0 Hz, V <sub>DS</sub> = -15 Vdc, I <sub>D</sub> = -2.0 mAdc, f = 1.0 kHz)	e <sub>n</sub>	—	300 120	— 500	NV/√Hz

\*JEDEC Registered Limits

MOTOROLA SMALL-SIGNAL SEMICONDUCTORS

6367254 MOTOROLA SC (XSTRS/R F)

96D 82604 D

3N157, 3N158

T-37-25

FIGURE 1 - FORWARD TRANSCONDUCTANCE

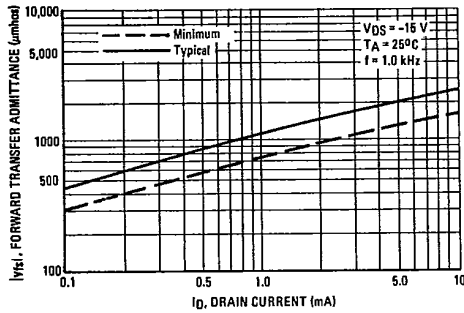


FIGURE 2 - OUTPUT TRANSCONDUCTANCE

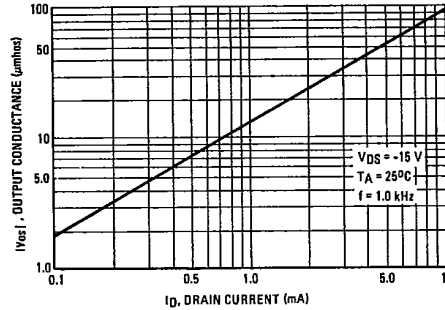


FIGURE 3 - FORWARD TRANSCONDUCTANCE versus TEMPERATURE

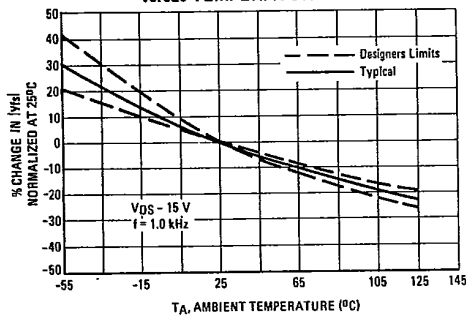


FIGURE 4 - BIAS CURVE

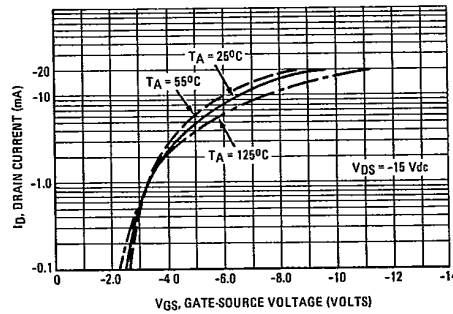


FIGURE 5 - "ON" DRAIN-SOURCE VOLTAGE

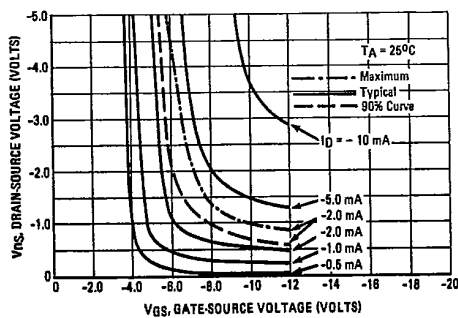
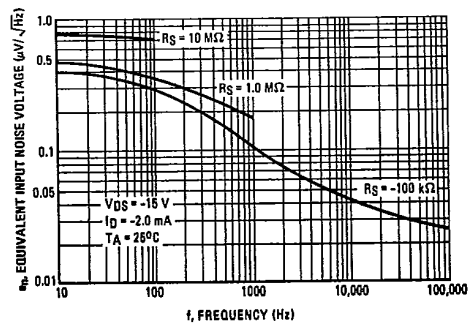


FIGURE 6 - EQUIVALENT INPUT NOISE VOLTAGE



6

6367254 MOTOROLA SC (XSTRS/R F)

96D 82605 D

3N157, 3N158

T-37-25

SWITCHING CHARACTERISTICS  
( $T_A = 25^\circ\text{C}$ )

FIGURE 7 – TURN-ON DELAY TIME

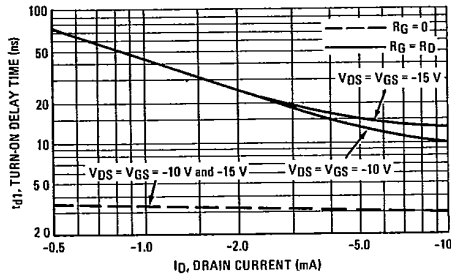


FIGURE 8 – RISE TIME

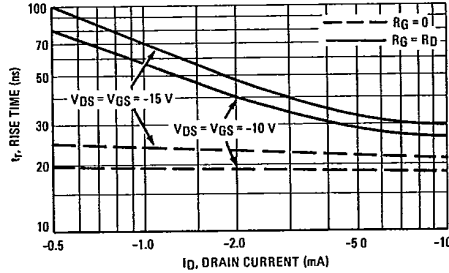


FIGURE 9 – TURN-OFF DELAY TIME

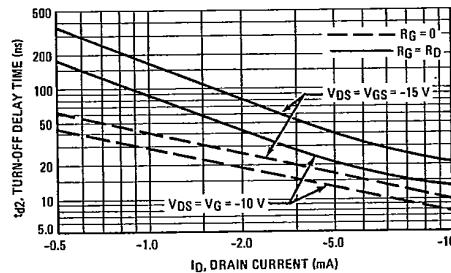


FIGURE 10 – FALL TIME

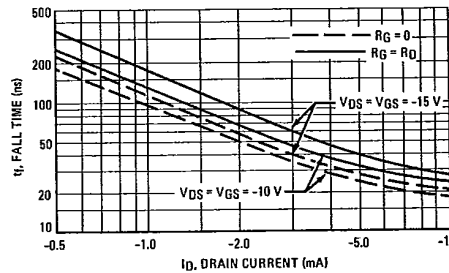


FIGURE 11 – SWITCHING CIRCUIT and WAVEFORMS

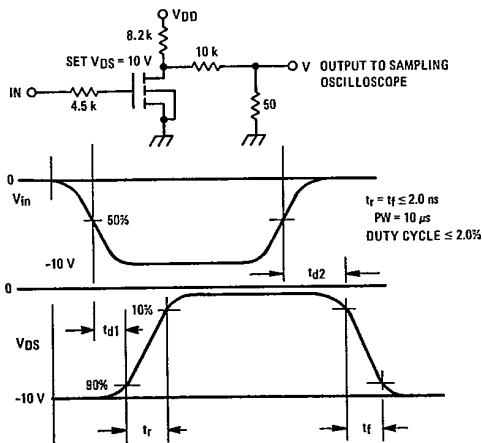
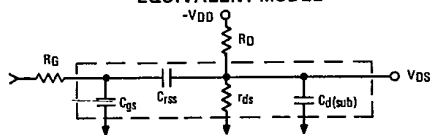


FIGURE 12 – SWITCHING CIRCUIT with MOSFET EQUIVALENT MODEL



The switching characteristics shown above were measured in a test circuit similar to Figure 11. At the beginning of the switching interval, the gate voltage is at ground and the gate source capacitance ( $C_{GS} \cdot C_{RSS} \cdot C_{RGS}$ ) has no charge. The drain voltage is at  $V_{DD}$  and thus the feedback capacitance ( $C_{RGS}$ ) is charged to  $V_{DD}$ . Similarly, the drain substrate capacitance ( $C_{d(sub)}$ ) is charged to  $V_{DD}$  since the substrate and source are connected to ground.

During the turn-on interval  $C_{GS}$  is charged to  $V_{GS}$  (the input voltage) through  $R_G$  (generator impedance) (Figure 12).  $C_{RSS}$  must be discharged to  $V_{GS} \cdot V_{D(on)}$  through  $R_G$  and the parallel combination of the load resistor ( $R_D$ ) and the channel resistance ( $r_{ds}$ ). In addition,  $C_{d(sub)}$  is discharged to a low value ( $V_{D(on)}$ ) through  $R_D$  in parallel with  $r_{ds}$ . During turn-off this charge flow is reversed.

Predicting turn-on time proves to be somewhat difficult since the channel resistance ( $r_{ds}$ ) is a function of the gate voltage ( $V_{GS}$ ). As  $C_{GS}$  becomes charged  $V_{GS}$  is approaching  $V_{in}$  and  $r_{ds}$  decreases (see Figure 5) and since  $C_{RSS}$  and  $C_{d(sub)}$  are charged through  $r_{ds}$ , turn-on time is quite non-linear.

If the charging time of  $C_{GS}$  is short compared to that of  $C_{RSS}$  and  $C_{d(sub)}$ , then  $r_{ds}$  (which is in parallel with  $R_D$ ) will be low compared to  $R_D$  during the switching interval and will largely determine the turn-on time. On the other hand, during turn-off  $r_{ds}$  will be almost an open circuit requiring  $C_{RSS}$  and  $C_{d(sub)}$  to be charged through  $R_D$  and resulting in a turn-off time that is long compared to the turn-on time. This is especially noticeable for the curves where  $R_G = 0$  and  $C_{GS}$  is charged through the pulse generator impedance only.

The switching curves shown with  $R_G = R_D$  simulate the switching behavior of cascaded stages where the driving source impedance is normally the same as the load impedance. The set of curves with  $R_G = 0$  simulates a low source impedance drive such as might occur in complementary logic circuits.