



### 3.3V CMOS QUADRUPLE 2-INPUT POSITIVE-OR GATE

**IDT74ALVC32**

#### FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Vcc = 3.3V ± 0.3V, Normal Range
- Vcc = 2.7V to 3.6V, Extended Range
- Vcc = 2.5V ± 0.2V
- CMOS power levels (0.4µ W typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in SOIC, SSOP, and TSSOP packages

#### DRIVE FEATURES:

- High Output Drivers: ±24mA
- Suitable for Heavy Loads

#### DESCRIPTION:

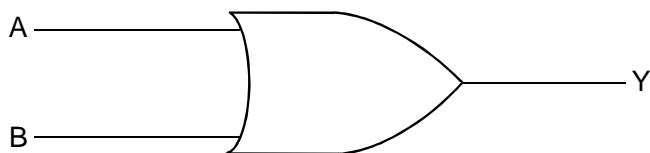
This quadruple 2-input positive-OR gate is built using advanced dual metal CMOS technology. The ALVC32 performs the Boolean function  $Y = \overline{A} \cdot \overline{B}$  or  $Y = A + B$  in positive logic.

The ALVC32 has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

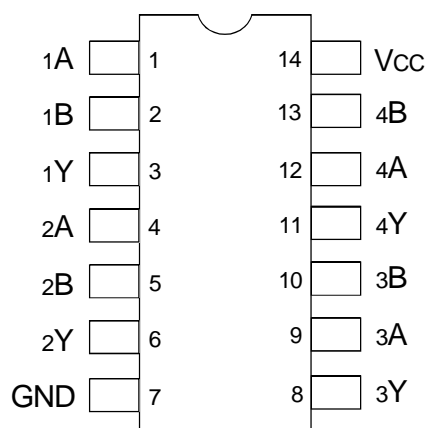
#### APPLICATIONS:

- 3.3V high speed systems
- 3.3V and lower voltage computing systems

#### FUNCTIONAL BLOCK DIAGRAM



#### PIN CONFIGURATION



SOIC/ SSOP/ TSSOP  
TOP VIEW

#### PIN DESCRIPTION

Pin Names	Description
xA, xB	Data Inputs
xY	Data Outputs

#### FUNCTION TABLE (EACH GATE)<sup>(1)</sup>

Inputs		Output
xA	xB	xY
H	X	H
X	H	H
L	L	L

#### NOTE:

1. H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care

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INDUSTRIAL TEMPERATURE RANGE

SEPTEMBER 2000

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V <sub>TERM</sub> <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub> +0.5	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	-50 to +50	mA
I <sub>IK</sub>	Continuous Clamp Current, V <sub>i</sub> < 0 or V <sub>i</sub> > V <sub>CC</sub>	±50	mA
I <sub>OK</sub>	Continuous Clamp Current, V <sub>o</sub> < 0	-50	mA
I <sub>CC</sub> I <sub>SS</sub>	Continuous Current through each V <sub>CC</sub> or GND	±100	mA

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>CC</sub> terminals.
- All terminals except V<sub>CC</sub>.

## CAPACITANCE (T<sub>A</sub> = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	5	7	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	7	9	pF
C <sub>I/O</sub>	I/O Port Capacitance	V <sub>IN</sub> = 0V	7	9	pF

### NOTE:

- As applicable to the device type.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: T<sub>A</sub> = -40°C to +85°C

Symbol	Parameter	Test Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage Level	V <sub>CC</sub> = 2.3V to 2.7V	1.7	—	—	V
		V <sub>CC</sub> = 2.7V to 3.6V	2	—	—	
V <sub>IL</sub>	Input LOW Voltage Level	V <sub>CC</sub> = 2.3V to 2.7V	—	—	0.7	V
		V <sub>CC</sub> = 2.7V to 3.6V	—	—	0.8	
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = 3.6V V <sub>i</sub> = V <sub>CC</sub>	—	—	±5	μA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = 3.6V V <sub>i</sub> = GND	—	—	±5	μA
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = 2.3V, I <sub>IN</sub> = -18mA	—	-0.7	-1.2	V
V <sub>H</sub>	Input Hysteresis	V <sub>CC</sub> = 3.3V	—	100	—	mV
I <sub>CCL</sub> I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = 3.6V V <sub>IN</sub> = GND or V <sub>CC</sub>	—	0.1	10	μA
ΔI <sub>CC</sub>	Quiescent Power Supply Current Variation	One input at V <sub>CC</sub> - 0.6V, other inputs at V <sub>CC</sub> or GND	—	—	750	μA

### NOTE:

- Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Max.	Unit
VOH	Output HIGH Voltage	VCC = 2.3V to 3.6V	IOH = - 0.1mA	VCC - 0.2	—	V
		VCC = 2.3V	IOH = - 6mA	2	—	
		VCC = 2.3V	IOH = - 12mA	1.7	—	
		VCC = 2.7V		2.2	—	
		VCC = 3V		2.4	—	
		VCC = 3V	IOH = - 24mA	2	—	
VOL	Output LOW Voltage	VCC = 2.3V to 3.6V	IOL = 0.1mA	—	0.2	V
		VCC = 2.3V	IOL = 6mA	—	0.4	
			IOL = 12mA	—	0.7	
		VCC = 2.7V	IOL = 12mA	—	0.4	
		VCC = 3V	IOL = 24mA	—	0.55	

**NOTE:**  
1. VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate VCC range. TA = - 40°C to + 85°C.

## OPERATING CHARACTERISTICS, TA = 25°C

Symbol	Parameter	Test Conditions	VCC = 2.5V ± 0.2V	VCC = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance per Gate	CL = 0pF, f = 10Mhz	24	26	pF

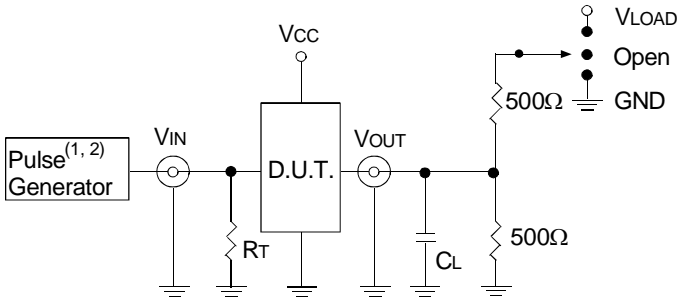
## SWITCHING CHARACTERISTICS<sup>(1)</sup>

Symbol	Parameter	VCC = 2.5V ± 0.2V		VCC = 2.7V		VCC = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tPLH	Propagation Delay xA or xB to xY	1	3.1	1	3.4	1	3.3	ns
tPHL								

**NOTE:**  
1. See TEST CIRCUITS AND WAVEFORMS. TA = - 40°C to + 85°C.

TEST CIRCUITS AND WAVEFORMS  
TEST CONDITIONS

Symbol	V <sub>CC</sub> <sup>(1)</sup> =3.3V±0.3V	V <sub>CC</sub> <sup>(1)</sup> =2.7V	V <sub>CC</sub> <sup>(2)</sup> =2.5V±0.2V	Unit
V <sub>LOAD</sub>	6	6	2 x V <sub>CC</sub>	V
V <sub>IH</sub>	2.7	2.7	V <sub>CC</sub>	V
V <sub>T</sub>	1.5	1.5	V <sub>CC</sub> / 2	V
V <sub>LZ</sub>	300	300	150	mV
V <sub>HZ</sub>	300	300	150	mV
C <sub>L</sub>	50	50	30	pF



Test Circuit for All Outputs

DEFINITIONS:

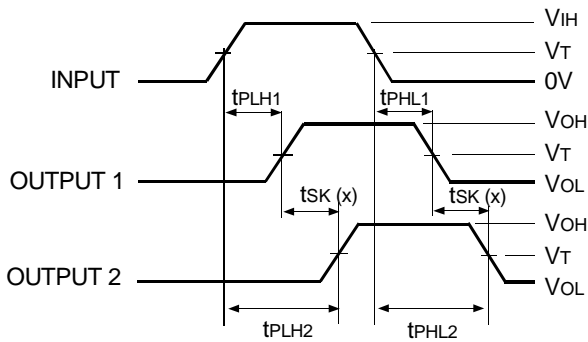
C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.  
R<sub>T</sub> = Termination resistance: should be equal to Z<sub>out</sub> of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>r</sub> ≤ 2.5ns; t<sub>f</sub> ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t<sub>r</sub> ≤ 2ns; t<sub>f</sub> ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V <sub>LOAD</sub>
Disable High Enable High	GND
All Other Tests	Open



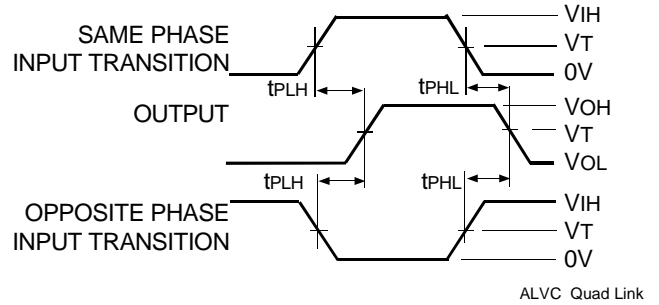
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

ALVC Quad Link

Output Skew - t<sub>SK</sub>(x)

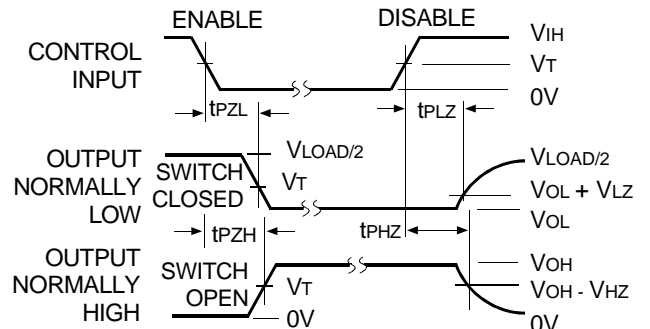
NOTES:

1. For t<sub>SK</sub>(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t<sub>SK</sub>(b) OUTPUT1 and OUTPUT2 are in the same bank.



Propagation Delay

ALVC Quad Link

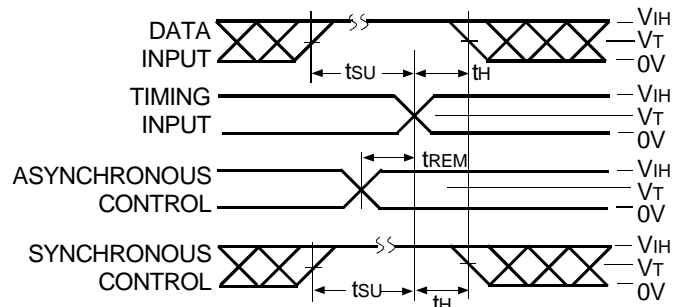


ALVC Quad Link

NOTE:

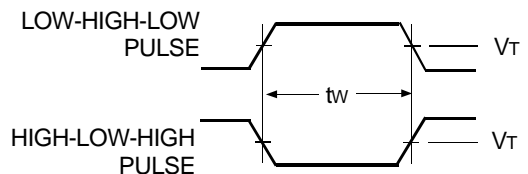
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

Enable and Disable Times



ALVC Quad Link

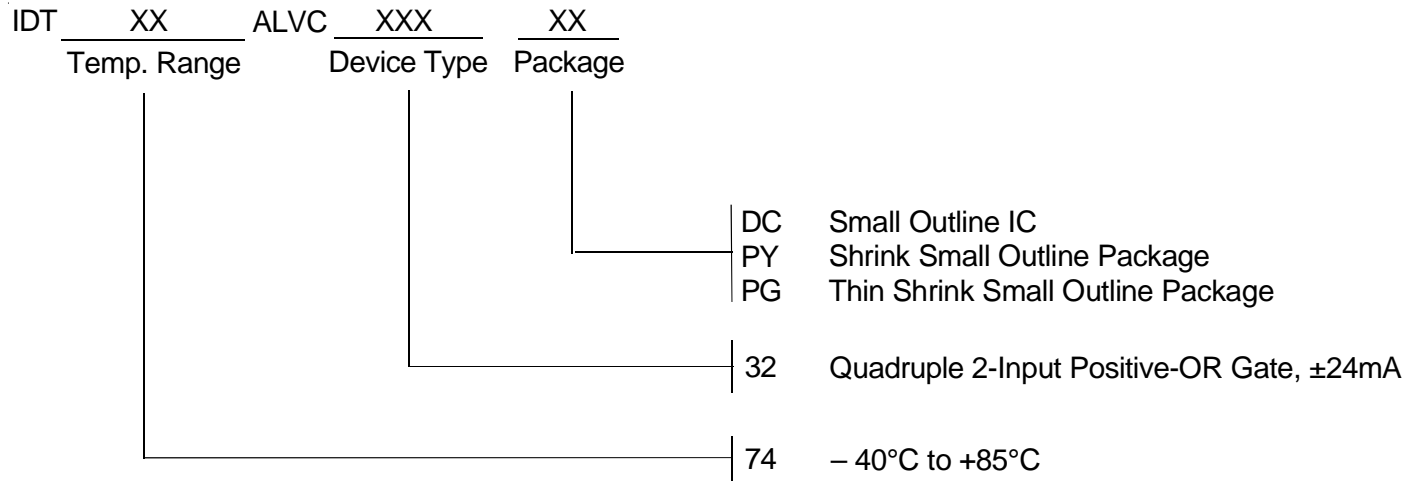
Set-up, Hold, and Release Times



ALVC Quad Link

Pulse Width

## ORDERING INFORMATION



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