a

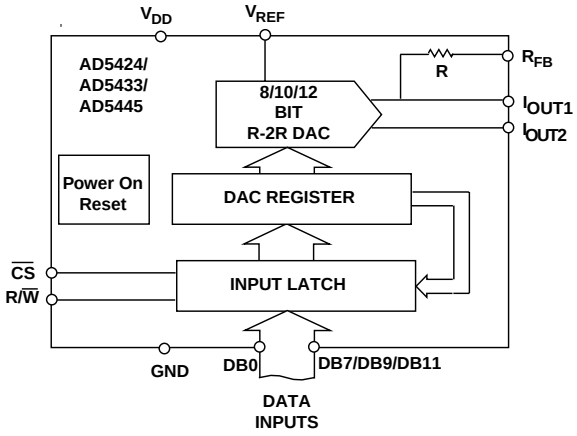
High Bandwidth CMOS 8-/10-/12-Bit Parallel Interface Multiplying DACs

Preliminary Technical Data — AD5424/AD5433/AD5445*

FEATURES
+2.5 V to +5.5 V Supply Operation
Fast Parallel Interface (10ns *WR* cycle)
10MHz Multiplying Bandwidth
±10V Reference Input
20-Lead TSSOP and Chip Scale (4 x4mm) Packages
8, 10 and 12 Bit Current Output DACs
Pin compatible 8, 10 & 12 Bit DACs in Chip Scale
Guaranteed Monotonic
Four Quadrant Multiplication
Power On Reset
Readback Function
5μA typical Power Consumption

APPLICATIONS
Portable Battery Powered Applications
Waveform Generators
Analog Processing
Instrumentation Applications
Programmable Amplifiers and Attenuators
Digitally-Controlled Calibration
Programmable Filters and Oscillators
Composite Video
Ultrasound
Gain, offset and Voltage Trimming

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD5424/AD5433/AD5445 are CMOS 8, 10 and 12-bit current output digital-to-analog converters (DACs) respectively.

These devices operate from a +2.5 V to 5.5 V power supply, making them suited to battery powered applications and many other applications.

These DACs utilize Data readback allowing the user to read the contents of the DAC register via the DB pins. On power-up, the internal register and latches are filled with zeros and the DAC outputs are at zero scale.

As a result of manufacture on a CMOS sub micron process, they offer excellent four quadrant multiplication characteristics, with large signal multiplying bandwidths of up to 10MHz.

The applied external reference input voltage (V_{REF}) determines the full scale output current. An integrated feedback resistor (R_{FB}) provides temperature tracking and full scale voltage output when combined with an external I-toV precision amplifier.

The AD5424 is available in small 20 lead CSP and 16 lead TSSOP packages, while the AD5433/AD5445 DACs are available in small 20-lead CSP and TSSOP packages.

PRODUCT HIGHLIGHTS

1. 10MHz Multiplying Bandwidth
2. 4mm x 4mm Chip Scale Packages and small TSSOP packages.
3. Low Voltage, Low Power Current Output DACs.

*US Patent Number 5,689,257

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703 **Analog Devices, Inc., 2002**

AD5424/AD5433/AD5445–SPECIFICATIONS[1]

(V_{DD} = 2.5 V to 5.5 V, V_{REF} = +10 V, $I_{OUT}2$ = 0 V. All specifications T_{MIN} to T_{MAX} unless otherwise noted. DC performance measured with OP1177, AC performance with AD811 unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Conditions
STATIC PERFORMANCE					
AD5424					
Resolution			8	Bits	
Relative Accuracy			±0.5	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed Monotonic
AD5433					
Resolution			10	Bits	
Relative Accuracy			±1	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed Monotonic
AD5445					
Resolution			12	Bits	
Relative Accuracy			±2	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed Monotonic
Gain Error			±2	mV	
Gain Error Temp Coefficient[2]		±5		ppm FSR/°C	
Output Leakage Current			±10	nA	Data = 0000_H, T_A = 25°C, I_{OUT1}
			±50	nA	Data = 0000_H, I_{OUT1}
Output Voltage Compliance Range		TBD		V	
REFERENCE INPUT[2]					
Reference Input Range		±10		V	
V_{REF} Input Resistance	8	10	12	kΩ	Input resistance TC = -50ppm/°C
DIGITAL INPUTS/OUTPUT[2]					
Input High Voltage, V_{IH}	1.7			V	V_{DD} = 2.5 V to 5.5 V
Input Low Voltage, V_{IL}			0.8	V	V_{DD} = 2.7 V to 5.5 V
			0.7	V	V_{DD} = 2.5 V to 2.7 V
Input Leakage Current, I_{IL}			1	µA	
Input Capacitance			10	pF	
V_{DD} = 4.5 V to 5.5 V					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 200 µA
Output High Voltage, V_{OH}	V_{DD} - 1			V	I_{SOURCE} = 200 µA
V_{DD} = 2.5 V to 3.6 V					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 200 µA
Output High Voltage, V_{OH}	V_{DD} - 0.5			V	I_{SOURCE} = 200 µA
DYNAMIC PERFORMANCE[2]					
Reference Multiplying BW	10			MHz	V_{REF} = 100 mV rms, DAC loaded all 1s
	TBD			MHz	V_{REF} = 6 V rms, DAC loaded all 1s
Output Voltage Settling Time					
AD5424		20	TBD	ns	Measured to ½ LSB. R_{LOAD} = 100Ω, C_{LOAD} =
AD5433		25	TBD	ns	15pF. DAC latch alternately loaded with
AD5445		30	TBD	ns	0s and 1s.
Slew Rate		100		V/µs	
Digital to Analog Glitch Impulse		3		nV-s	1 LSB change around Major Carry
Multiplying Feedthrough Error			-75	dB	DAC latch loaded with all 0s. Reference = 10kHz.
Output Capacitance			2	pF	DAC Latches Loaded with all 0s
			4	pF	DAC Latches Loaded with all 1s
Digital Feedthrough		5		nV-s	Feedthrough to DAC output with *CS* high and Alternate Loading of all 0s and all 1s.
Total Harmonic Distortion		-85		dB	V_{REF} = 6 V rms, All 1s loaded, f = 1kHz
		-85		dB	V_{REF} = 5 V, Sinewave generated from digital code.
Output Noise Spectral Density		25		nV/√Hz	@ 1kHz
SFDR performance		72		dB	
Intermodulation Distortion		TBD		dB	
POWER REQUIREMENTS					
Power Supply Range	2.5		5.5	V	
I_{DD}			10	µA	Logic Inputs = 0 V or V_{DD}
Power Supply Sensitivity[2]			0.001	%/%	ΔV_{DD} = ±5%

NOTES

[1]Temperature range is as follows: B Version: –40°C to +105°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

Single Supply Operation (Biased Mode)

(V_{DD} = 2.5 V to 5.5 V, V_{REF} = +2 V, $I_{OUT}2$ = 1 V. All specifications T_{MIN} to T_{MAX} unless otherwise noted. DC performance measured with OP1177, AC performance with AD811 unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Conditions
STATIC PERFORMANCE					
AD5424					
Resolution			8	Bits	
Relative Accuracy			±0.5	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed Monotonic
AD5433					
Resolution			10	Bits	
Relative Accuracy			±1	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed Monotonic
AD5445					
Resolution			12	Bits	
Relative Accuracy			±2	LSB	
Differential Nonlinearity			±1	LSB	Guaranteed Monotonic
Gain Error			±2	mV	
Gain Error Temp Coefficient[2]		±5		ppm FSR/°C	
Output Leakage Current			±10	nA	Data = 0000_H, T_A = 25°C, I_{OUT1}
			±50	nA	Data = 0000_H, I_{OUT1}
Output Voltage Compliance Range		TBD		V	
REFERENCE INPUT[2]					
Reference Input Range		tbd		V	
V_{REF} Input Resistance	8	10	12	kΩ	Input resistance TC = -50ppm/°C
DIGITAL INPUTS/OUTPUT[2]					
Input High Voltage, V_{IH}	1.7			V	V_{DD} = 2.5 V to 5.5 V
Input Low Voltage, V_{IL}			0.8	V	V_{DD} = 2.7 V to 5.5 V
			0.7	V	V_{DD} = 2.5 V to 2.7 V
Input Leakage Current, I_{IL}			1	µA	
Input Capacitance			10	pF	
V_{DD} = 4.5 V to 5.5 V					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 200 µA
Output High Voltage, V_{OH}	V_{DD} - 1			V	I_{SOURCE} = 200 µA
V_{DD} = 2.5 V to 3.6 V					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 200 µA
Output High Voltage, V_{OH}	V_{DD} - 0.5			V	I_{SOURCE} = 200 µA
DYNAMIC PERFORMANCE[2]					
Reference Multiplying BW	10			MHz	V_{REF} = 100 mV rms, DAC loaded all 1s
	TBD			MHz	V_{REF} = 1 V rms, DAC loaded all 1s
Output Voltage Settling Time					
AD5424		15	TBD	ns	Measured to ½ LSB. R_{LOAD} = 100Ω, C_{LOAD} =
AD5433		22	TBD	ns	15pF. DAC latch alternately loaded with
AD5445		30	TBD	ns	0s and 1s.
Slew Rate		100		V/µs	
Digital to Analog Glitch Impulse		3		nV-s	1 LSB change around Major Carry
Multiplying Feedthrough Error			-75	dB	DAC latch loaded with all 0s. Reference = 10kHz.
Output Capacitance			2	pF	DAC Latches Loaded with all 0s
			4	pF	DAC Latches Loaded with all 1s
Digital Feedthrough		5		nV-s	Feedthrough to DAC output with *CS* high and Alternate Loading of all 0s and all 1s.
Total Harmonic Distortion		-85		dB	V_{REF} = 2 Vp-p, 1V Bias, All 1s loaded, f = 1kHz
		-85		dB	V_{REF} = 2 V, Sinewave generated from digital code.
Output Noise Spectral Density		25		nV/√Hz	@ 1kHz
SFDR performance		72		dB	
Intermodulation Distortion		TBD		dB	
POWER REQUIREMENTS					
Power Supply Range	2.5		5.5	V	
I_{DD}			10	µA	Logic Inputs = 0 V or V_{DD}
Power Supply Sensitivity[2]			0.001	%/%	ΔV_{DD} = ±5%

NOTES

[1]Temperature range is as follows: B Version: –40°C to +105°C.

[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

AD5424/AD5433/AD5445–SPECIFICATIONS[1]

TIMING CHARACTERISTICS[1,2]

(V_{DD} = 2.5 V to 5.5 V, V_{REF} = +5 V, $I_{OUT}2$ = 0 V. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX}	Units	Conditions/Comments
t_1	0	ns min	R/*W* to *CS* Setup Time
t_2	0	ns min	R/*W* to *CS* Hold Time
t_3	10	ns min	*CS* Low Time (Write Cycle)
t_4	6	ns min	Data Setup Time
t_5	0	ns min	Data Hold Time
t_6	5	ns min	R/*W* high to *CS* low
t_7	7	ns min	*CS* Min High Time
t_8	5	ns typ	Data Acess Time
	25	ns max	
t_9	5	ns typ	Bus Relinquish Time
	10	ns max	

NOTES

[1]See Figure 1. Temperature range is as follows: B Version: –40°C to +105°C. Guaranteed by design and characterisation, not subject to production test.

[2]All input signals are specified with tr =tf = 5ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2. Digital Output timing measured with Load circuit in Figure 2.

Specifications subject to change without notice.

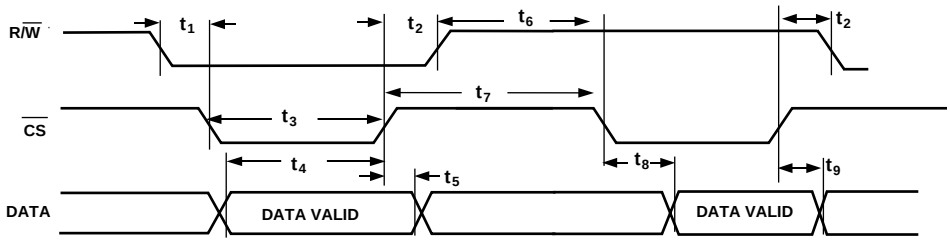


Figure 1. Timing Diagram.

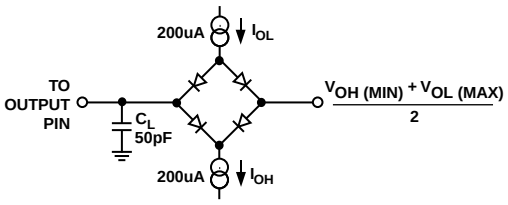


Figure 2. Load Circuit for Data Output Timing Specifications

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to GND	–0.3 V to +7 V
V_{REF}, R_{FB} to GND	–12 V to +12 V
$I_{OUT}1$, $I_{OUT}2$ to GND	–0.3 V to +7 V
Logic Inputs & Output[2]	-0.3V to V_{DD} +0.3 V
Operating Temperature Range	
Industrial (B Version)	–40°C to +105°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	+150°C
16 lead TSSOP θ_{JA} Thermal Impedance	150°C/W
20 lead TSSOP θ_{JA} Thermal Impedance	143°C/W
20 lead CSP θ_{JA} Thermal Impedance	135°C/W
Lead Temperature, Soldering (10seconds)	300°C
IR Reflow, Peak Temperature (< 20 seconds)	+235°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2]Overvoltages at DBx, *CS* and *W*/R, will be clamped by internal diodes. Current should be limited to the maximum ratings given.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD5424BRU	-40 °C to +105 °C	TSSOP (Thin Shrink Small Outline Package)	RU-16
AD5424BCP	-40 °C to +105 °C	CSP (Chip Scale Package)	CP-20
AD5433BRU	-40 °C to +105 °C	TSSOP (Thin Shrink Small Outline Package)	RU-20
AD5433BCP	-40 °C to +105 °C	CSP (Chip Scale Package)	CP-20
AD5445BRU	-40 °C to +105 °C	TSSOP (Thin Shrink Small Outline Package)	RU-20
AD5445BCP	-40 °C to +105 °C	CSP (Chip Scale Package)	CP-20

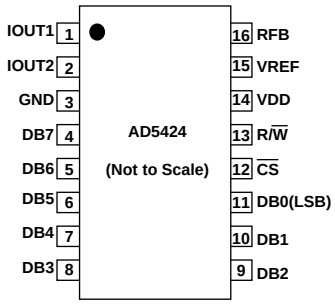
CAUTION

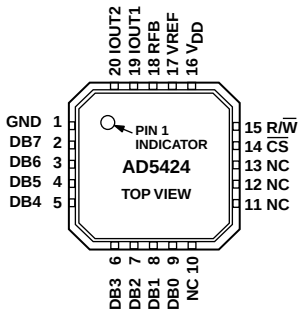
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5424/AD5433/AD5445 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD5424 PIN FUNCTION DESCRIPTION

Pin TSSOP	Pin CSP	Mnemonic	Function
1	19	$I_{OUT}1$	DAC Current Output.
2	20	$I_{OUT}2$	DAC Analog Ground. This pin should normally be tied to the analog ground of the system.
3	1	GND	Ground Pin.
4-11	2-9	DB7-DB0	Parallel Data Bits 7 through 0.
	10-13	NC	No internal connection
12	14	*CS*	Chip Select Input. Active Low. Used in conjunction with R/*W* to load parallel data to the input latch or to read data from the DAC register.
13	15	R/*W*	Read/Write. When low, used in conjunction with CS to load parallel data. When high, used in conjunction with *CS* to readback contents of DAC Register.
14	16	V_{DD}	Positive power supply input. These parts can be operated from a supply of +2.5 V to +5.5 V.
15	17	V_{REF}	DAC reference voltage input terminal.
16	18	R_{FB}	DAC feedback resistor pin. Establish voltage output for the DAC by connecting to external amplifier output.

PIN CONFIGURATIONS
TSSOP & CSP

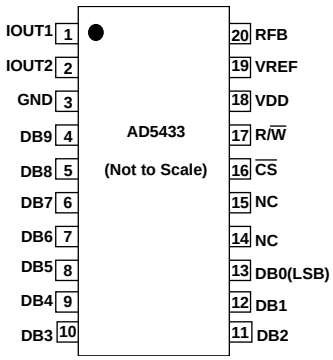


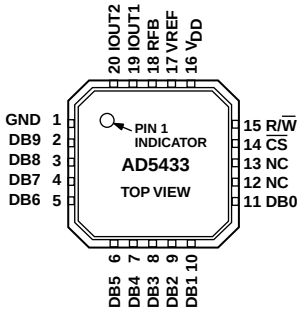


AD5433 PIN FUNCTION DESCRIPTION

Pin TSSOP	Pin CSP	Mnemonic	Function
1	19	$I_{OUT}1$	DAC Current Output.
2	20	$I_{OUT}2$	DAC Analog Ground. This pin should normally be tied to the analog ground of the system.
3	1	GND	Ground Pin.
4-13	2-11	DB9-DB0	Parallel Data Bits 7 through 0.
14, 15	12, 13	NC	Not internally connected.
16	14	*CS*	Chip Select Input. Active Low. Used in conjunction with R/*W* to load parallel data to the input latch or to read data from the DAC register.
17	15	R/*W*	Read/Write. When low, used in conjunction with CS to load parallel data. When high, used in conjunction with *CS* to readback contents of DAC Register.
18	16	V_{DD}	Positive power supply input. These parts can be operated from a supply of +2.5 V to +5.5 V.
19	17	V_{REF}	DAC reference voltage input terminal.
20	18	R_{FB}	DAC feedback resistor pin. Establish voltage output for the DAC by connecting to external amplifier output.

PIN CONFIGURATIONS
TSSOP & CSP

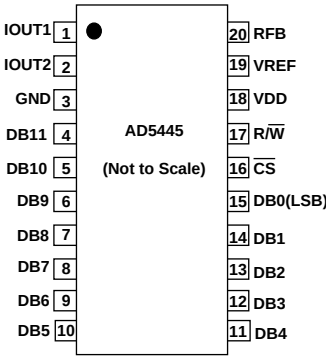


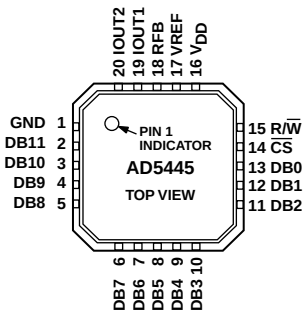


AD5445 PIN FUNCTION DESCRIPTION

Pin TSSOP	Pin CSP	Mnemonic	Function
1	19	$I_{OUT}1$	DAC Current Output.
2	20	$I_{OUT}2$	DAC Analog Ground. This pin should normally be tied to the analog ground of the system.
3	1	GND	Ground Pin.
4-15	2-13	DB11-DB0	Parallel Data Bits 7 through 0.
16	14	*CS*	Chip Select Input. Active Low. Used in conjunction with R/*W* to load parallel data to the input latch or to read data from the DAC register.
17	15	R/*W*	Read/Write. When low, used in conjunction with CS to load parallel data. When high, used in conjunction with *CS* to readback contents of DAC Register.
18	16	V_{DD}	Positive power supply input. These parts can be operated from a supply of +2.5 V to +5.5 V.
19	17	V_{REF}	DAC reference voltage input terminal.
20	18	R_{FB}	DAC feedback resistor pin. Establish voltage output for the DAC by connecting to external amplifier output.

PIN CONFIGURATIONS
TSSOP & CSP





TERMINOLOGY

Relative Accuracy
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is normally expressed in LSBs or as a percentage of full scale reading.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max over the operating temperature range ensures monotonicity.

Gain Error
Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For these DACs, ideal maximum output is V_{REF} – 1 LSB. Gain error of the DACs is adjustable to zero with external resistance.

Output Leakage Current
Output leakage current is current which flows in the DAC ladder switches when these are turned off. For the I_{OUT1} terminal, it can be measured by loading all 0s to the DAC and measuring the I_{OUT1} current. Minimum current will flow in the I_{OUT2} line when the DAC is loaded with all 1s

Output Capacitance
Capacitance from I_{OUT1} or I_{OUT2} to AGND.

Output Current Settling Time
This is the amount of time it takes for the output to settle to a specified level for a full scale input change. For these devices, it is specifed with a 100 Ω resistor to ground.

Digital to Analog Glitch Impulse
The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage signal.

Digital Feedthrough
When the device is not selected, high frequency logic activity on the device digital inputs is capacitivelly coupled through the device to show up as noise on the I_{OUT} pins and subsequently into the following circuitry. This noise is digital feedthrough.

Multiplying Feedthrough Error
This is the error due to capacitive feedthrough from the DAC reference input to the DAC I_{OUT1} terminal, when all o0s are loaded to the DAC.

Harmonic Distortion
The DAC is driven by an ac reference. The ratio of the rms sum of the harmonics of the DAC output to the fundamental value is the THD. Usually only the lower order harmonices are included, such as second to fifth.

$$THD = 20\log \frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2)}}{V_1}$$

Intermodulation Distortion
The DAC is driven by two combinded sine waves references of frequencies fa and fb. Distortion products are produced at sum and difference frequencies of mfa±nfb where m, n = 0, 1, 2, 3... Intermodulation terms are those for which m or n is not equal to zero. The second order terms include (fa +fb) and (fa - fb) and the third order terms are (2fa + fb), (2fa -fb), (f+2fa + 2fb) and (fa - 2fb). IMD is defined as

$$IMD = 20\log \frac{\text{(rms sum of the sum and diff distortion products)}}{\text{rms amplitude of the fundamental}}$$

Compliance Voltage Range
The maximum range of (output) terminal voltage for which the device will provide the specified characteristics.

GENERAL DESCRIPTION

DAC Section
The AD5424, AD5433 and AD5445 are 8, 10 and 12 bit current output DACs consisting of a standard inverting R-2R ladder configuration. A simplified diagram for the 8-Bit AD5424 is shown in Figure 3. The feedback resistor R_{FB} has a value of R. The value of R is typically 10kΩ (minimum 8kΩ and maximum 12kΩ). If I_{OUT1} and I_{OUT2} are kept at the same potential, a constant current flows in each ladder leg, regardless of digital input code. Therefore, the input resistance presented at V_{REF} is always constant.

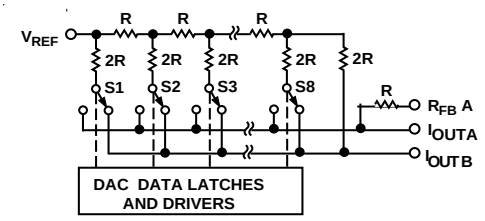


Figure 3. Simplified Ladder

Access is provided to the V_{REF}, R_{FB}, I_{OUT1} and I_{OUT2} terminals of the DAC, making the device extremely versatile and allowing it to be configured in several different operating modes, for example, to provide a unipolar output, bipolar output or in single supply modes of operation. in unipolar mode or four quadrant multiplication in bipolar mode.

Unipolar Mode
Using a single op amp, these devices can easily be configured to provide 2 quadrant multiplying operation or a unipolar output voltage swing as shown in Figure 4.

When an output amplifier is connected in unipolar mode, the output voltage is given by:

$$V_{OUT} = -D \times V_{REF}$$

Where D is the fractional representation of the digital word loaded to the DAC.

D = 0 to 256 (8-Bit AD5424)
= 0 to 1024 (10-Bit AD5433)
= 0 to 4096 (12-Bit AD5445)

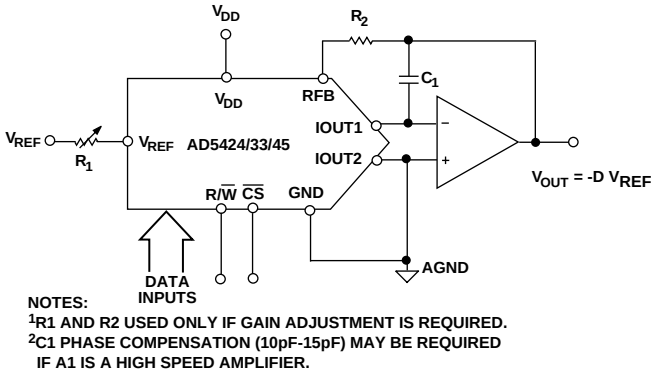


Figure 4. Unipolar Operation

With a fixed 10 V reference, the circuit shown above will give an unipolar 0V to -10V output voltage swing. When V_{IN} is an ac signal, the circuit performs two-quadrant multiplication.

The following table shows the relationship between digital code and expected output voltage for unipolar operation. (AD5424, 8-Bit device).

Table I. Unipolar Code Table

Digital Input	Analog Output (V)
1111 1111	$-V_{REF}$ (255/256)
1000 0000	$-V_{REF}$ (128/256) = $-V_{REF}/2$
0000 0001	$-V_{REF}$ (1/256)
0000 0000	$-V_{REF}$ (0/256) = 0

Bipolar Operation

In some applications, it may be necessary to generate full 4-Quadrant multplying operation or a bipolar output swing. This can be easily accomplished by using another external amplifier and some external resistors as shown in Figure 5.

When V_{IN} is an ac signal, the circuit performs four-quadrant multiplication.

Table II. shows the relationship between digital code and the expected output voltage for bipolar operation (AD5426, 8-Bit device).

Table II. Bipolar Code Table

Digital Input	Analog Output (V)
1111 1111	$+V_{REF}$ (127/128)
1000 0000	0
0000 0001	$-V_{REF}$ (127/128)
0000 0000	$-V_{REF}$ (128/128)

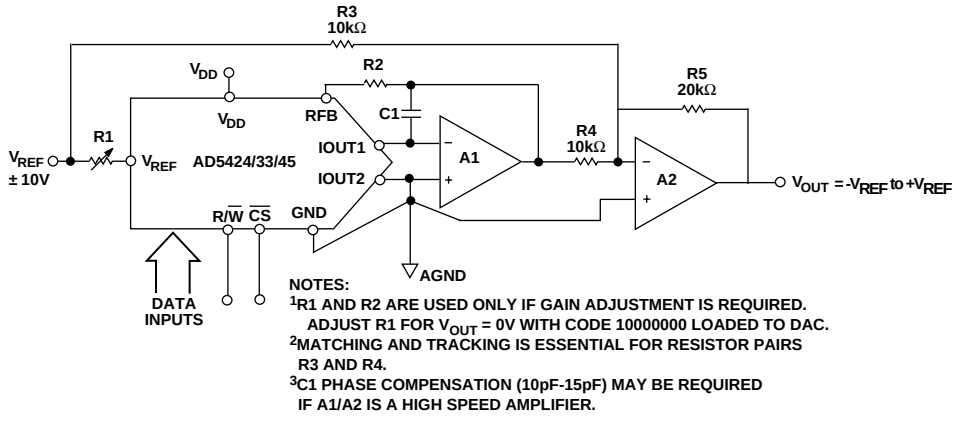


Figure 5. Bipolar Operation (4 Quadrant Multiplication)

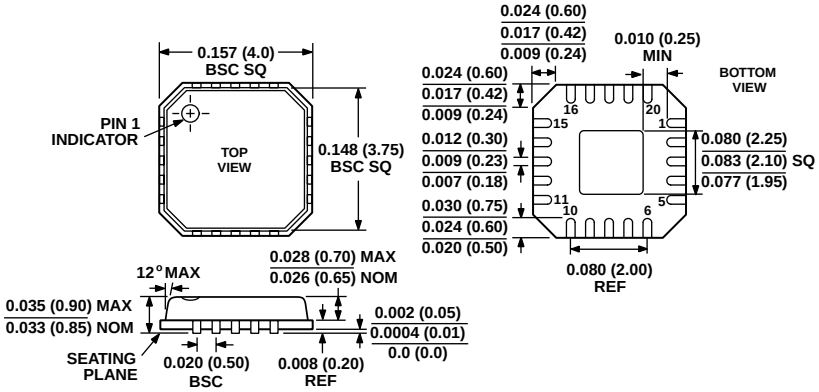
Overview of AD54xx devices

Part No	Resolution	#DACs	INL	Settling Time	Interface	Package	Features
AD5424	8	1	±0.5	20ns	Parallel	RU-16, CP-20	10 MHz, 10 ns *CS* Pulse Width
AD5425	8	1	±0.5	20ns	Serial	RM-10	Byte Load,10 MHz BW, 50 MHz Serial
AD5426	8	1	±0.5	20ns	Serial	RM-10	10 MHz BW, 50 MHz Serial
AD5432	10	1	±1	25ns	Serial	RM-10	10 MHz BW, 50 MHz Serial
AD5433	10	1	±1	25ns	Parallel	RU-20, CP-20	10 MHz, 10 ns *CS* Pulse Width
AD5443	12	1	±2	30ns	Serial	RM-10	10 MHz BW, 50 MHz Serial
AD5445	12	1	±2	30ns	Parallel	RU-20, CP-20	10 MHz, 10 ns CS Pulse Width

OUTLINE DIMENSIONS

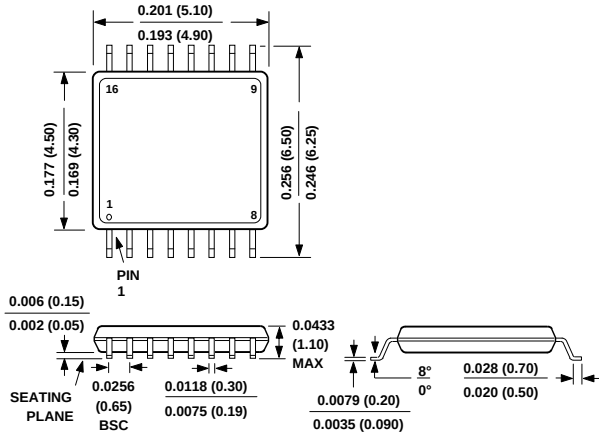
Dimensions shown in inches and (mm).

20 Lead CSP
(CP-20)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS

16 Lead TSSOP
(RU-16)



20 Lead TSSOP
(RU-20)