



Advance Information

UHF Silicon FET Power Amplifier

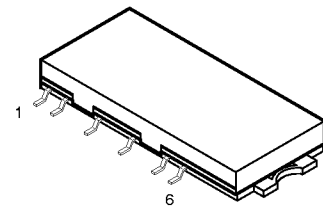
This device is designed specifically for TETRA digital 3.0 W mobile radios, operates from a 12.5 V supply and features 28 dB minimum gain.

- Specified 12.5 V Characteristics:
 - RF Input Power: 9.0 dBm
 - RF Output Power: 5.0 W
 - Power Gain: 28 dB Min
 - Harmonics: -30 dBc Max @ 2 f_o
- Metal Case Low Profile Gives Consistent Performance and Reliability
- 50 Ω Input/Output Impedances
- Guaranteed Stability and Ruggedness

MHW2723

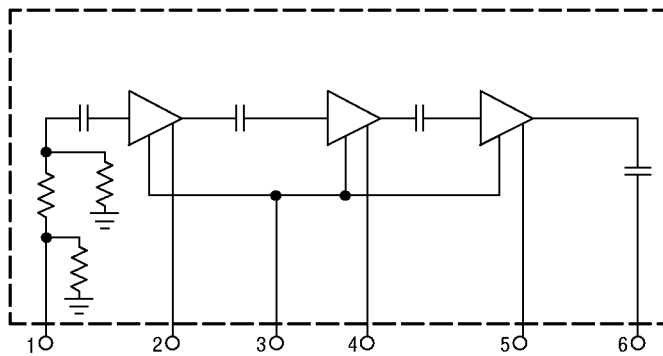
UHF POWER AMPLIFIER 5.0 W, 380 to 470 MHz

SEMICONDUCTOR TECHNICAL DATA



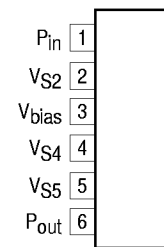
CASE 420Z

Simplified Block Diagram



This device contains 3 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MHW2723	T _C = -30 to 90°C	Power Module

MHW2723

MAXIMUM RATINGS (T_C = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
DC Supply Voltage (Pins 2, 4, 5)	V _{S2, 4, 5}	16	Vdc
DC Bias Voltage (Pin 3)	V _{bias}	5.0	Vdc
RF Input Power	P _{in}	14	dBm
RF Output Power (V _{S2, 4, 5} = 16 V)	P _{out}	12	W
Operating Case Temperature Range	T _C	-30 to 90	°C
Storage Temperature Range	T _{stg}	-30 to 100	°C

NOTES: 1. Meets Human Body Model (HBM) ≤3000 V.
2. ESD data available upon request.

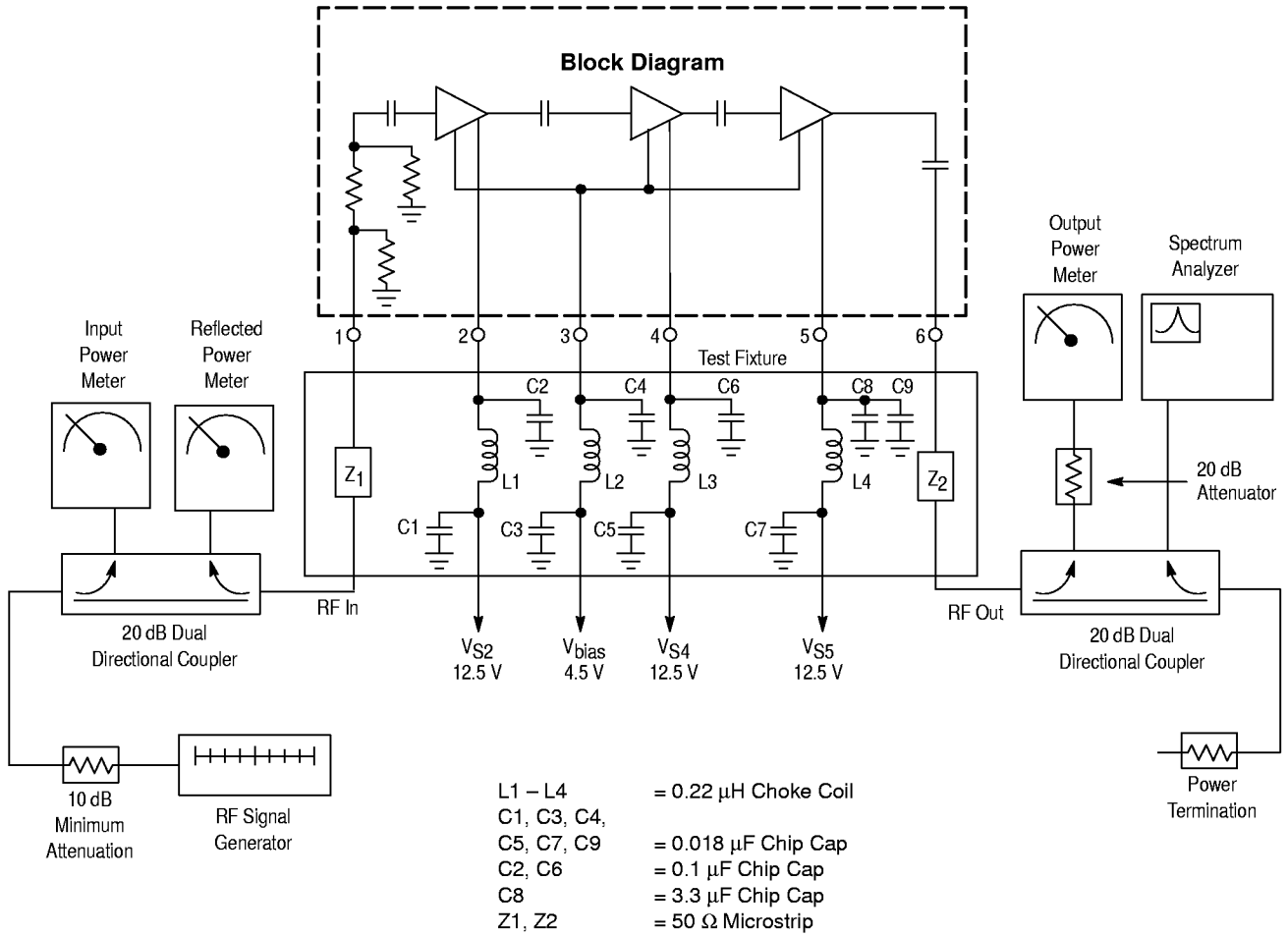
ELECTRICAL CHARACTERISTICS (V_{bias} = 4.5 V; V_{S2, 4, 5} = 12.5 Vdc; T_C = 25°C, 50 Ω system, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	380	–	470	MHz
RF Input Power Range	P _{in}	-8.0	–	14	dBm
Saturated Output Power (P _{in} = 14 dBm) (Note 1)	P _{sat}	12	–	–	W
Power Gain (Adjust P _{in} for P _{out} = 5.0 W)	G _p	28	–	–	dB
Input Return Loss (P _{in} = -8 to 14 dBm; 50 Ω Ref.)	VSWR _{in}	–	–	2:1	–
Efficiency (P _{out} = 5.0 W)	η	18	–	–	%
Adjacent Channel Power (P _{out} = 5.0 W; f = f _o ± 25 KHz, 18 KHz Bandwidth, π/4 DQPSK Modulation 36 KBITS/S, On/Off Factor 0.35) (Note 2)	ACP	-30	–	–	dBc
Alternate Channel Power (P _{out} = 5.0 W; f = f _o ± 50 KHz, 18 KHz Bandwidth, π/4 DQPSK Modulation 36 KBITS/S, On/Off Factor 0.35) (Note 2)	ACP	-40	–	–	dBc
Bias Current (V _{bias} = 4.5 V)	I _{bias}	–	–	10	mA
Rise Time (P _{out} = 0.1 mW to 12 W) (Note 1)	t _r	–	–	20	μsec
Stability (P _{out} = -20 dBm Avg to 38 dBm Avg; V _{bias} = 4.5 V Pulse Pin; V _{S2, 4, 5} = 10.8–16 Vdc; Load VSWR = 2:1, Source VSWR = 2:1, All Phase Angles at Frequency of Test)	–	All Spurious Outputs More Than 60 dB Below Desired Signal			
Harmonics (P _{out} = 5.0 W) 2 f _o	–	–	–	-30	dBc
Isolation (V _{bias} = 0 V; P _{in} = Nominal Drive Level for P _{out} = 12 W; V _{S2, 4, 5} = 12.5 Vdc; Case Temperature = 25°C; Load Impedance and Source Impedance = 50 Ω)	–	–	–	60	dB
Load Mismatch Stress (V _{S2, 4, 5} = 16 Vdc; V _{bias} = 4.5 V; P _{in} = 12 dBm; (25% Duty Cycle Period = 56.7 ms); Load VSWR = 2:1, All Phase Angles at Frequency of Test) (Note 1)	ψ	No Degradation in Output Power Before & After Test			
Noise Power (P _{out} = 5.0 W; f = f _o + 5.0 MHz; Bandwidth = 18 KHz)	P _N	–	–	-85	dBm

NOTES: 1. Pulsed V_{bias} or P_{in}; Duty Cycle = 25%, Period = 56.7 ms; On Time = 14.17 ms.
2. TETRA Signal Format – Continuous Wave.

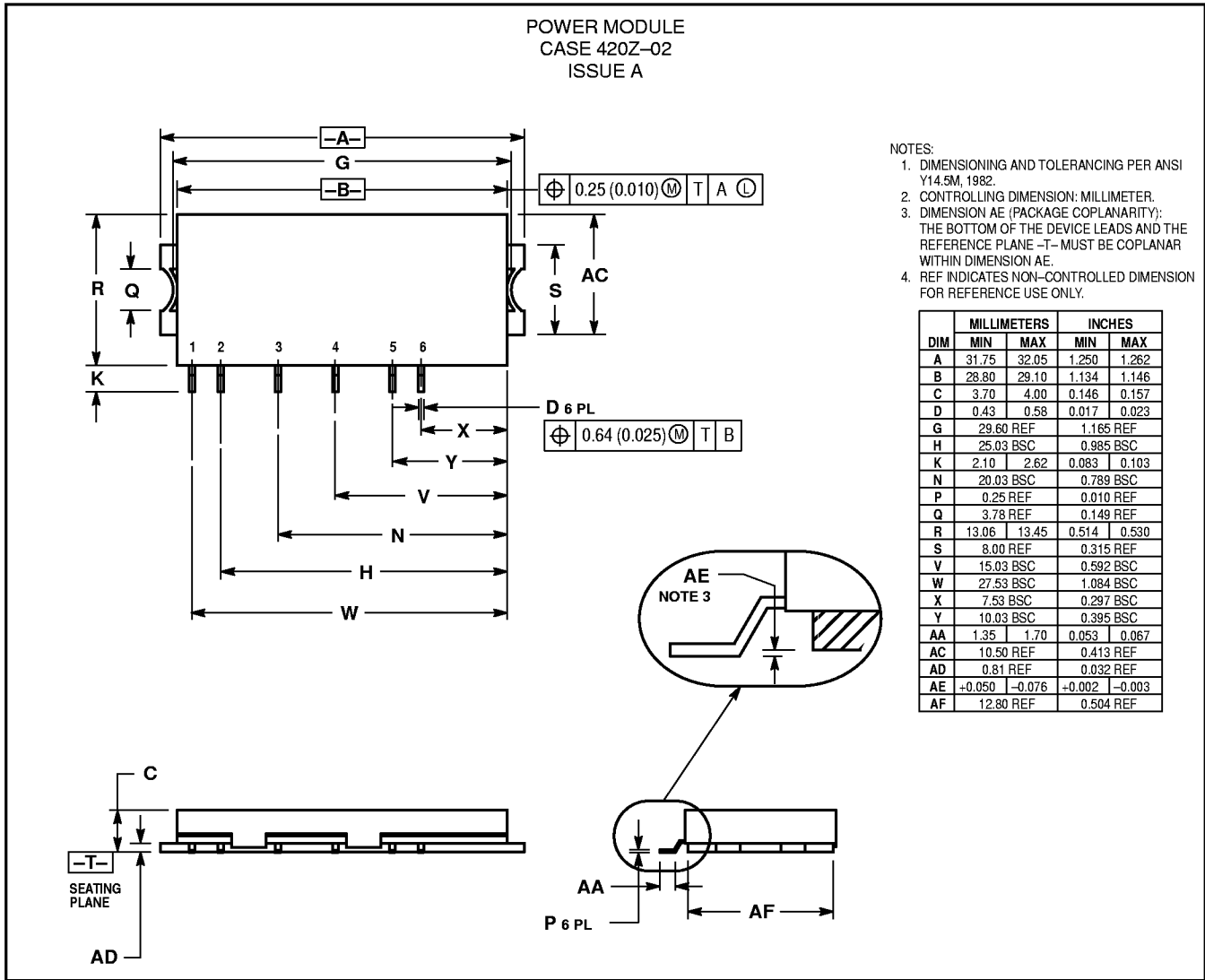
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Figure 1. Test Circuit Diagram



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