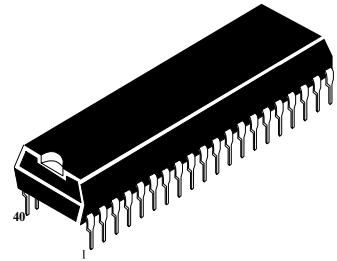


LCD CONTROL IC WITH I<sup>2</sup>C INTERFACE

Description

Functions:

- Direct and duplex LCD control modes. IC controls 32 LCD segments in direct mode and 64 segments in duplex mode;
- Ensures interface of I<sup>2</sup>C bus interface; can be used as expander of I<sup>2</sup>C bus output



T<sub>amb</sub> = -10 to +70 °C

Figure 1 - Package type

Features:

- Supply voltage 2.5 to 6V;
- Low power consumption;
- Embedded oscillator for LCD control signals shaping;
- Autoincremented data input;
- Possibility to switch over display memory banks in direct control mode;
- Possibility for cascading IC to increase number of controlled segment up to 256;
- Blanking of display on supply reset.

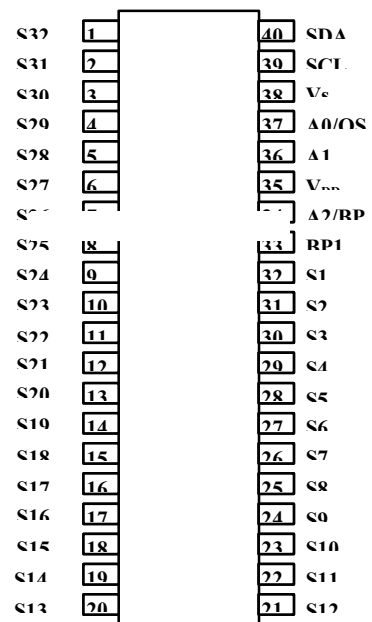


Figure 2 - Pinout

Operation temperature range

Operation temperature range from minus 40 to plus 85 °C.

## INF8577N

**Table 1 - Absolute maximum and maximum conditions**

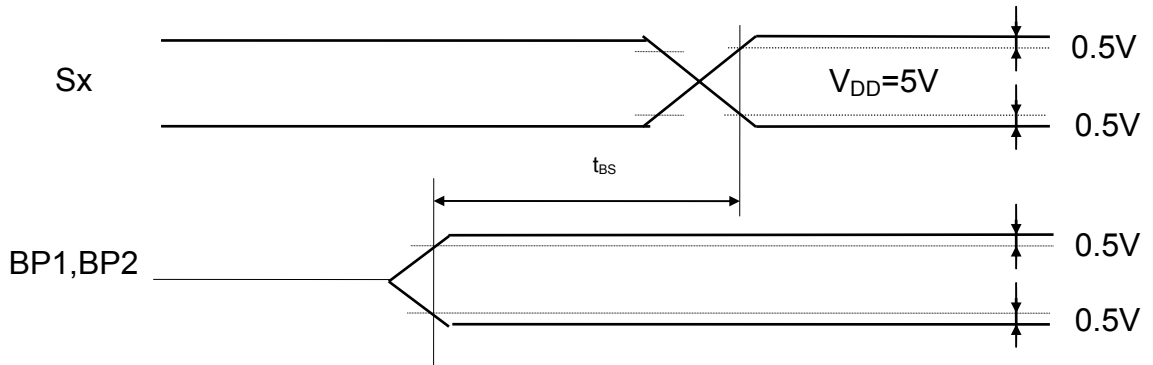
Parameter, unit	Symbol	Maximum ratings		Absolute maximum ratings	
		min	max	min	max
Supply voltage, V	$V_{DD}$	2.5	6.0	-0.5	8.0
Input voltage, V	$V_1$	0	$V_{DD}$	-0.5	$V_{DD}+0.5$
Constant component of LCD driver, mV	$V_{BP}$	-20	20		
Consumption current, mA	$I_{DD}, I_{SS}$	-	0.125	-50	50
Input current, mA	$I_I$	-	-	-20	20
Output current, mA	$I_O$	-	-	-25	25
Reset forming voltage when switching on the supply, V	$V_{POR}$	-	2.0	-	-
Low input voltage on output A0/OSC, V	$V_{IL1}$	0	0.05	-	-
High input voltage on output A0/OSC, V	$V_{IH1}$	$V_{DD}-0.5$	$V_{DD}$	-	-
Low input voltage on output A1, V	$V_{IL2}$	0	$0.3 V_{DD}$	-	-
High input voltage on output A1, V	$V_{IH2}$	$0.7 V_{DD}$	$V_{DD}$	-	-
Low input voltage on output A2/BP2, V	$V_{IL3}$	0	0.10	-	-
High input voltage on output A2/BP2, V	$V_{IH3}$	$V_{DD}-0.10$	$V_{DD}$	-	-
Low input voltage on outputs SCL, SDA, V	$V_{IL4}$	0	$0.3 V_{DD}$	-	-
High input voltage on outputs SCL, SDA, V	$V_{IH4}$	$0.7 V_{DD}$	6.0	-	-
Clock signal frequency, kHz	$f_{SCL}$	-	100	-	-

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**Table 2 - Electrical parameters** (Tamb = from minus 40 to plus 85°C )

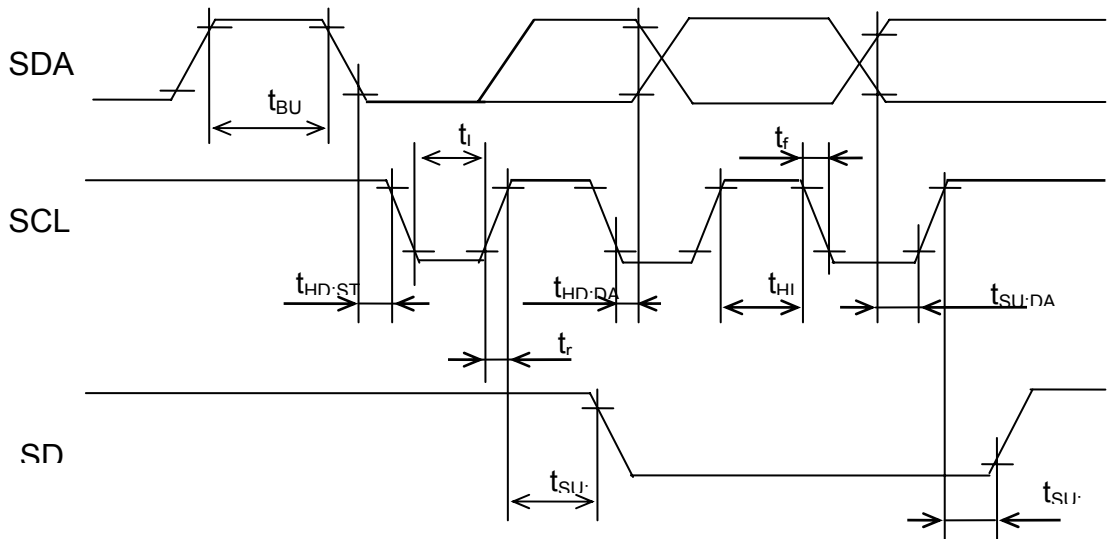
Parameter	Symbol	Test conditions	Value		Unit
			min	max	
current	$I_{DD1}$	6.0 V, $f_{SCL}=100$ kHz, $R_{OSC}=1$ MOhm, $C_{OSC}=680$ pF	-	125	uA
	$I_{DD2}$	$V_{DD}= 2.5$ to 6.0 V, $f_{SCL}=0$ kHz, $R_{OSC}=1$ MOhm, $C_{OSC}=680$ pF	-	75	
	$I_{DD3}$	$V_{DD}=5$ V, $f_{SCL}=0$ kHz, (direct control mode) $A0/OSC=V_{DD}$ , at Tamb =25°C	-	20	
	$I_{DD4}$	$V_{DD}=5$ V, $f_{SCL}=0$ kHz, $R_{OSC}=1$ MOhm, $C_{OSC}=680$ pF at Tamb =25°C	-	40	
Low output voltage - on output SDA	$V_{OL}$	$V_{DD}=5$ V, $I_{OL}=3.0$ mA	-	0.4	V
Leakage current on input - on outputs A1, SCL, SDA	$I_{L1}$	$V_{DD}= 2.5$ to 6.0 V, $V_{SS} =0V$ , $V_I=V_{DD}$ or $V_{SS}$	-1	1	uA
Leakage current on input A2/BP2,BP1	$I_{L2}$	$V_{DD}=2.5$ to 6.0 V, $V_{SS} =0V$ $V_I=V_{DD}$ or $V_{SS}$	-5	5	uA
Input current - on output A2/BP2	$I_{PD}$	$V_{DD}= 2.5$ to 6.0 V, $V_I=V_{DD}$	-	5	uA
Leakage current on input - on output A0/OSC	$I_{L3}$	$V_{DD}= 2.5$ to 6.0 V, $V_I=V_{DD}$	-1	1	uA
Oscillator initial current	$I_{OSC}$	$V_{DD}= 2.5$ to 6.0 V, $V_{SS} =0V$ $V_I=V_{SS}$	-	5	uA
Low output voltage - on outputs S1-S32	$V_{OL1}$	$V_{DD}=5$ V, $I_{OL1}=0.3$ mA	-	0.8	V
High output voltage - on outputs S1-S32	$V_{OH1}$	$V_{DD}=5$ V, $I_{OH1}=-0.3$ mA	$V_{DD}-$ 0.8	-	V
Output current on outputs of LCD lines control - on outputs BP1,A2/BP2	$I_{load}$	$V_{DD}=5$ V, $V_{SS} =0V$ $V_O=V_{SS}+0.5V$ or $V_{DD}-0.5V$ or $(V_{SS}+V_{DD})/2+0.5V$	-100	100	uA
Low output voltage - on outputs BP1, A2/BP2	$V_{OL2}$	$V_{DD}=5$ V, $I_{OL2}=100$ mA	-	0.5	V
High output voltage - on outputs BP1, A2/BP2	$V_{OH2}$	$V_{DD}=5$ V, $I_{OH2}=-100$ mA	4.5	-	V
Mean level output voltage - on outputs BP1, A2/BP2	$V_{OL3}$	$V_{DD}=5$ V, $I_{OL3}=100$ mA	1.75	3.3	V
Frequency of signals on LCD control outputs	$f_{LCD}$	$R_{OSC}=1$ MOhm, $C_{OSC}=680$ pF	65	120	Hz

**Time diagrams**



$t_{BS} \leq 100 \text{ mks}$

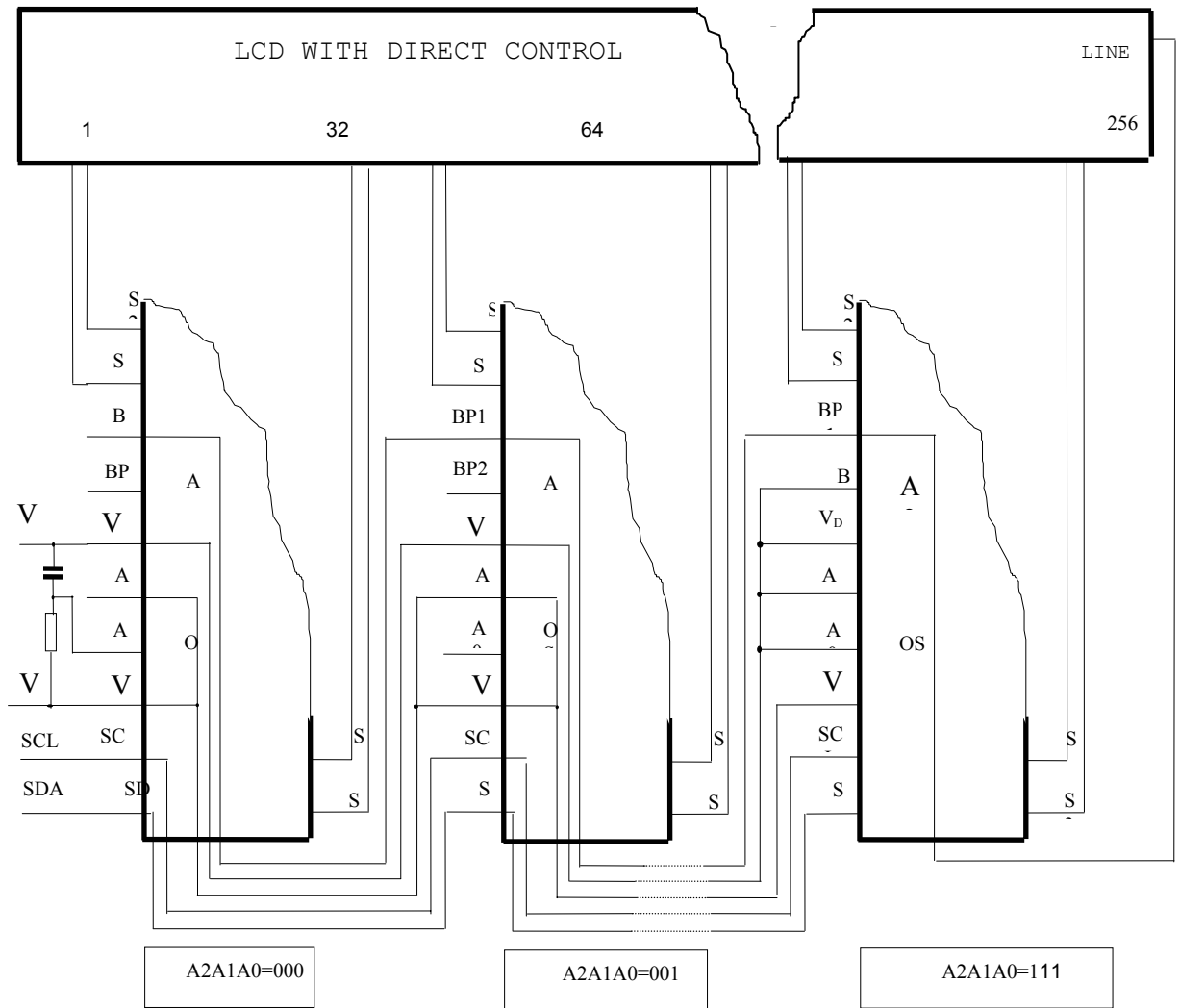
**Figure 3 - Time diagram of LCD driver operation**



$t_{BU} \geq 4.7 \mu s$ ,  $t_{LOW} \geq 4.7 \mu s$ ,  $t_{HIGH} \geq 4.0 \mu s$ ,  $t_r \leq 1.0 \text{ mks}$ ,  $t_f \leq 0.3 \mu s$ ,  $t_{HD;STA} \geq 4.0 \mu s$ ,  
 $t_{HD;DAT} \geq 0 \text{ ns}$ ,  $t_{SU;DAT} \geq 250 \text{ ns}$ ,  $t_{SU;STA} \geq 4.0 \text{ mks}$ ,  $t_{SU;STO} \geq 4.0 \text{ mks}$

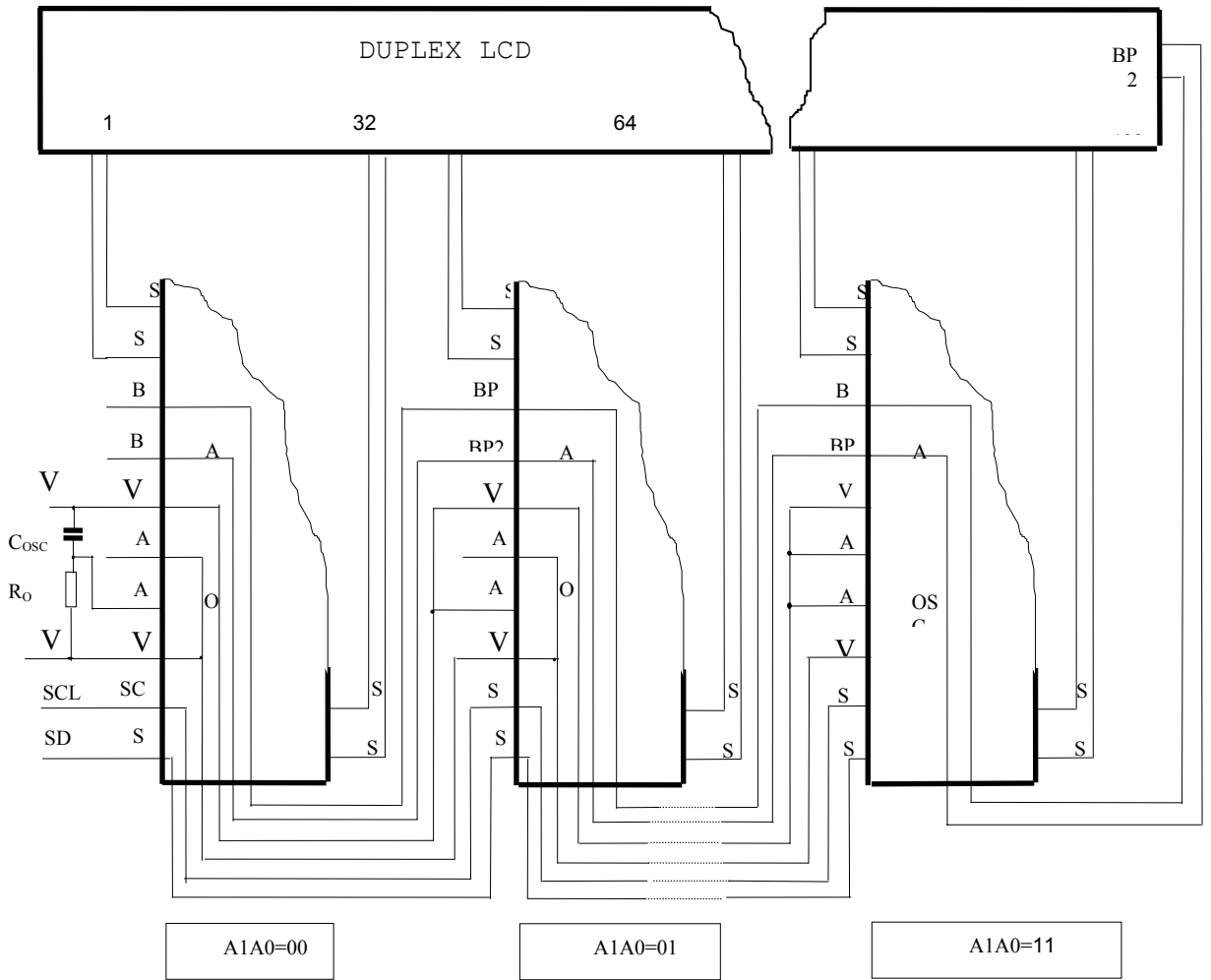
**Figure 4 - Time diagram of I<sup>2</sup>C bus operation**

Application circuits



Eight ICs INF8577CN control 256 driver segments.

Figure 5 - LCD driver with direct control



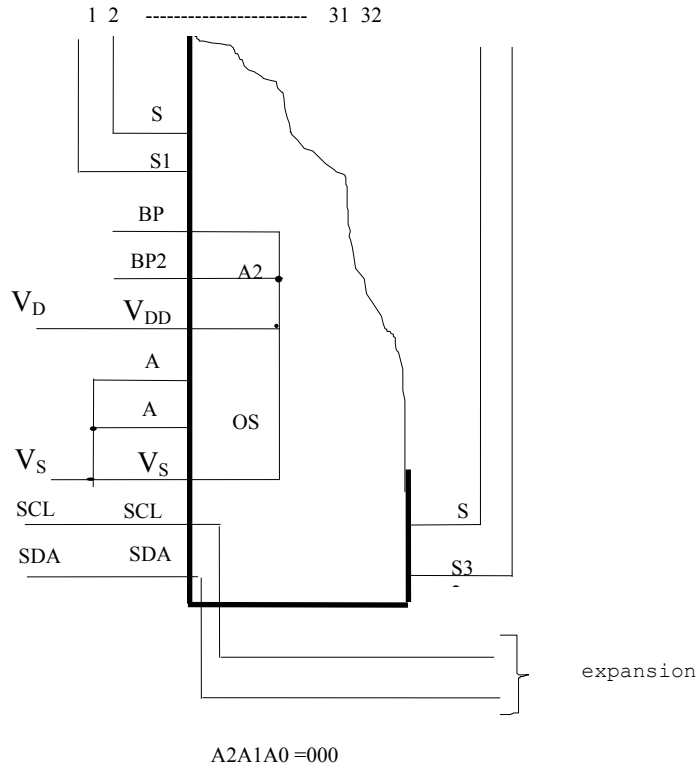
Eight ICs INF8577CN control 2 x 128 driver segments.

**Figure 6 - LCD driver with duplex control**

# INF8577N

INF8577CN

32-bit output bus



Output BP1 is always connected to V<sub>SS</sub>, output A0/OSC should be connected to V<sub>DD</sub>, or V<sub>SS</sub>.

**FIGURE 7 - USING IC INF8577CN AS**

**32-bit expander of I<sup>2</sup>C bus**

# INF8577N

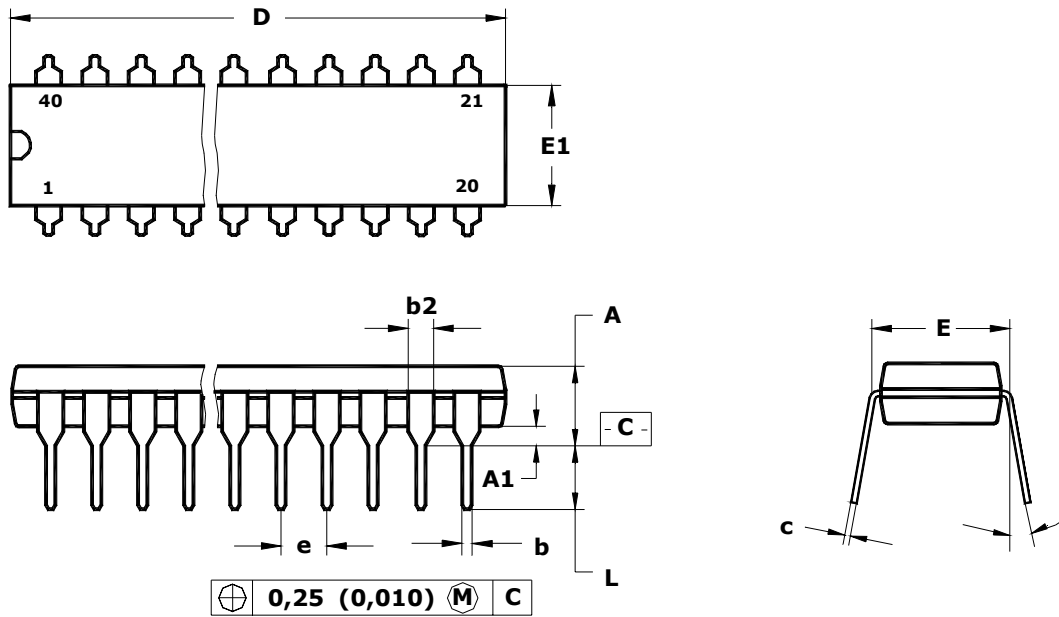
**Table 3 - Pins description**

Pin No.	Symbol	Description
01	S32	Output of LCD segment control
02	S31	Output of LCD segment control
03	S30	Output of LCD segment control
04	S29	Output of LCD segment control
05	S28	Output of LCD segment control
06	S27	Output of LCD segment control
07	S26	Output of LCD segment control
08	S25	Output of LCD segment control
09	S24	Output of LCD segment control
10	S23	Output of LCD segment control
11	S22	Output of LCD segment control
12	S21	Output of LCD segment control
13	S20	Output of LCD segment control
14	S19	Output of LCD segment control
15	S18	Output of LCD segment control
16	S17	Output of LCD segment control
17	S16	Output of LCD segment control
18	S15	Output of LCD segment control
19	S14	Output of LCD segment control
20	S13	Output of LCD segment control
21	S12	Output of LCD segment control
22	S11	Output of LCD segment control
23	S10	Output of LCD segment control
24	S9	Output of LCD segment control
25	S8	Output of LCD segment control
26	S7	Output of LCD segment control
27	S6	Output of LCD segment control
28	S5	Output of LCD segment control
29	S4	Output of LCD segment control
30	S3	Output of LCD segment control
31	S2	Output of LCD segment control
32	S1	Output of LCD segment control
33	BP1	Synchronization input when cascading / line control output
34	A2/BP2	Input of hardware address line and synchronization when cascading / line control output
35	V <sub>DD</sub>	Supply output from voltage source
36	A1	Input of hardware address line
37	A0/OSC	Input of hardware address line / oscillator input
38	V <sub>SS</sub>	Common output
39	SCL	Input of I <sup>2</sup> C bus clock signal line
40	SDA	Input / output of I <sup>2</sup> C bus data line



# INF8577N

## N SUFFIX PLASTIK DIP (MS-011AC)



Dimensions D, E1 don't include fin size which should not exceed 0,25 (0,010) per side.

	D	E1	A	b	b2	e	$\alpha$	L	E	c	A1
Millimeters											
min	50,30	12,32	—	0,36	0,77	2,54	0°	2,92	15,24	0,20	0,39
max	53,20	14,73	6,35	0,56	1,77		10°	5,08	15,87	0,38	
Inches											
min	1,980	0,485	—	0,014	0,030	0,100	0°	0,115	0,600	0,008	0,015
max	2,094	0,580	0,250	0,022	0,070		10°	0,200	0,625	0,015	

**Figure 8 - Overall dimensions of 2123.40-C package.**