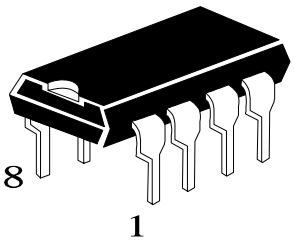
# 2048 x 8 -Bit CMOS EEPROM with I²C-bus interface

The INF85116N is an 16-Kbits (2048 x 8-bit) floating gate Electrically Erasable Programmable Read Only Memory (EEPROM). Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip, using a voltage multiplier. As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Only one INF85116N device is required to support all eight blocks of 256 x 8-bit each.




### *FEATURES*

- Low power CMOS
  -maximum active current 1.0 mA
  -maximum standby current 10 μA (at 5.5 V), typical 4 μA
- Non-volatile storage of 16-Kbits organized as eight blocks of 256x8-bits during 20 years ( at 55°C )
- Single supply (Ucc=2,7 ÷ 5,5 V);
- Automatically increased word's address
- On-chip voltage multiplier
- Serial input/output I²C-bus
- 1000000 ERASE/WRITE cycles per byte
- Internal timer for writing (no external components)
- Write operations: multi byte write mode to 32 bytes
- Write - protection input
- Power-on-reset

Temperature range: -40°C ÷ +85°C

### PIN DESCRIPTION

| Simbol | Pin | Description |
|---|---|---|
| n. c. | 1 | not connected |
| n. c | 2 | not connected |
| n. c | 3 | not connected |
| Uss | 4 | negative supply voltage |
| SDA | 5 | serial data input/output ( I²C-bus) |
| SCL | 6 | serial clock input ( I²C-bus) |
| WP | 7 | write - protection input |
| Ucc | 8 | positive supply voltage |

### PIN CONFIGURATION

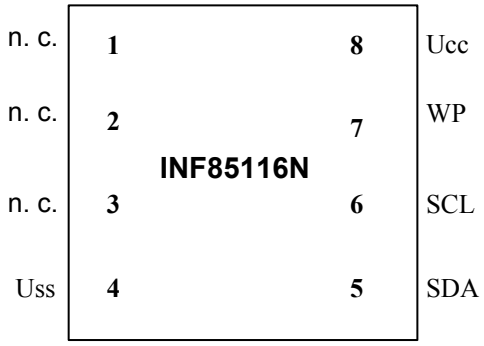



**Table 1. Quick reference data**

| Symbol | Parameter | min | max | Unit |
|---|---|---|---|---|



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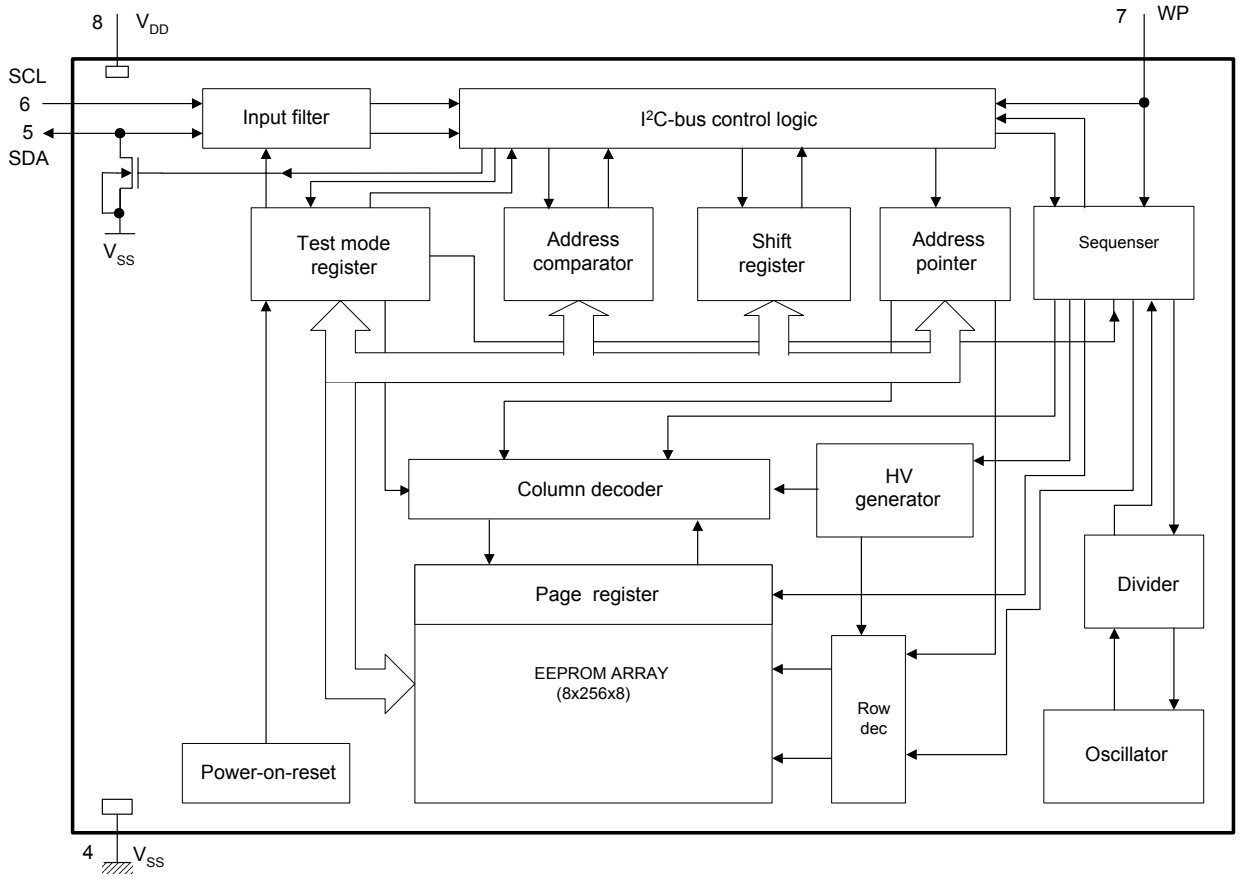
| | | | | |
|---|---|---|---|---|
| $U_{DD}$ | Supply voltage | 2.7 | 5.5 | V |
| $I_{OL}$ | LOW level output current | - | 6 | mA |
| $T_{amb}$ | Operating ambient temperature | -40 | +85 | °C |

## BLOCK DIAGRAM




## Table 2. Limiting values

| Symbol | Parameter | min | max | Unit |
|---|---|---|---|---|
| $U_{DD}$ | Supply voltage | -0.3 | 6.5 | V |
| Ui | Input voltage on any pin /$Z_i$/>500 Ω | -0.8 | 6.5 | V |
| Ii | Input current on any pin | - | 1 | mA |
| Io | Output current | - | 10 | mA |
| $T_{stg}$ | Storage temperature | -65 | +150 | °C |

## Table 3. Characteristics

| Symbol | Parameter | Conditions | min | max | Unit |
|---|---|---|---|---|---|
| $I_{DD(stb)}$ | Standby supply current | $U_{DD}$ = 2.7V<br>$U_{DD}$ = 5.5V | - | 6<br>10 | μA<br>μA |
| $I_{CCR}$ | Supply current READ | $f_{SCL}$=400κHz,<br>$U_{DD}$ = 5.5V | - | 1 | mA |
| $I_{CCW}$ | Supply current E / W | $f_{SCL}$=400κHz,<br>$U_{DD}$ = 5.5V | - | 1 | mA |
| **WP input (pin 7)** | | | | | |
| $U_{IL}$ | LOW level input voltage | | -0.8 | +0.1$U_{DD}$ | V |
| $U_{IH}$ | HIGH level input voltage | | 0.9$U_{DD}$ | $U_{DD}$+0.8 | V |
| **SCL input (pin 6)** | | | | | |
| $U_{IL}$ | LOW level input voltage | | -0.8 | +0.3$U_{DD}$ | V |
| $U_{IH}$ | HIGH level input voltage | | 0.7$U_{DD}$ | 6.5 | V |
| $I_{LI}$ | Input leakage current | $U_I$=$U_{DD}$ or $U_{SS}$ | - | ±1 | μA |
| $f_{SCL}$ | Clock input frequency | | 0 | 400 | kHz |
| $t_{sp}$ | Pulse width of spikes suppressed by filter | | 0<br>100 | | ns |
| $C_I$ | Input capacitance | $U_I$= $U_{SS}$ | - | 7 | pF |
| **SDA input/output (pin 5)** | | | | | |
| $U_{IL}$ | LOW level input voltage | | -0.8 | 0.3$U_{DD}$ | V |
| $U_{IH}$ | HIGH level input voltage | | 0.7$U_{DD}$ | 6.5 | V |
| $U_{OL1}$<br>$U_{OL2}$ | LOW level output voltage | $I_{OL}$=3mA,<br>$U_{DD}$ = $U_{DD\ (min)}$<br>$I_{OL}$=6mA,<br>$U_{DD}$ = $U_{DD\ (min)}$ | - | 0.4<br><br>0.6 | V |
| $I_{LO}$ | Output leakage current | $U_{OH}$=$U_{DD}$ | - | 1 | μA |
| $t_{O(F)}$ | Output fall time from $U_{IHmin}$ to $U_{ILmax}$ | with up to 3mA sink current at $U_{OL1}$<br>with up to 6mA sink current at $U_{OL2}$ | 20+0.1 $C_B$*<br>20+0.1 $C_B$ | 250<br>250 | ns<br>ns |
| $t_{SP}$ | Pulse width of spikes suppressed by filter | | 0 | 100 | ns |
| $C_I$ | Input capacitance | $U_I$=0V | - | 10 | pF |
| $t_{E/W}$ | E/W cycle time | | - | 10 | ms |
| $N_{E/W}$ | E/W cycle per byte | $T_{amb}$ =(-40-+85) °C,<br>$T_{amb}$ =22°C | 100000<br>1000000 | - | |
| $t_S$ | Data retention time | $T_{amb}$ = 55°C | 20 | - | years |

∗ - The bus capacitance ranges from 10 to 400pF ( $C_B$ = total capacitance of one bus line in pF)

## Table 4. I²C-bus characteristics

| Symbol | Parameter | Condi-tions | Standard mode | | Fast mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | min | max | min | max | |
| $f_{SCL}$ | Clock frequency | | 0 | 100 | 0 | 400 | kHz |
| $t_{BUF}$ | Time the bus must be free before | - | 4.7 | - | 1.3 | - | µs |
| $t_{HD, STA}$ | START condition hold time after which first clock pulse is generated | - | 4.0 | - | 0.6 | - | µs |
| $t_{LOW}$ | LOW level clock period | - | 4.7 | - | 1.3 | - | µs |
| $t_{HIGH}$ | HIGH level clock period | - | 4.0 | - | 0.6 | - | µs |
| $t_{SU, STA}$ | Set-up time for START condition | repeated start | 4.7 | - | 0.6 | - | µs |
| $t_{HD, DAT}$ | Data hold time for CBUS compatible masters | - | 5 | - | - | - | µs |
| $t_{HD, DAT}$ | Data hold time for I²C - bus devices | note 1 | 0 | - | 0 | - | ns |
| $t_{SU, DAT}$ | Data set-up time | - | 250 | - | 100 | - | ns |
| $t_R$ | SDA and SCL rise time | - | - | 1000 | 20+0.1 $C_b$ (2) | 300 | ns |
| $t_F$ | SDA and SCL fall time | - | - | 300 | 20+0.1 $C_b$ (2) | 300 | ns |
| $t_{SU, STO}$ | Set-up time for STOP condition | - | 4.0 | - | 0.6 | - | µs |

Notes:
**1.** The hold time required (not greater than 300 ns) to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter.
**2**. $C_b$ = total capacitance of one bus line in pF.