Features

- 80C51 Core with 12 or 6 Clocks Per Instruction
- 768 bytes RAM
- AT83C5122 with 32 Kbytes ROM
- AT85C5122 with 32 Kbytes Code RAM
- AT89C5122 with 32 Kbytes Flash RAM
- Multi-protocol Smart Card Interface
  - Certified According to ISO7816, EMV2000, GIE-CB and WHQM Standards
  - Asynchronous Protocols T = 0 and T = 1, with Direct and Inverse Modes
  - Step-Up/Down Converter with Programmable Voltage Output: 5V and 3V (60 mA), 1.8V (20 mA)
  - 4 kV ESD Protection (MIL/STD 833 Class 3)
- Alternate Card Support with CLK, IO and RST
- USB Module 7 Endpoints Programmable with In or Out Directions and with ISO, Bulk or Interrupt Transfers
- Keyboard Interrupt Interface on Port 5 (8 bits)
- UART with Integrated Baud Rate Generator (BRG)
- SPI Interface (Master Slave)
- 8 MHz on-chip Oscillator (Possible Operation at 8 MHz without External Capacitors)
  - Analog PLL for 96 MHz Synthesis. Possible 48 MHz Clock Input
- Two 16-bit Timer/Counters: T0 and T1
- Five 8-bit I/O Ports, One 6-bit
- Seven LED Outputs with Programmable Current Sources: 2-4-10 mA
- Hardware Watchdog and Power-fail Detector (PFD)
- Idle and Power-down Modes
- Self Powered USB
- Low Power
  - 30 mA Maximum Operating Current (at 32 MHz X1)
  - 100 µA Maximum Power-down Current at 5.4V (without Smart Card and USB)
- Voltage Ranges
  - 3.6 to 5.5V (-M Version)
- Commercial and Industrial Temperature Ranges
- Packages: VQFP64, PLCC28

Description

AT8xC5122 is a high-performance CMOS derivative of the 80C51 8-bit microcontrollers optimized for USB keyboard with smart card reader applications.

AT8xC5122 retains the features of the Atmel 80C51 with 32 Kbytes ROM capacity, 768 bytes of internal RAM, a 4-level interrupt system, two 16-bit timer/counters (T0/T1), a full duplex enhanced UART (EUART) with baud rate generator (BRG) and an on-chip oscillator.

In addition, AT8xC5122 has a USB 2.0 full speed function controller with seven Endpoints, a multi-protocol smart card interface, a dual data pointer, seven programmable LED current sources (2-4-10 mA) and a hardware watchdog.

AT89C5122 Flash RAM version and AT85C5122 Code RAM version with 32 Kbytes memory can be loaded by In-System Programming (ISP) software residing in the on-chip ROM from USB or UART.

AT8xC5122 have 2 software-selectable modes of reduced activity for further reduction in power consumption.

C51 Microcontroller with USB and Smart Card Reader Interfaces

AT83C5122
AT85C5122
AT89C5122

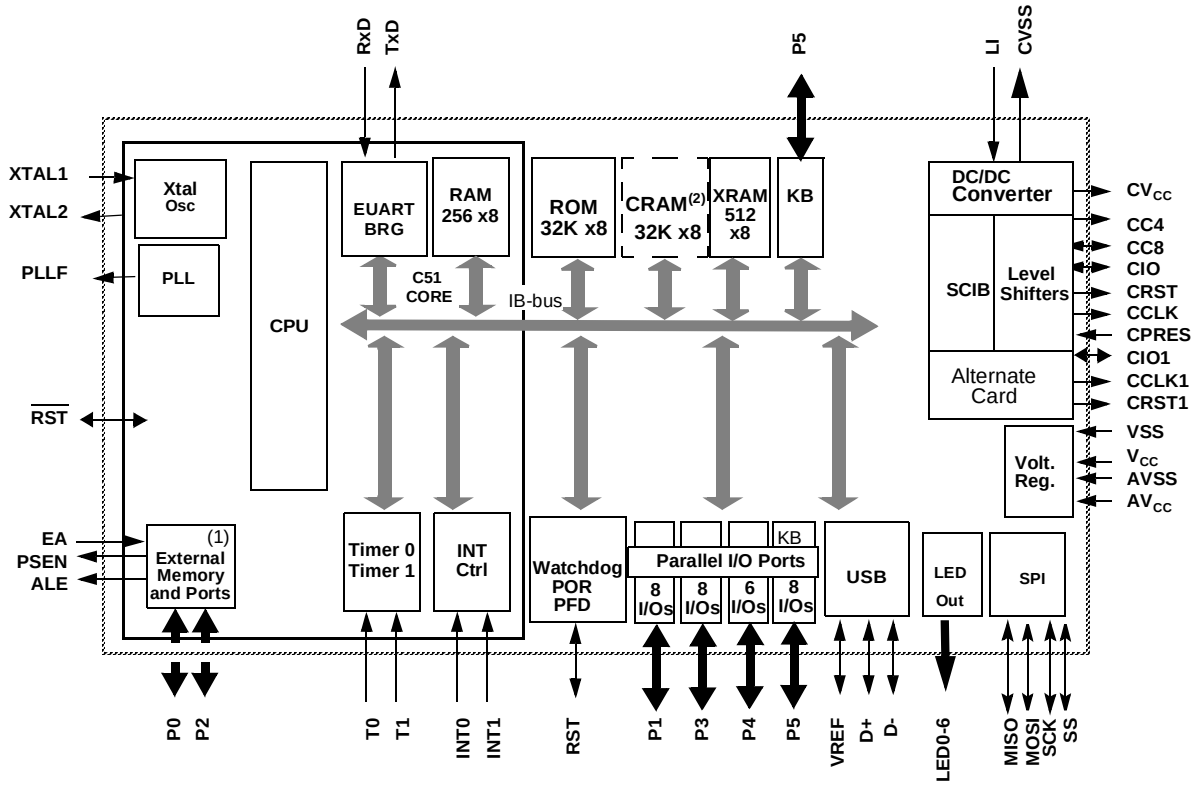
Preliminary

Summary

Rev. 4198AS–SCR–11/02

Note: This is a summary document. For more information, please contact cardreader@nto.atmel.com.

Block Diagram



1. Only on high-pin count version
2. Only on ROM/RAM version

Pin Configurations

Figure 1. VQFP64 Pinout

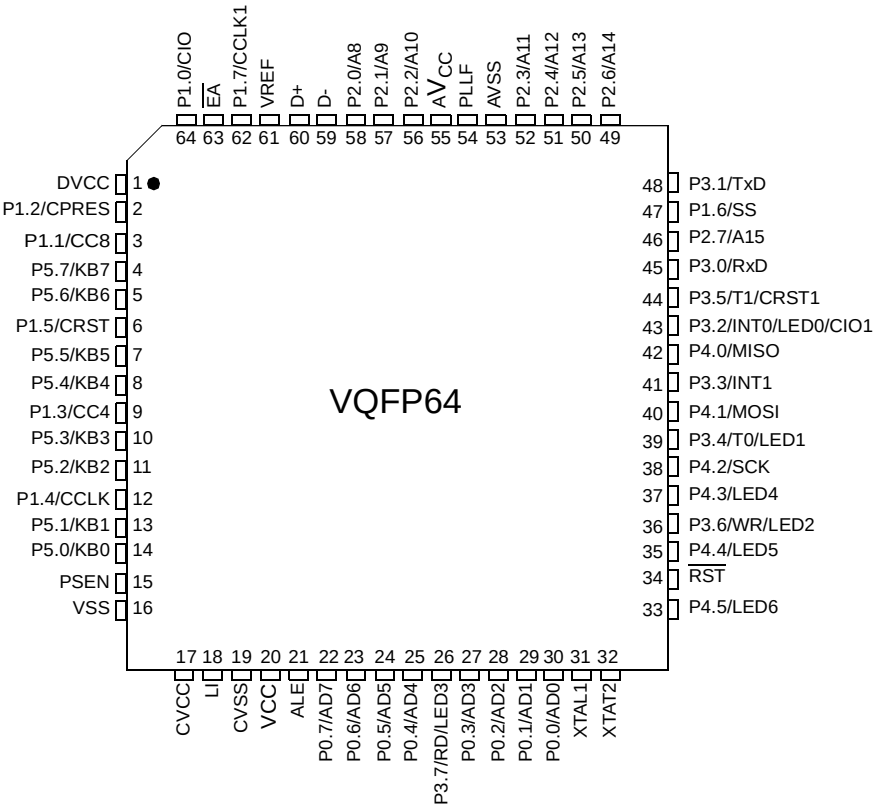
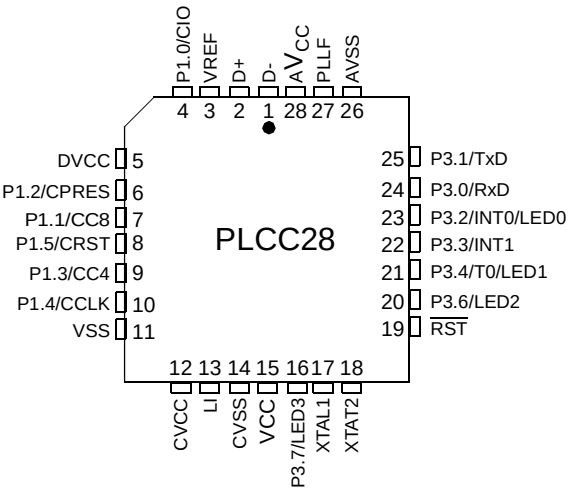


Figure 2. PLCC28 Pinout



Pin Description

All the AT8xC5122 signals are detailed in Table 1:

Table 1. Pin Description

Port	Pin Number VQFP64	Pin Number PLCC28	Internal Power Supply	ESD	I/O	Reset Level	Alt	Reset Config	Conf 1	Conf 2	Conf 3	Led
P0.0	30	-	VCC	2 kV	I/O	Float	AD0	P0		KB_OUT	Push-pull	
P0.1	29	-	VCC	2 kV	I/O	Float	AD1	P0		KB_OUT	Push-pull	
P0.2	28	-	VCC	2 kV	I/O	Float	AD2	P0		KB_OUT	Push-pull	
P0.3	27	-	VCC	2 kV	I/O	Float	AD3	P0		KB_OUT	Push-pull	
P0.4	25	-	VCC	2 kV	I/O	Float	AD4	P0		KB_OUT	Push-pull	
P0.5	24	-	VCC	2 kV	I/O	Float	AD5	P0		KB_OUT	Push-pull	
P0.6	23	-	VCC	2 kV	I/O	Float	AD6	P0		KB_OUT	Push-pull	
P0.7	22	-	VCC	2 kV	I/O	Float	AD7	P0		KB_OUT	Push-pull	
P1.0	64	4	CVCC	4 kV	I/O	0	CIO	Port51	CVCC inactive at reset			
P1.1	3	7	CVCC	4 kV	I/O	0	CC8	Port51	CVCC inactive at reset			
P1.2	2	6	VCC	2 kV	I/O	1	CPRES	Port51	Weak & medium pull-ups can be deconnected			
P1.3	9	9	CVCC	4 kV	I/O	0	CC4	Port51	CVCC inactive at reset			
P1.4	12	10	CVCC	4 kV	O	0	CCLK	Push-pull	CVCC inactive at reset			
P1.5	6	8	CVCC	4 kV	O	0	CRST	Push-pull	CVCC inactive at reset			
P1.6	47	-	VCC	2 kV	I/O	1	SS	Port51				
P1.7	62	-	VCC	2 kV	I/O	1	CCLK1	Port51				
P2.0	58	-	VCC	2 kV	I/O	1	A8	Port51	Push-pull	KB_OUT	Input WPU	
P2.1	57	-	VCC	2 kV	I/O	1	A9	Port51	Push-pull	KB_OUT	Input WPU	
P2.2	56	-	VCC	2 kV	I/O	1	A10	Port51	Push-pull	KB_OUT	Input WPU	
P2.3	52	-	VCC	2 kV	I/O	1	A11	Port51	Push-pull	KB_OUT	Input WPU	
P2.4	51	-	VCC	2 kV	I/O	1	A12	Port51	Push-pull	KB_OUT	Input WPU	
P2.5	50	-	VCC	2 kV	I/O	1	A13	Port51	Push-pull	KB_OUT	Input WPU	
P2.6	49	-	VCC	2 kV	I/O	1	A14	Port51	Push-pull	KB_OUT	Input WPU	
P2.7	46	-	VCC	2 kV	I/O	1	A15	Port51	Push-pull	KB_OUT	Input WPU	

Table 1. Pin Description (Continued)

Port	Pin Number VQFP64	Pin Number PLCC28	Internal Power Supply	ESD	I/O	Reset Level	Alt	Reset Config	Conf 1	Conf 2	Conf 3	Led
P3.0	45	24	VCC	2 kV	I/O	1	RxD	Port51	Push-pull	KB_OUT	Input WPU	
P3.1	48	25	VCC	2 kV	I/O	1	TxD	Port51	Push-pull	KB_OUT	Input WPU	
P3.2	43	23	VCC	2 kV	I/O	1	INT0	Port51				LED0
P3.3	41	22	VCC	2 kV	I/O	1	INT1	Port51	Push-pull	KB_OUT	Input WPU	
P3.4	39	21	VCC	2 kV	I/O	1	T0	Port51	Push-pull	KB_OUT	Input WPU	LED1
P3.5	44	-	VCC	2 kV	I/O	1	T1	Port51				
P3.6	36	20	VCC	2 kV	I/O	1	WR	Port51				LED2
P3.7	26	16	VCC	2 kV	I/O	1	RD	Port51				LED3
P4.0	42	-	VCC	2 kV	I/O	1	MISO	Port51				
P4.1	40	-	VCC	2 kV	I/O	1	MOSI	Port51				
P4.2	38	-	VCC	2 kV	I/O	1	SCK	Port51				
P4.3	37	-	VCC	2 kV	I/O	1		Port51	Push-pull	KB_OUT	Input MPU	LED4
P4.4	35	-	VCC	2 kV	I/O	1		Port51	Push-pull	KB_OUT	Input MPU	LED5
P4.5	33	-	VCC	2 kV	I/O	1		Port51	Push-pull	KB_OUT	Input MPU	LED6
P5.0	14	-	VCC	2 kV	I/O	1	KB0	Port51	Push-pull	Input MPU	Input WPU	
P5.1	13	-	VCC	2 kV	I/O	1	KB1	Port51	Push-pull	Input MPU	Input WPU	
P5.2	11	-	VCC	2 kV	I/O	1	KB2	Port51	Push-pull	Input MPU	Input WPU	
P5.3	10	-	VCC	2 kV	I/O	1	KB3	Port51	Push-pull	Input WPD	Input WPU	
P5.4	8	-	VCC	2 kV	I/O	1	KB4	Port51	Push-pull	Input WPD	Input WPU	
P5.5	7	-	VCC	2 kV	I/O	1	KB5	Port51	Push-pull	Input WPD	Input WPU	
P5.6	5	-	VCC	2 kV	I/O	1	KB6	Port51	Push-pull	Input WPD	Input WPU	

Table 1. Pin Description (Continued)

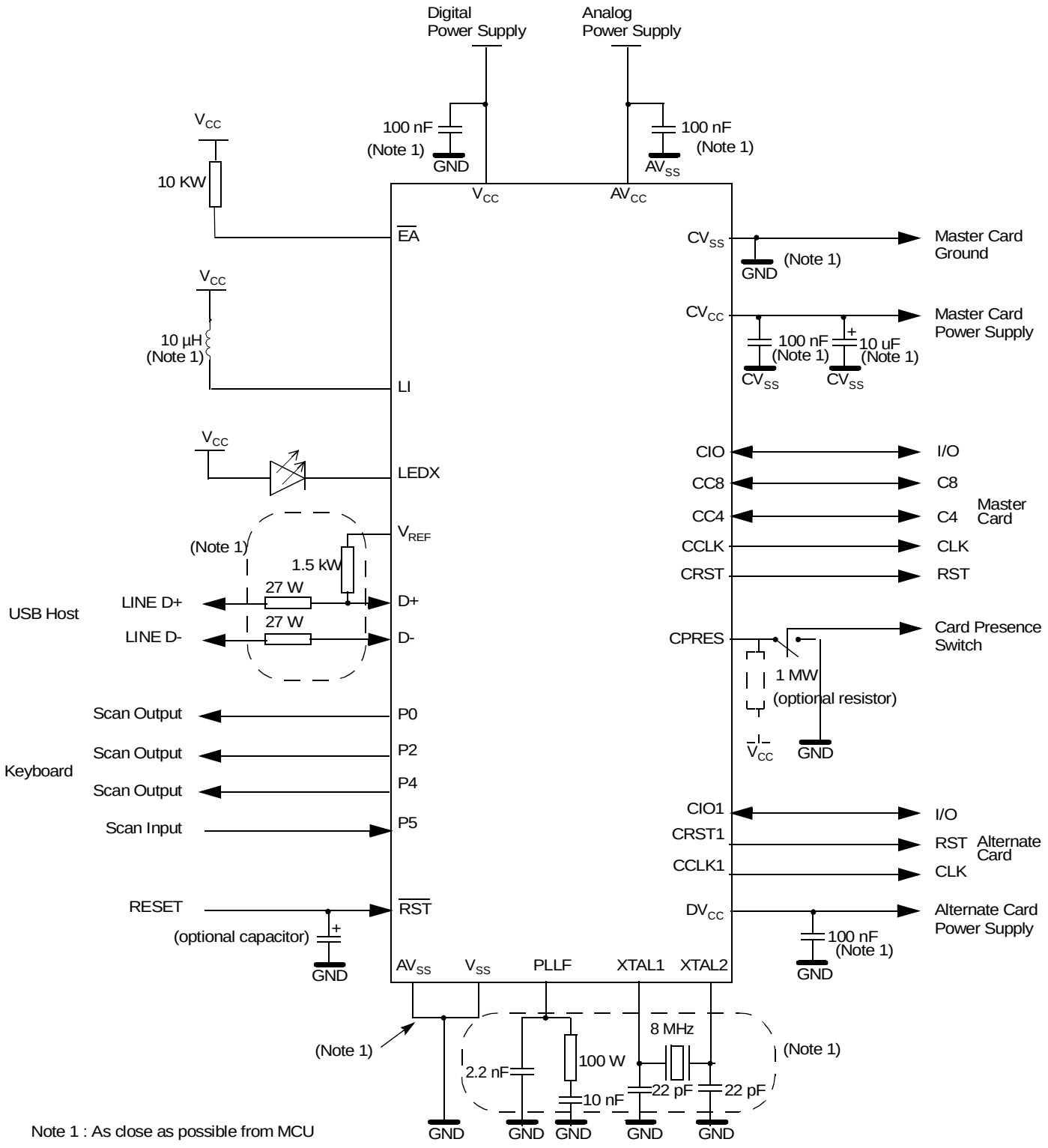
Port	Pin Number VQFP64	Pin Number PLCC28	Internal Power Supply	ESD	I/O	Reset Level	Alt	Reset Config	Conf 1	Conf 2	Conf 3	Led
P5.7	4	-	VCC	2 kV	I/O	1	KB7	Port51	Push-pull	Input WPD	Input WPU	
$\overline{RST}$	34	19	VCC		I/0		**Reset Input** Holding this pin low for 64 oscillator periods while the oscillator is running resets the device. The Port pins are driven to their reset conditions when a voltage lower than V_{IL} is applied, whether or not the oscillator is running. This pin has an internal pull-up resistor which allows the device to be reset by connecting a capacitor between this pin and VSS. Asserting $\overline{RST}$ when the chip is in Idle mode or Power-down mode returns the device to normal operation. The output is active for at least 12 oscillator periods when an internal reset occurs.					
D+	60	2	DVCC		I/O		**USB Positive Data Upstream Port** This pin requires an external 1.5 kΩ pull-up to VREF for full speed					
D-	59	1	DVCC		I/O		**USB Negative Data Upstream Port**					
VREF	61	3	AVCC		O		**USB Voltage Reference** : 3.0 < VREF < 3.6V VREF can be connected to D+ with a 1.5 kΩ resistor. The VREF voltage is controlled by software.					
XTAL1	31	17	VCC		I		**Input to the on-chip invertor oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin.					
XTAL2	32	18	VCC		O		**Output of the on-chip invertor oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave XTAL2 unconnected.					
$\overline{EA}$	63	-	VCC		I		**External Access Enable** $\overline{EA}$ must be strapped to ground in order to enable the device to fetch code from external memory locations 0000h to FFFFh. If security level 1 is programmed, $\overline{EA}$ will be latched on reset.					
ALE	21	-	VCC		O		**Address Latch Enable/Program Pulse:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming. ALE can be disabled by setting SFR's AUXR.0 bit. With this bit set, ALE will be inactive during internal fetches					
$\overline{PSEN}$	15	-	VCC		O		**Program Strobe Enable:** The read strobe to external program memory. When executing code from the external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.					
PLLF	54	27	AVCC		O		**PLL Low Pass Filter input** Receives the RC network of the PLL low pass filter.					
AVCC	55	28			PWR		**Analog Supply Voltage** AVCCis used to supply the on-chip PLL and the USB drivers.					
VCC	20	15			PWR	VCC	**Supply Voltage** VCC is used to power the internal voltage regulators and internal I/O's.					

Table 1. Pin Description (Continued)

Port	Pin Number VQFP64	Pin Number PLCC28	Internal Power Supply	ESD	I/O	Reset Level	Alt	Reset Config	Conf 1	Conf 2	Conf 3	Led
LI	18	13			PWR		**DC/DC Input** LI must be tied to VCC through an external coil (typically 4.7 µH) and provide the current for the pump charge of the DC/DC converter					
CVCC	17	12			PWR		**Card Supply Voltage** CVCC is the programmable voltage output for the card interface. It must be connected to an external decoupling capacitor.					
DVCC	1	5			PWR		**Digital Supply Voltage** DVCC is used to supply the digital core and internal I/O's. It is internally connected to the output of a 3.3V voltage regulator and must be connected to an external decoupling capacitor.					
CVSS	19	14			GND		**DC/DC Ground** CVSS is used to sink high shunt currents from the external coil.					
VSS	16	11			GND		**Digital Ground** VSS is used to supply the buffer ring and the digital core.					
AVSS	53	26			GND		**Analog Ground** AVSS is used to supply the on-chip PLL and the USB drivers.					

Typical Application

Figure 3. Typical Application Schematic



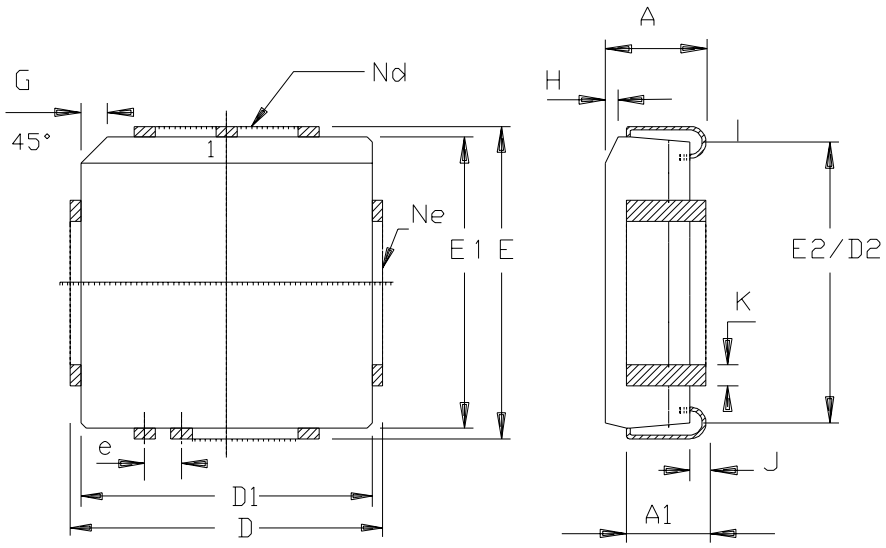
Note 1 : As close as possible from MCU

Ordering Information

Part-Number	CodeMemory Size (bytes)	Supply Voltage (V)	Temperature Range	Max Frequency (MHz)	Package	Packing
AT83C5122xxx-RDTIM	32K ROM	3.6 - 5.5	Industrial	32	VQFP64	Tray
AT83C5122xxx-RDRIM	32K ROM	3.6 - 5.5	Industrial	32	VQFP64	Reel
AT83C5122xxx-SISIM	32K ROM	3.6 - 5.5	Industrial	32	PLCC28	Stick
AT83C5122xxx-SIRIM	32K ROM	3.6 - 5.5	Industrial	32	PLCC28	Reel
AT85C5122-RDTIM	32K RAM	3.6 - 5.5	Industrial	32	VQFP64	Tray
AT85C5122-RDRIM	32K RAM	3.6 - 5.5	Industrial	32	VQFP64	Reel
AT85C5122-SISIM	32K RAM	3.6 - 5.5	Industrial	32	PLCC28	Stick
AT85C5122-SIRIM	32K RAM	3.6 - 5.5	Industrial	32	PLCC28	Reel
AT89C5122-RDTIM	32K FLASH RAM	3.6 - 5.5	Industrial	32	VQFP64	Tray
AT89C5122-RDRIM	32K FLASH RAM	3.6 - 5.5	Industrial	32	VQFP64	Reel
AT89C5122-SISIM	32K FLASH RAM	3.6 - 5.5	Industrial	32	PLCC28	Stick
AT89C5122-SIRIM	32K FLASH RAM	3.6 - 5.5	Industrial	32	PLCC28	Reel

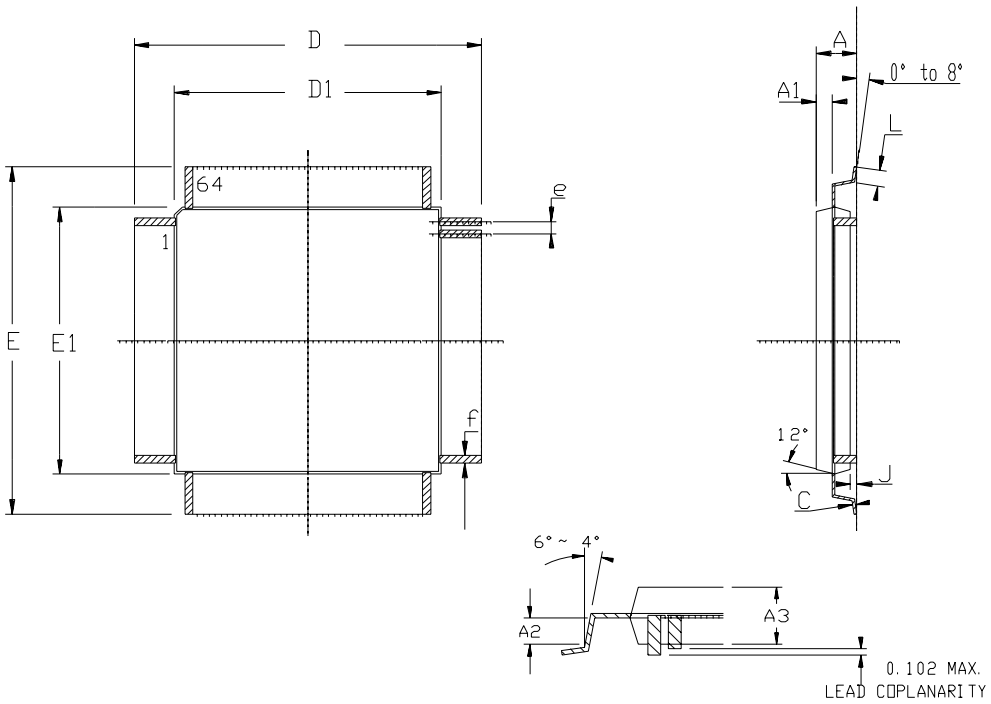
Packaging Information

PLCC28



	MM		INCH	
A	4.20	4.57	.165	.180
A1	2.29	3.04	.090	.120
D	12.32	12.57	.485	.495
D1	11.43	11.58	.450	.456
D2	9.91	10.92	.390	.430
E	12.32	12.57	.485	.495
E1	11.43	11.58	.450	.456
E2	9.91	10.92	.390	.430
e	1.27	BSC	.050	BSC
G	1.07	1.22	.042	.048
H	1.07	1.42	.042	.056
J	0.51	-	.020	-
K	0.33	0.53	.013	.021
Nd	7		7	
Ne	7		7	
PKG STD	00			

VQFP64



	MM		INCH	
	Min	Max	Min	Max
A	–	1.60	–	.063
A1	0.64 REF		.025 REF	
A2	0.64 REF		.025 REF	
A3	1.35	1.45	.053	.057
D	11.75	12.25	.463	.483
D1	9.90	10.10	.390	.398
E	11.75	12.25	.463	.483
E1	9.90	10.10	.390	.398
J	0.05	–	.002	–
L	0.45	0.75	.018	.030
e	0.50 BSC		.0197 BSC	
f	0.25 BSC		.010 BSC	

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