DATA SHEET

TDA6404; TDA6405; TDA6405A
5 V mixer/oscillator-PLL synthesizers for hyperband tuners

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Philips
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PHILIPS

5 V mixer/oscillator-PLL synthesizers for hyperband tuners

TDA6404; TDA6405; TDA6405A

FEATURES

- Single chip 5 V mixer/oscillator-PLL synthesizer for hyperband tuners
- I^2C-bus protocol
- 3 PNP band switch buffers (25 mA)
- 33 V tuning voltage output
- In-lock detector
- 5-level Analog-to-Digital Converter (ADC)
- 15-bit programmable divider
- Programmable reference divider ratio (512, 640 or 1024)
- Programmable charge pump current
- Balanced mixer with a common emitter input for VHF (single input)
- Balanced mixer with a common base input for UHF (double input)
- 4-pin common emitter oscillator for VHF
- 4-pin common emitter oscillator for UHF
- IF amplifier with a low output impedance to drive a SAW filter directly (≈2 kΩ load)
- Low power, low radiation, small size

APPLICATIONS

- Hyperband tuners for Europe using a 2-band mixer/oscillator in a switched concept.

GENERAL DESCRIPTION

The TDA6404, TDA6405 and TDA6405A are programmable 2-band mixer/oscillator-PLL synthesizers intended for VHF/UHF and hyperband tuners (see Fig.1).

The devices include two double balanced mixers and two oscillators for the VHF and UHF band, an IF amplifier and a PLL synthesizer. With proper oscillator application and by using a switchable inductor to split the VHF band into two sub-bands (the full VHF/UHF and hyperband) the TV bands can be covered.

Two pins are available between the mixer output and the IF amplifier input to enable IF filtering for improved signal handling. Three PNP ports are provided for band switching. Band selection is made according to the band switch bits VHFL, VHFH and UHF.

The PLL synthesizer consists of a divide-by-eight prescaler, a 15-bit programmable divider, a 4 MHz crystal oscillator and its programmable reference divider and a phase comparator combined with a charge pump which drives the tuning amplifier, including 33 V output.

Depending on the reference divider ratio (512, 640 or 1024), the phase comparator operates at 7.8125 kHz, 6.25 kHz or 3.90625 kHz.

The devices are controlled according to the I^2C-bus format. The in-lock detector bit FL is set to logic 1 when the loop is locked and is read on the SDA line (status byte) during a read operation. The ADC input is available for digital Automatic Frequency Control (AFC). The ADC code is read during a read operation on the I^2C-bus (see Table 9). In test mode, pin ADC is used as a test output for f_{REF} and $\frac{1}{2}f_{DIV}$.

When the charge pump current switch mode is activated and the loop is phase-locked the charge pump current value is automatically switched to LOW. This is to improve carrier-to-noise ratio. The status of this feature can be read in the ACPS flag during a read operation on the I^2C-bus (see Table 7).

Five serial bytes (including address byte) are required for the I^2C-bus format to address the devices, select the VCO frequency, program the three PNP ports, set the charge pump current and to set the reference divider ratio. The devices have four independent I^2C-bus addresses which can be selected by applying a specific voltage on the AS input (see Table 4).

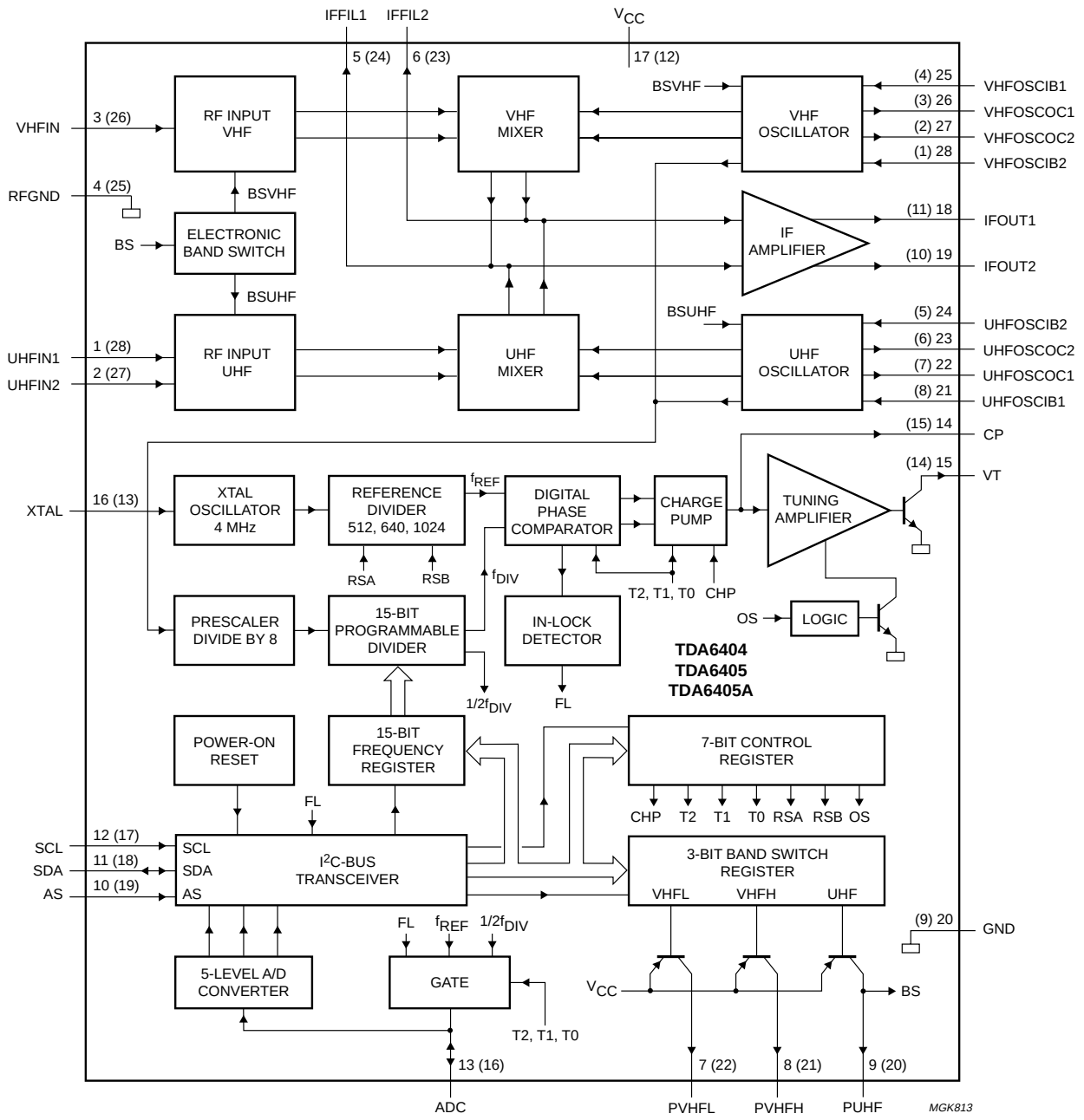
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	operating	4.5	5	5.5	V
I_{CC}	supply current	all PNP ports are 'OFF'	–	78	–	mA
f_{XTAL}	crystal oscillator frequency	R_{XTAL} = 25 to 150 Ω	3.2	4.0	4.48	MHz
$I_{o(PNP)}$	PNP port output current		–	–	25	mA
T_{stg}	IC storage temperature		–40	–	+150	°C
T_{amb}	operating ambient temperature		–20	–	+85	°C
$f_{(i)RF}$	RF input frequency	VHF band	45.25	–	399.25	MHz
		UHF band	407.25	–	855.25	MHz
G_V	voltage gain	VHF band	–	27	–	dB
		UHF band	–	38	–	dB
F	noise figure	VHF band	–	8	–	dB
		UHF band	–	8.5	–	dB
V_o	output voltage causing 1% cross modulation in channel	VHF band	–	119	–	dBμV
		UHF band	–	118	–	dBμV

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA6404TS; TDA6405TS; TDA6405ATS	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1

BLOCK DIAGRAM



The pin numbers in parenthesis represent the TDA6405 and TDA6405A.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN		DESCRIPTION
	TDA6404	TDA6405; TDA6405A	
UHFIN1	1	28	UHF input 1
UHFIN2	2	27	UHF input 2
VHFIN	3	26	VHF input
RFGND	4	25	RF ground
IFFIL1	5	24	IF filter output 1
IFFIL2	6	23	IF filter output 2
PVHFL	7	22	PNP port output for VHF low band
PVHFH	8	21	PNP port output for VHF high band
PUHF	9	20	PNP port output for UHF band
AS	10	19	address selection input
SDA	11	18	serial data input/output (I^2C-bus)
SCL	12	17	serial clock input (I^2C-bus)
ADC	13	16	Analog-to-Digital Converter input/output
CP	14	15	charge pump output
VT	15	14	tuning output
XTAL	16	13	crystal oscillator input
V_{CC}	17	12	supply voltage
IFOUT1	18	11	IF amplifier output 1
IFOUT2	19	10	IF amplifier output 2
GND	20	9	ground
UHFOSCIB1	21	8	UHF oscillator base input 1
UHFOSCOC1	22	7	UHF oscillator collector output 1
UHFOSCOC2	23	6	UHF oscillator collector output 2
UHFOSCIB2	24	5	UHF oscillator base input 2
VHFOSCIB1	25	4	VHF oscillator base input 1
VHFOSCOC1	26	3	VHF oscillator collector output 1
VHFOSCOC2	27	2	VHF oscillator collector output 2
VHFOSCIB2	28	1	VHF oscillator base input 2

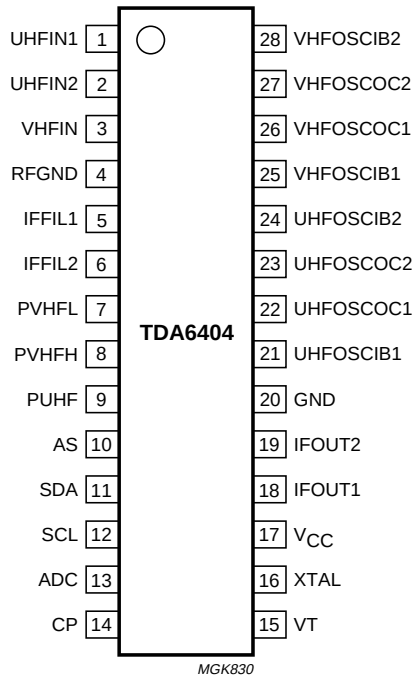


Fig.2 Pin configuration for TDA6404.

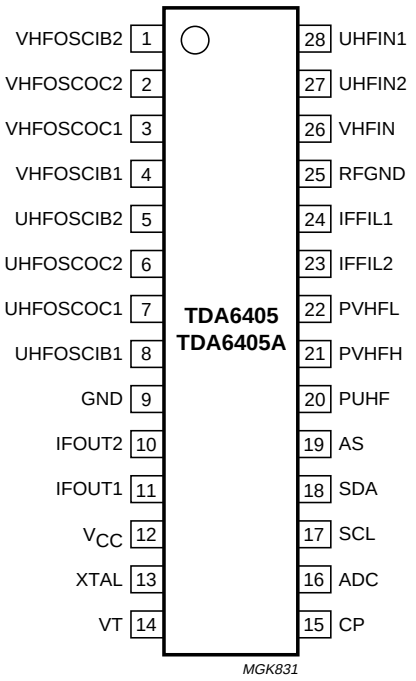


Fig.3 Pin configuration for TDA6405(A)

FUNCTIONAL DESCRIPTION

The devices are controlled via the I²C-bus.
For programming, there is one module address (7 bits) and the R/$\overline{W}$ bit for selecting the read or write mode.

Write mode

Data bytes can be sent to the devices after the address transmission (first byte) by setting the R/$\overline{W}$ bit to logic 0. Four data bytes are needed to fully program the devices. The I²C-bus transceiver has an auto-increment facility which permits the programming of the devices within one single transmission (address + 4 data bytes).

The devices can also be partially programmed, providing that the first data byte following the address is divider byte 1 (DB1) or control byte (CB). The bits in the data bytes are defined in Tables 1 and 2.

The first bit of the data byte transmitted indicates whether frequency data (first bit = 0) or control and band switch data (first bit = 1) will follow. Until an I²C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the devices. The frequency register is loaded after the 8th clock pulse of the second divider byte (DB2). The control register is loaded after the 8th clock pulse of the CB. The band switch register is loaded after the 8th clock pulse of the band switch byte (BB).

Table 1 I²C-bus mode, write data format for the TDA6404 and TDA6405

NAME	BYTE	BITS								ACK
		MSB							LSB	
Address byte	ADB	1	1	0	0	0	MA1	MA0	R/$\overline{W}$ = 0	A
Divider byte 1	DB1	0	N14	N13	N12	N11	N10	N9	N8	A
Divider byte 2	DB2	N7	N6	N5	N4	N3	N2	N1	N0	A
Control byte	CB	1	CHP	T2	T1	T0	RSA	RSB	OS	A
Band-switch byte	BB	X	X	X	X	X	UHF	VHFH	VHFL	A

Table 2 I²C-bus mode, write data format for the TDA6405A

NAME	BYTE	BITS								ACK
		MSB							LSB	
Address byte	ADB	1	1	0	0	0	MA1	MA0	R/$\overline{W}$ = 0	A
Divider byte 1	DB1	0	N14	N13	N12	N11	N10	N9	N8	A
Divider byte 2	DB2	N7	N6	N5	N4	N3	N2	N1	N0	A
Control byte	CB	1	CHP	T2	T1	T0	RSA	RSB	OS	A
Band-switch byte	BB	X	X	X	X	UHF	X	VHFH	VHFL	A

I²C-bus address selection

The module address contains programmable address bits (MA1 and MA0) which offer the possibility of having several synthesizers (up to 4) in one system by applying a specific voltage on the AS input. The relationship between MA1 and MA0 and the input voltage applied to the AS input is given in Table 4.

Table 3 Description of symbols used in Tables 1 and 2

SYMBOL	DESCRIPTION
A	acknowledge
MA1 and MA0	programmable address bits (see Table 4)
N14 to N0	programmable divider bits; $N = N14 \times 2^{14} + N13 \times 2^{13} + ... + N1 \times 2^{1} + N0$
CHP	charge pump current bit: CHP = 0; I_{CP} = 60 μA CHP = 1; I_{CP} = 280 μA (default)
T2, T1 and T0	test bits (see Table 5)
RSA and RSB	reference divider ratio select bits (see Table 6)
OS	tuning amplifier control bit: OS = 0; normal operation; tuning voltage is ‘ON’ OS = 1; tuning voltage is ‘OFF’ (high-impedance)
UHF, VHFH and VHFL	PNP ports control bits: bit = 0; buffer n is ‘OFF’ (default) bit = 1; buffer n is ‘ON’
X	don’t care bit: may be a logic 0 or a logic 1

Table 4 Address selection I^2C-bus

MA1	MA0	VOLTAGE APPLIED ON AS INPUT
0	0	0 to $0.1V_{CC}$
0	1	open or $0.2V_{CC}$ to $0.3V_{CC}$
1	0	$0.4V_{CC}$ to $0.6V_{CC}$
1	1	$0.9V_{CC}$ to $1.0V_{CC}$

Table 5 Test mode

T2	T1	T0	TEST MODES
0	0	0	automatic charge pump off
0	0	1	automatic charge pump on; note 1
0	1	X	charge pump is 'OFF'
1	1	0	charge pump is sinking current
1	1	1	charge pump is sourcing current
1	0	0	f_{REF} is available on pin ADC; note 2
1	0	1	$\frac{1}{2}f_{DIV}$ is available on pin ADC; note 2

Notes

1. This is the default mode at Power-on reset.
2. The ADC input cannot be used when these test modes are active.

Table 6 Reference divider ratio select bits

RSA	RSB	REFERENCE DIVIDER RATIO	FREQUENCY STEP (kHz)
X	0	640	6.25
0	1	1024	3.90625
1	1	512	7.8125

Read mode

Data can be read from the devices by setting the R/$\overline{W}$ bit to logic 1 (see Tables 7 and 8). After the slave address has been recognized, the devices generate an acknowledge pulse and the first data byte (status byte) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a HIGH-level of the SCL clock signal. A second data byte can be read from the devices if the processor generates an acknowledge on the SDA line (master acknowledge). End of transmission will occur if no master acknowledge occurs. The devices will then release the data line to allow the processor to generate a STOP condition. The POR flag is set to logic 1 at power-on. The flag is reset when an end-of-data is detected by the devices (end of a read sequence). Control of the loop is made possible with the in-lock flag FL which indicates when the loop is locked (FL = 1).

The ACPS flag is LOW when the automatic charge pump switch mode is 'ON' and the loop is locked. In other conditions, ACPS = 1. When ACPS = 0, the charge pump current is forced to the LOW value.

A built-in ADC is available on ADC pin. This converter can be used to apply AFC information to the controller from the IF section of the television. The relationship between the bits A2, A1 and A0 is given in Table 9.

Table 7 Read data format

NAME	BYTE	BITS								ACK
		MSB(1)							LSB	
Address byte	ADB	1	1	0	0	0	MA1	MA0	R/$\overline{W}$ = 1	A
Status byte	SB	POR	FL	ACPS	1	1	A2	A1	A0	–

Note

1. MSB is transmitted first.

Table 8 Description of symbols used in Table 7

SYMBOL	DESCRIPTION
A	acknowledge
POR	Power-on reset flag (POR = 1 at power-on)
FL	in-lock flag (FL = 1 when the loop is locked)
ACPS	automatic charge pump switch flag: ACPS = 0; active ACPS = 1; not active
A2, A1 and A0	digital outputs of the 5-level ADC (see Table 9)

Table 9 Analog-to-digital converter levels; note 1

A2	A1	A0	VOLTAGE APPLIED ON ADC INPUT
1	0	0	$0.60V_{CC}$ to $1.00V_{CC}$
0	1	1	$0.45V_{CC}$ to $0.60V_{CC}$
0	1	0	$0.30V_{CC}$ to $0.45V_{CC}$
0	0	1	$0.15V_{CC}$ to $0.30V_{CC}$
0	0	0	0 to $0.15V_{CC}$

Note

1. Accuracy is $\pm 0.03V_{CC}$.

Power-on reset

The power-on detection threshold voltage V_{POR} is set to V_{CC} = 2 V at room temperature. Below this threshold, the device is reset to the power-on state.

At power-on state, the charge pump current is set to 280 μA, the tuning voltage output is disabled, the test bits T2, T1 and T0 are set to logic 001 (automatic charge pump switch ‘ON’) and RSB is set to logic 1.

PUHF is ‘OFF’, which means that the UHF oscillator and the UHF mixer are switched off. Consequently, the VHF oscillator and the VHF mixer are switched on. PVHFL and PVHFH are ‘OFF’, which means that the VHF tank circuit is working in the VHF I sub-band. The tuning amplifier is switched off until the first transmission. In that case, the tank circuit in VHF I is supplied with the maximum tuning voltage. The oscillator is therefore working at the end of the VHF I sub-band.

Table 10 Default bits at Power-on reset

NAME	BYTE	BITS							
		MSB							LSB
Address byte	ADB	1	1	0	0	0	MA1	MA0	X
Divider byte 1	DB1	0	X	X	X	X	X	X	X
Divider byte 2	DB2	X	X	X	X	X	X	X	X
Control byte	CB	1	1	0	0	1	X	1	0
Band-switch byte	BB	X	X	X	X	0	0	0	0

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134) (note 1).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.3	+6	V
$V_{O(n)}$	output voltage on pins PVHFL, PVHFH and PUHF	–0.3	+6	V
$I_{O(n)}$	output current on pins PVHFL, PVHFH and PUHF	–1	+30	mA
$V_{O(CP)}$)	charge pump output voltage	–0.3	+6	V
$V_{O(VT)}$	tuning output voltage	–0.3	+35	V
$V_{I/O(ADC)}$	ADC input/output voltage	–0.3	+6	V
$V_{I(SCL)}$	serial clock input voltage	–0.3	+6	V
$V_{I/O(SDA)}$	serial data input/output voltage	–0.3	+6	V
$I_{O(SDA)}$	data output current	–1	+10	mA
$V_{I(AS)}$	address selection input voltage	–0.3	+6	V
$V_{I(XTAL)}$	crystal oscillator input voltage	–0.3	+6	V
$I_{O(n)}$	output current of each pin to ground:			
	for TDA6404, pins 1 to 6 and 17 to 28	–	–10	mA
	for TDA6405 and TDA6405A, pins 1 to 12 and 23 to 28	–	–10	mA
$t_{sc(max)}$	maximum short-circuit time (all pins to V_{CC} and all pins to GND, RFGND)	–	10	s
T_{stg}	IC storage temperature	–40	+150	°C
T_{amb}	operating ambient temperature	–20	+85	°C
T_j	junction temperature	–	150	°C

Note

1. Maximum ratings can not be exceeded, not even momentarily without causing irreversible IC damage. Maximum ratings can not be accumulated.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	85	K/W

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (T_{amb} = 25 °C)						
V_{CC}	supply voltage		4.5	5	5.5	V
I_{CC}	supply current at V_{CC} = 5 V	all PNP ports are 'OFF'	–	78	86	mA
		one PNP port is 'ON', sourcing 25 mA	–	110	121	mA
PLL Synthesizer part (V_{CC} = 4.5 to 5.5 V; T_{amb} = −20 to +85 °C; unless otherwise specified)						
FUNCTIONAL RANGE						
V_{POR}	Power-on reset voltage	below this supply voltage Power-on reset becomes active; see Table 10	1.5	2.0	–	V
D/D	divider ratio	15-bit frequency word	256	–	32767	
f_{XTAL}	crystal oscillator frequency	R_{XTAL} = 25 to 150 Ω	3.2	4	4.48	MHz
$\lvert Z_{XTAL} \rvert$	input impedance	f_{XTAL} = 4 MHz	600	1200	–	Ω
PNP PORTS						
$I_{L(off)}$	leakage current	V_{CC} = 5.5 V; V_{PNPn} = 0	−10	–	–	µA
$V_{O(sat)}$	output saturation voltage	one PNP port is 'ON', sourcing 25 mA; $V_{PNPn(sat)} = V_{CC} - V_{PNPn}$	–	0.25	0.4	V
ADC INPUT						
V_I	ADC input voltage	see Table 9	0	–	V_{CC}	V
I_{IH}	HIGH-level input current	$V_{ADC} = V_{CC}$	–	–	10	µA
I_{IL}	LOW-level input current	V_{ADC} = 0	−10	–	–	µA
ADDRESS SELECTION INPUT (AS)						
V_{IL}	LOW-level input voltage		0	–	1.5	V
V_{IH}	HIGH-level input voltage		3	–	5.5	V
I_{IH}	HIGH-level input current	V_{AS} = 5.5 V	–	–	10	µA
I_{IL}	LOW-level input current	V_{AS} = 0	−10	–	–	µA
SCL AND SDA INPUTS						
V_{IL}	LOW-level input voltage		0	–	1.5	V
V_{IH}	HIGH-level input voltage		3.0	–	5.5	V
I_{IH}	HIGH-level input current	V_{bus} = 5.5 V; V_{CC} = 0	–	–	10	µA
		V_{bus} = 5.5 V; V_{CC} = 5.5 V	–	–	10	µA
I_{IL}	LOW-level input current	V_{bus} = 1.5 V; V_{CC} = 0	–	–	10	µA
		V_{bus} = 0; V_{CC} = 5.5 V	−10	–	–	µA
f_{SCL}	serial clock frequency		–	100	150	kHz
SDA OUTPUT						
I_L	leakage current	V_{SDA} = 5.5 V	–	–	10	µA
V_O	output voltage	I_{SDA} = 3 mA (sink current)	–	–	0.4	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CHARGE PUMP OUTPUT (CP)						
$\|I_{IH}\|$	HIGH-level input current	CHP = 1	–	280	–	μA
$\|I_{IL}\|$	LOW-level input current	CHP = 0	–	60	–	μA
V_O	output voltage	PLL is locked; T_{amb} = 25 °C	–	1.95	–	V
$I_{L(off)}$	off-state leakage current	T2 = 0; T1 = 1	–15	–0.5	+15	nA
TUNING VOLTAGE OUTPUT (VT)						
$I_{L(off)}$	off-state leakage current	OS = 1; tuning supply = 33 V	–	–	10	μA
V_O	output voltage when the loop is closed	OS = 0; T2 = 0; T1 = 0; T0 = 1; R_L = 27 kΩ; tuning supply = 33 V	0.2	–	32.7	V
Mixer/oscillator part (V_{CC} = 5 V; T_{amb} = 25 °C; unless otherwise specified); measured in Fig.11						
IF AMPLIFIER						
S_{22}	output reflection coefficient	magnitude at 36.15 MHz; Z_o = 50 Ω	–	–12.5	–	dB
		phase at 36.15 MHz; Z_o = 50 Ω	–	1.41	–	deg
R_s	real part of $Z_o = R_s + j\omega L_s$	R_s at 36.15 MHz	–	81	–	Ω
L_s	imaginary part of $Z_o = R_s + j\omega L_s$	L_s at 36.15 MHz	–	9.5	–	nH
VHF MIXER (INCLUDING IF AMPLIFIER)						
$f_{i(RF)}$	RF input frequency	picture carrier frequency	45.25	–	399.25	MHz
F	noise figure	f_{RF} = 50 MHz; see Figs 8 and 9	–	7	9	dB
		f_{RF} = 150 MHz; see Figs 8 and 9	–	8	10	dB
		f_{RF} = 300 MHz;	–	9	11	dB
g_{os}	optimum source conductance for noise figure	f_{RF} = 50 MHz	–	0.7	–	mS
		f_{RF} = 150 MHz	–	0.9	–	mS
		f_{RF} = 300 MHz	–	1.5	–	mS
g_i	input conductance	f_{RF} = 45.25 MHz	–	0.25	–	mS
		f_{RF} = 399.25 MHz	–	0.5	–	mS
C_i	input capacitance	f_{RF} = 45.25 to 399.25 MHz	–	2	–	pF
V_o	output voltage causing 1% cross modulation in channel	f_{RF} = 45.25 MHz; see Fig.6	116	119	–	dBμV
		f_{RF} = 399.25 MHz; see Fig.6	116	119	–	dBμV
V_i	input voltage causing pulling in channel (750 Hz)	f_{RF} = 399.25 MHz; note 1	–	88	–	dBμV
G_V	voltage gain	f_{RF} = 45.25 MHz; see Fig.4	24.5	27	29.5	dB
		f_{RF} = 399.25 MHz; see Fig.4	24.5	27	29.5	dB
VHF OSCILLATOR						
f_{osc}	oscillator frequency		84.15	–	438.15	MHz
$\Delta f_{osc(V)}$	oscillator frequency shift with supply voltage	ΔV_{CC} = 5%; worst case in the frequency range; note 2	–	100	200	kHz
		ΔV_{CC} = 10%; worst case in the frequency range; note 2	–	200	–	kHz

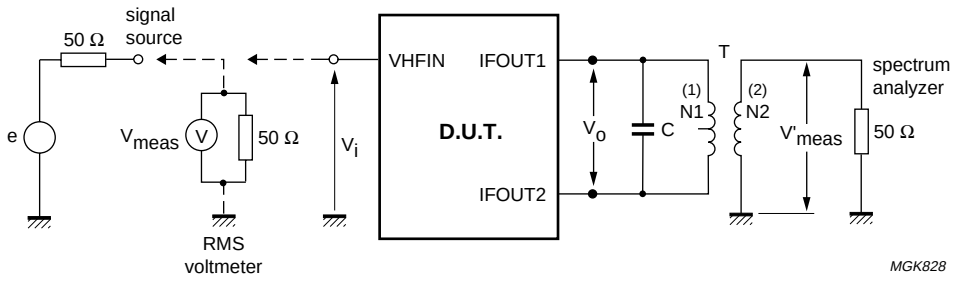
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\Delta f_{osc(T)}$	oscillator frequency drift with temperature	ΔT = 25 °C with compensation; worst case in the frequency range; note 3	–	1300	2000	kHz
$\Delta f_{osc(t)}$	oscillator frequency drift with time	with compensation; worst case in the frequency range; note 4	–	600	900	kHz
Φ_{osc}	phase noise, carrier to noise sideband	±100 kHz frequency offset; worst case in the frequency range	–	106	–	dBc/Hz
$RSC_{(p-p)}$	ripple susceptibility of V_{CC} (peak-to-peak value)	V_{CC} = 5 V; worst case in the frequency range; ripple frequency 500 kHz; note 5	15	40	–	mV
UHF MIXER (INCLUDING IF AMPLIFIER)						
$f_{i(RF)}$	RF input frequency	picture carrier frequency	407.25	–	855.25	MHz
F	noise figure	f_{RF} = 407.25 MHz; not corrected for image; see Fig.10	–	8	10	dB
		f_{RF} = 855.25 MHz; not corrected for image; see Fig.10	–	9	11	dB
R_s	real part of $Z_i = R_s + j\omega L_s$	f_{RF} = 407.25 MHz	–	30	–	Ω
		f_{RF} = 855.25 MHz	–	38	–	Ω
L_s	imaginary part of $Z_i = R_s + j\omega L_s$	f_{RF} = 407.25 MHz	–	9	–	nH
		f_{RF} = 855.25 MHz	–	6	–	nH
V_o	output voltage causing 1% cross modulation in channel	f_{RF} = 407.25 MHz; see Fig.7	116	119	–	dBµV
		f_{RF} = 855.25 MHz; see Fig.7	114	117	–	dBµV
V_i	input voltage causing pulling in channel (750 Hz)	f_{RF} = 855.25 MHz; note 1	–	78	–	dBµV
G_V	voltage gain	f_{RF} = 407.25 MHz; see Fig.5	35	38	41	dB
		f_{RF} = 855.25 MHz; see Fig.5	35	38	41	dB
UHF OSCILLATOR						
f_{osc}	oscillator frequency		446.15	–	894.15	MHz
$\Delta f_{osc(V)}$	oscillator frequency shift with supply voltage	ΔV_{CC} = 5%; worst case in the frequency range; note 2	–	30	80	kHz
		ΔV_{CC} = 10%; worst case in the frequency range; note 2	–	80	–	kHz
$\Delta f_{osc(T)}$	oscillator frequency drift with temperature	ΔT = 25 °C; with compensation; worst case in the frequency range; note 3	–	600	1000	kHz
$\Delta f_{osc(t)}$	oscillator frequency drift with time	with compensation; worst case in the frequency range; note 4	–	200	400	kHz
Φ_{osc}	phase noise, carrier to noise sideband	±100 kHz frequency offset; worst case in the frequency range	–	106	–	dBc/Hz
$RSC_{(p-p)}$	ripple susceptibility of V_{CC} (peak-to-peak value)	V_{CC} = 5 V; worst case in the frequency range; ripple frequency 500 kHz; note 5	15	20	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
REJECTION AT THE IF AMPLIFIER OUTPUT						
INT_{DIF}	level of divider interferences in the IF signal	note 6	–	20	–	dBμV
$INTR_{XTAL}$	crystal oscillator interferences rejection	note 7	60	–	–	dBc
$INTRF_{REF}$	reference frequency rejection	note 8	50	–	–	dBc
INT_{CHX}	channel x beat	note 9	60	–	–	dBc
INT_{S02}	S02 beat	note 10	66	–	–	dBc

Notes

1. This is the level of the RF signal (100% amplitude modulated with 11.89 kHz) that causes a 750 Hz frequency deviation on the oscillator signal; it produces sidebands 30 dB below the level of the oscillator signal.
2. The frequency shift is defined as the change of the oscillator frequency when the supply voltage varies from V_{CC} = 5 to 4.75 V (4.5 V) or from V_{CC} = 5 to 5.25 V (5.5 V). The oscillator is free-running during this measurement.
3. The frequency drift is defined as the change of the oscillator frequency when the ambient temperature varies from T_{amb} = 25 to 0 °C or from T_{amb} = 25 to 50 °C. The oscillator is free-running during this measurement.
4. The switching on drift is defined as the change of the oscillator frequency between 5 seconds and 15 minutes after switching on. The oscillator is free-running during this measurement.
5. The ripple susceptibility is measured for a 500 kHz ripple at the IF amplifier output using the measurement circuit; the level of the ripple signal is increased until a difference of 53.5 dB between the IF carrier set at 100 dBμV and the sideband components is reached.
6. This is the level of divider interferences close to the IF frequency. For example:
   Ch S1: f_{osc} = 144.15 MHz and $\frac{1}{4}f_{osc}$ = 36.0375 MHz.
   Ch S2: f_{osc} = 151.15 MHz and $\frac{1}{4}f_{osc}$ = 37.7875 MHz.
   Ch S14: f_{osc} = 291.15 MHz and $\frac{1}{8}f_{osc}$ = 36.39375 MHz.
   The VHF RF input must be left open (i.e. not connected to any load or cable).
   The UHF RF inputs are connected to a hybrid.
7. Crystal oscillator interference means the 4 MHz sidebands caused by the crystal oscillator.
   The rejection should be >60 dB for an IF output signal of 100 dBμV.
8. The reference frequency rejection is the level of reference frequency sidebands related to the sound subcarrier.
   The rejection should be >50 dB for an IF output signal of 100 dBμV, f_{REF} = 7.8125 kHz.
9. Channel x beat: picture carrier frequency (69.25 MHz) and sound carrier frequency (74.75 MHz) both at 80 dBμV, f_{osc} at 108.15 MHz. The rejection of the interfering product RF picture carrier frequency + RF sound carrier frequency – f_{osc} at 35.85 MHz should be >60 dB.
10. Channel S02: picture carrier frequency is 76.25 MHz at 80 dBμV, f_{osc} = 115.15 MHz.
    The rejection of $f_{osc} - 2 \times f_{IF}$ = 37.35 MHz should be >66 dB.

TEST AND APPLICATION INFORMATION



(1) N1 is 2×5 turns

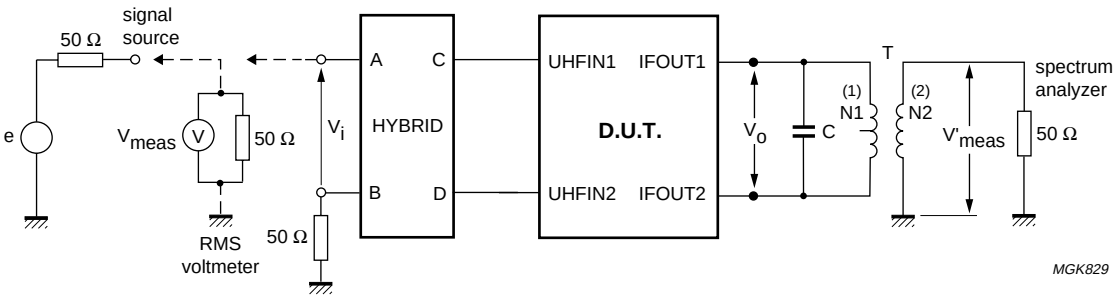
(2) N2 is 2 turns

$Z_i >> 50\ \Omega \Rightarrow V_i = 2 \times V_{meas}$; $V_i = 80\ dB\mu V$

$V_o = V'_{meas} + 16\ dB$ (transformer ratio $\frac{N1}{N2} = 5$ and transformer loss)

$G_v = 20 \log \frac{V_o}{V_i}$

Fig.4 Voltage gain (G_v) measurement in the VHF band.



(1) N1 is 2×5 turns

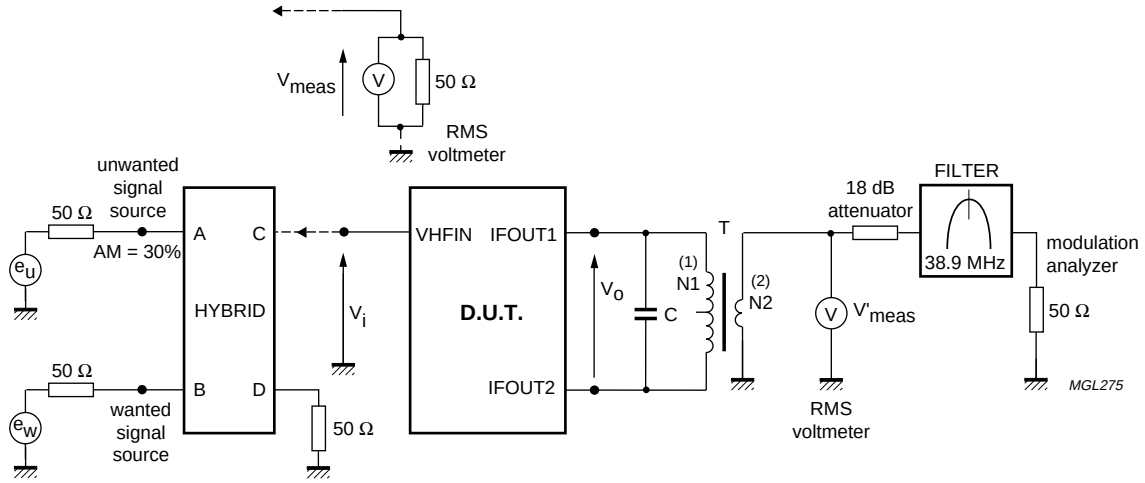
(2) N2 is 2 turns

$V_i = V_{meas}$; $V_i = 70\ dB\mu V$

$V_o = V'_{meas} + 16\ dB$ (transformer ratio $\frac{N1}{N2} = 5$ and transformer loss)

$G_v = 20 \log \frac{V_o}{V_i} + 1\ dB$ (1 dB = correction for hybrid loss)

Fig.5 Voltage gain (G_v) measurement in the UHF band.



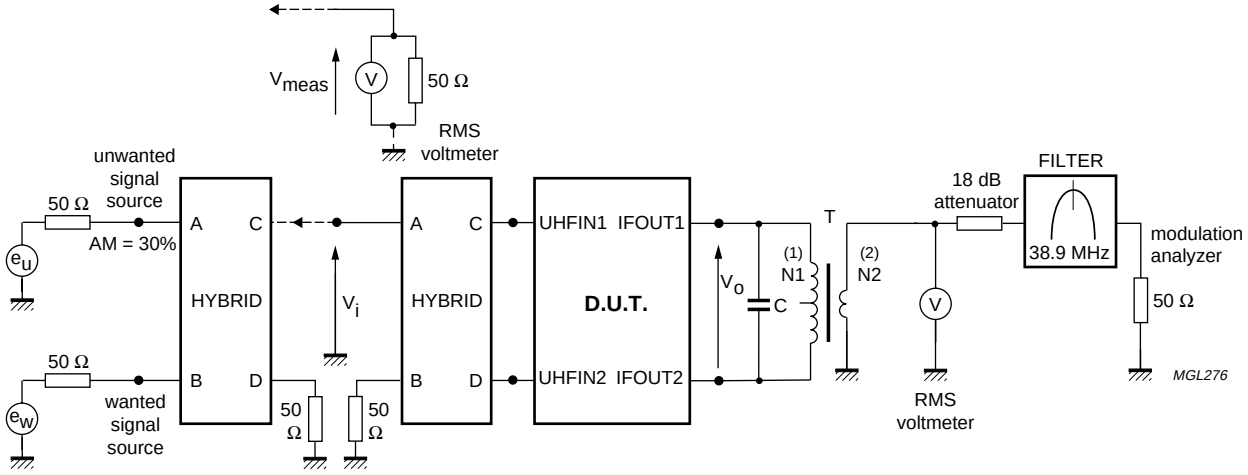
(1) N1 is 2×5 turns

(2) N2 is 2 turns

$Z_i >> 50\ \Omega \Rightarrow V_i = 2 \times V_{meas}$; $V'_{meas} = V_o - 16$ dB (transformer ratio $\frac{N1}{N2} = 5$ and transformer loss)

Wanted input signal V_i = 80 dBµV at wanted f_{RF} = 45.25 MHz (399.25 MHz).
Measured level of the unwanted output signal V_{ou} causing 0,3% AM modulation in the wanted output signal;
unwanted f_{RF} = 50.75 MHz (404.75 MHz); $V_{ou} = V'_{meas}$ + 16 dB.

Fig.6 Cross modulation measurement in the VHF band.



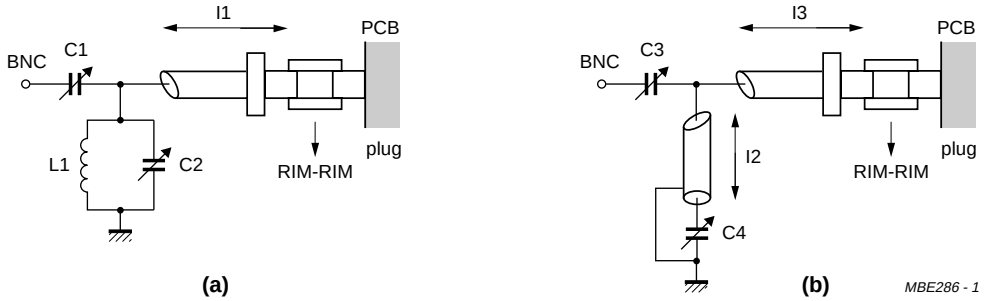
(1) N1 is 2×5 turns

(2) N2 is 2 turns

$V_i = V_{meas}$; $V'_{meas} = V_o - 16$ dB (transformer ratio $\frac{N1}{N2} = 5$ and transformer loss)

Wanted input signal V_i = 70 dBµV at f_{RF} = 407.25 MHz (855.25 MHz).
Measured level of the unwanted output signal V_{ou} causing 0,3% AM modulation in the wanted output signal;
unwanted f_{RF} = 412.75 MHz (860.75 MHz); $V_{ou} = V'_{meas}$ + 16 dB.

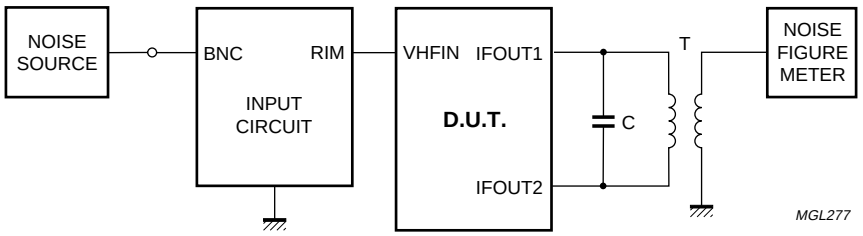
Fig.7 Cross modulation measurement in the UHF band.



(a) For f_{RF} = 50 MHz:
VHF mixer frequency response measured = 57 MHz;
loss = 0 dB.
Image suppression = 16 dB.
C1 = 9 pF; C2 = 15 pF.
L1 = 7 turns (Ø 5.5 mm; wire Ø = 0.5 mm).
I1 = semi rigid cable (RIM): 5 cm long.
(semi rigid cable (RIM); 33 dB/100 m; 50 Ω; 96 pF/m)·

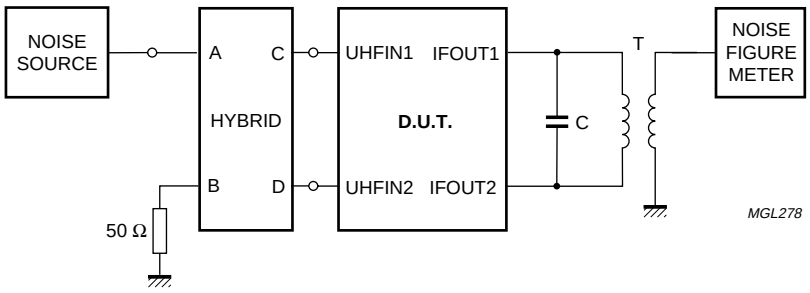
(b) For f_{RF} = 150 MHz:
VHF mixer frequency response measured = 150.3 MHz;
loss = 1.3 dB.
Image suppression = 13 dB.
C3 = 5 pF; C4 = 25 pF.
I2 = semi rigid cable (RIM): 30 cm long.
I3 = semi rigid cable (RIM): 5 cm long
(semi rigid cable (RIM); 33 dB/100 m; 50 Ω; 96 pF/m).

Fig.8 Input circuit for optimum noise figure in the VHF band.



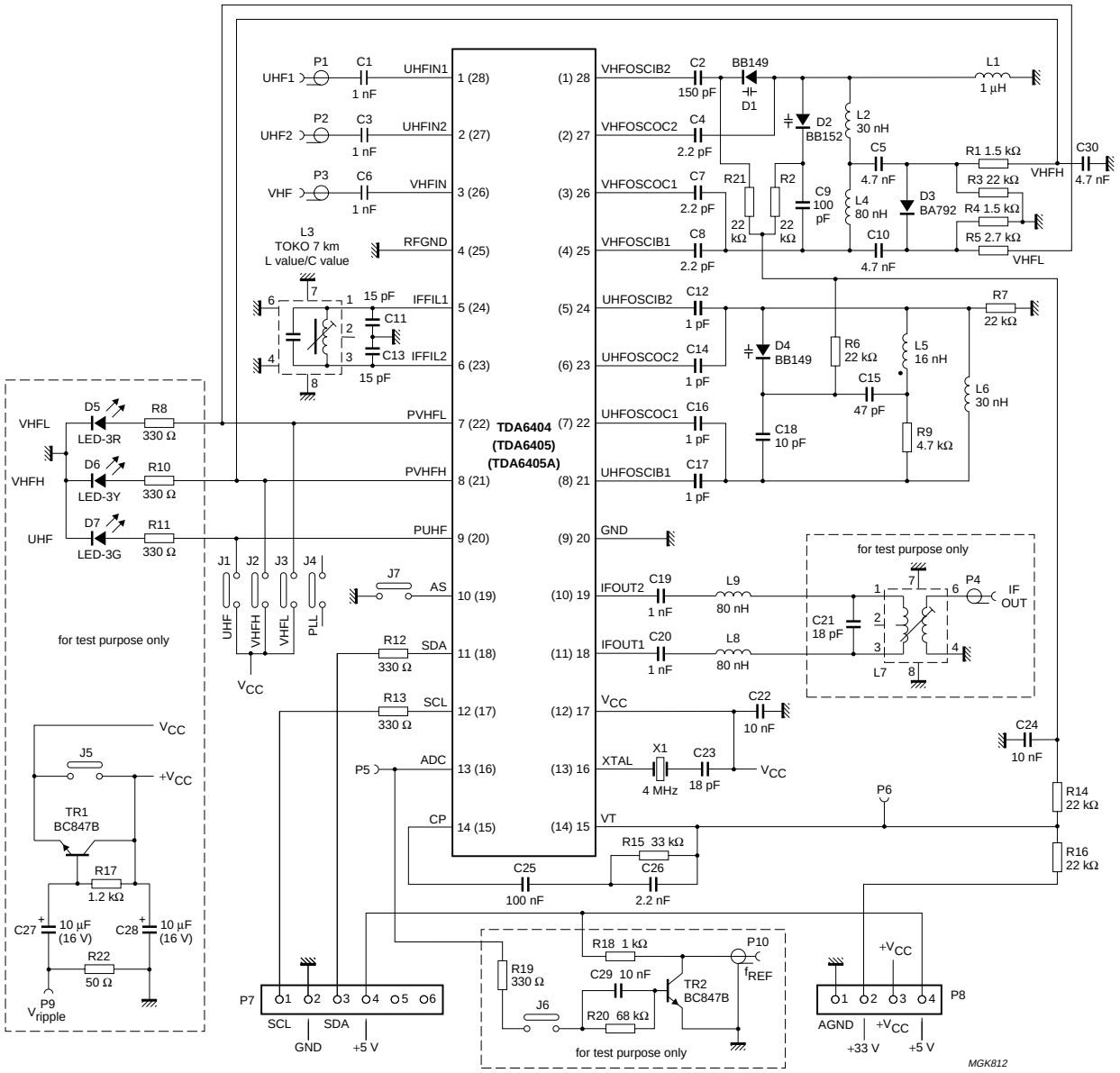
F = F_{meas} – loss (of input circuit) (dB).

Fig.9 Noise figure (F) measurement in the VHF band.



Loss (in hybrid) = 1 dB.
$F = F_{meas}$ – loss (in hybrid).

Fig.10 Noise figure (F) measurement in the UHF band.



The pin numbers in parenthesis represent the TDA6405 and TDA6405A.

Fig.11 Measurement circuit.

Component values for measurement circuit

Table 11 Capacitors (all SMD and NP0 unless otherwise specified)

COMPONENT	VALUE
C1	1 nF
C2	150 pF
C3	1 nF
C4	2.2 pF (N750)
C5	4.7 nF
C6	1 nF
C7	2.2 pF (N750)
C8	2.2 pF (N750)
C9	100 pF (N750)
C10	4.7 nF
C11	15 pF
C12	1 pF (N750)
C13	15 pF
C14	1 pF (N750)
C15	47 pF
C16	1 pF (N750)
C17	1 pF (N750)
C18	10 pF (N750)
C19	1 nF
C20	1 nF
C21	18 pF
C22	10 nF
C23	18 pF
C24	10 nF
C25	100 nF
C26	2.2 nF
C27	10 μF (16 V; electrolytic)
C28	10 μF (16 V; electrolytic)
C29	10 nF
C30	4.7 nF

Table 12 Resistors (all SMD)

COMPONENT	VALUE
R1	1.5 kΩ
R2	22 kΩ
R3	22 kΩ
R4	1.5 kΩ
R5	2.7 kΩ
R6	22 kΩ
R7	22 kΩ
R8	330 Ω
R9	4.7 kΩ
R10	330 Ω
R11	330 Ω
R12	330 Ω
R13	330 Ω
R14	22 kΩ
R15	33 kΩ
R16	22 kΩ
R17	1.2 kΩ
R18	1 kΩ
R19	330 Ω
R20	68 kΩ
R21	22 kΩ
R22	50 Ω

Table 13 Diodes and ICs

COMPONENT	VALUE
D1	BB149
D2	BB152
D3	BA792
D4	BB149
D5	LED-3R
D6	LED-3Y
D7	LED-3G
IC	TDA6404; TDA6405; TDA6405A

Table 14 Coils

COMPONENT	VALUE
L1	1 μH (inductor)
L2	30 nH
L4	80 nH
L5	16 nH
L6	30 nH
L8	80 nH
L9	80 nH

Table 15 Transformer

COMPONENT	VALUE
L3	23 turns (TOKO, wire 0.07 mm)
L7	N1 = 2 × 5 turns N2 = 2 turns (TOKO, wire 0.09 mm)

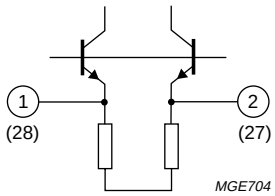
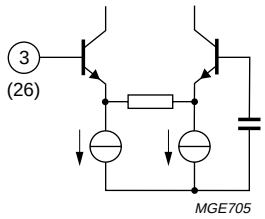
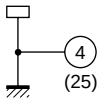
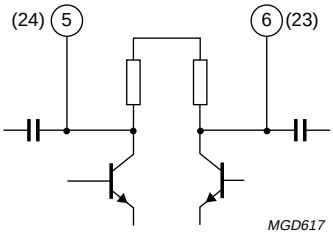
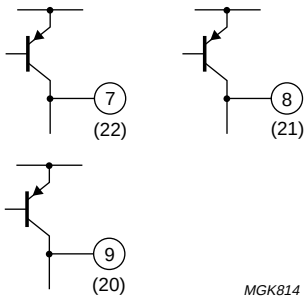
Table 16 Crystal

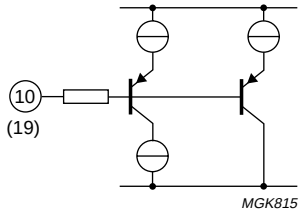
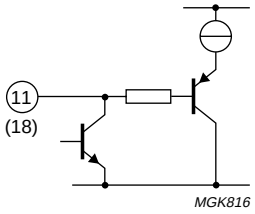
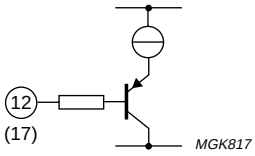
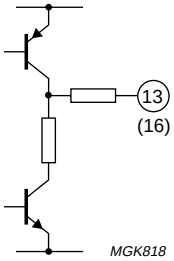
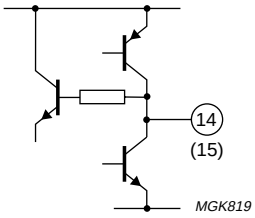
COMPONENT	VALUE
X1	4 MHz

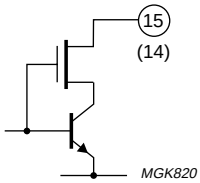
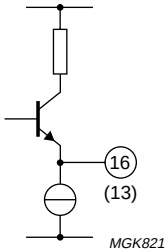
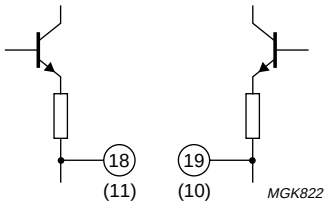
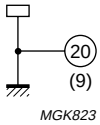
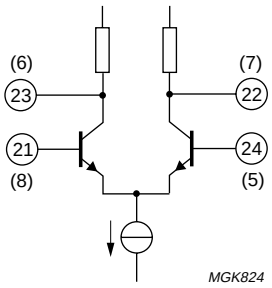
Table 17 Transistors

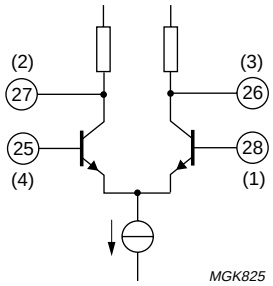
COMPONENT	VALUE
TR1	BC847B
TR2	BC847B

INTERNAL PIN CONFIGURATION

SYMBOL	PIN		CONFIGURATION(1)	AVERAGE DC VOLTAGE (V)	
	TDA6404	TDA6405: TDA6405A		VHF	UHF
UHFIN1	1	28		note 2	1.0
UHFIN2	2	27		note 2	1.0
VHFIN	3	26		1.9	note 2
RFGND	4	25		0.0	0.0
IFFIL1	5	24		3.4	3.4
IFFIL2	6	23		3.4	3.4
PVHFL	7	22		0.0 or ($V_{CC} - V_{CE}$)	0.0
PVHFH	8	21		($V_{CC} - V_{CE}$) or 0.0	0.0
PUHF	9	20		0.0	($V_{CC} - V_{CE}$)

SYMBOL	PIN		CONFIGURATION(1)	AVERAGE DC VOLTAGE (V)	
	TDA6404	TDA6405: TDA6405A		VHF	UHF
AS	10	19		V_{AS}	V_{AS}
SDA	11	18		note 2	note 2
SCL	12	17		note 2	note 2
ADC	13	16		1.9	1.9
CP	14	15		1.9	1.9

SYMBOL	PIN		CONFIGURATION(1)	AVERAGE DC VOLTAGE (V)	
	TDA6404	TDA6405: TDA6405A		VHF	UHF
VT	15	14		V_{VT}	V_{VT}
XTAL	16	13		3.0	3.0
V_{CC}	17	12	supply voltage	5.0	5.0
IFOUT1	18	11		2.2	2.2
IFOUT2	19	10		2.2	2.2
GND	20	9		0.0	0.0
UHFOSCIB1	21	8		note 2	1.9
UHFOSCOC1	22	7		note 2	2.5
UHFOSCOC2	23	6		note 2	2.5
UHFOSCIB2	24	5		note 2	1.9

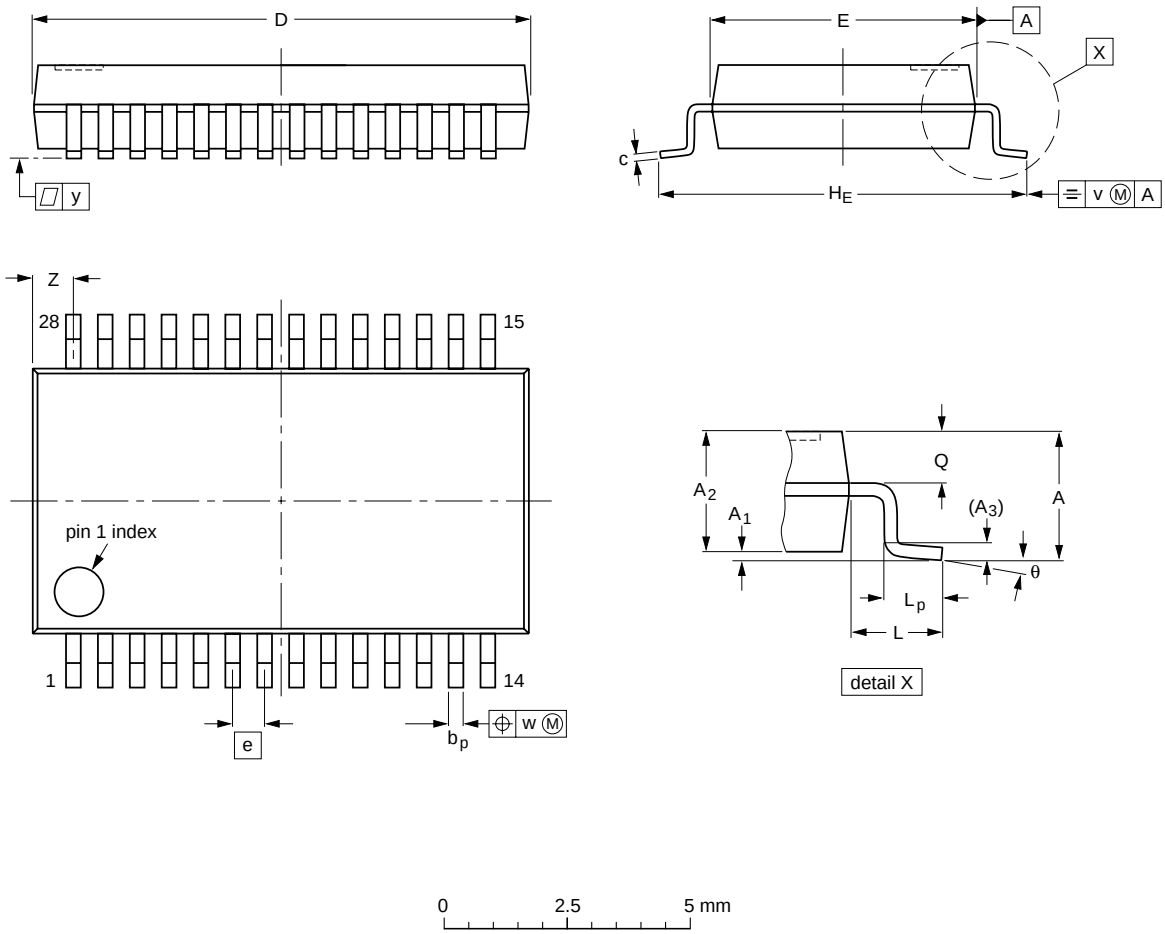
SYMBOL	PIN		CONFIGURATION(1)	AVERAGE DC VOLTAGE (V)	
	TDA6404	TDA6405: TDA6405A		VHF	UHF
VHFOSCIB1	25	4		2.0	note 2
VHFOSCOC1	26	3		2.7	note 2
VHFOSCOC2	27	2		2.7	note 2
VHFOSCIB2	28	1		2.0	note 2

Notes

1. The pin numbers in parenthesis represent the TDA6405 and TDA6405A.
2. Not applicable.

PACKAGE OUTLINE

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm **SOT341-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT341-1		MO-150AH				~~93-09-08~~ 95-02-04

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

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