

256-pixel CCD Linear Image Sensor (B/W)

Description

The ILX521A is a rectangular reduction type CCD linear image sensor designed for image scanner sensor. A built-in timing generator and clock driver ensure single 5V power supply for easy use.

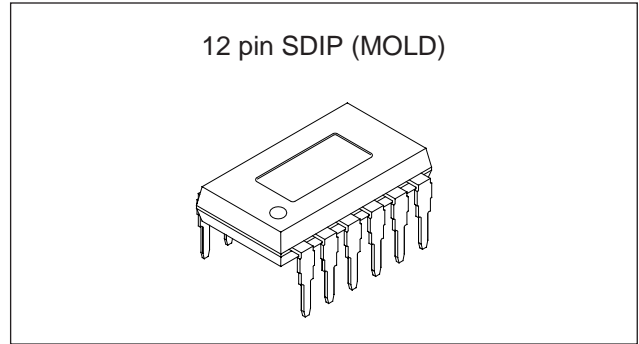
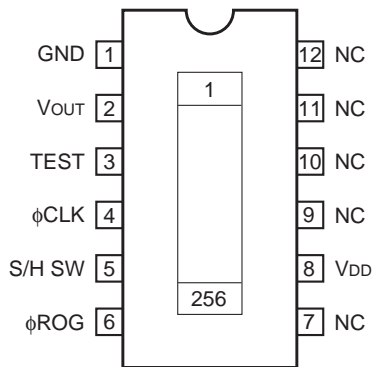
Features

- Number of effective pixels: 256 pixels
- Pixel size: 14µm × 14µm (14µm pitch)
- Built-in timing generator and clock driver
- Built-in S/H circuit
- Maximum data rate: 2MHz
- Single 5V power supply
- Clear mold package (12-pin SDIP)

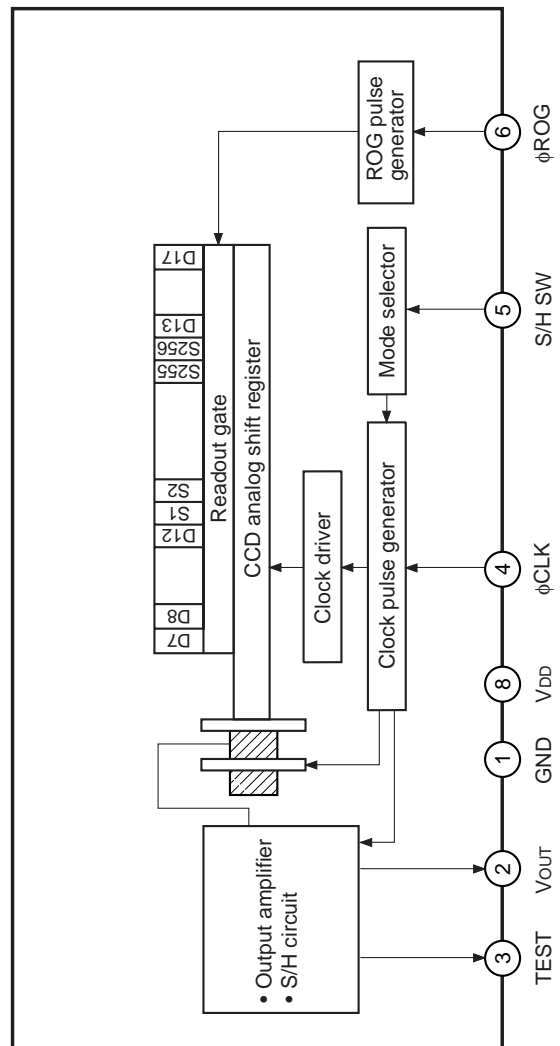
Absolute Maximum Ratings

- Supply voltage  $V_{DD}$  6 V
- Operating temperature -10 to +60 °C
- Storage temperature -30 to +80 °C

Pin Configuration (Top View)



Block Diagram



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**Pin Description**

Pin No.	Symbol	Description
1	GND	GND
2	V <sub>OUT</sub>	Signal output
3	TEST	Test (open)
4	φCLK	Clock pulse input
5	S/H SW	Switching of with S/H or without S/H
6	φROG	Readout gate pulse input
7	NC	NC
8	V <sub>DD</sub>	5V power supply
9	NC	NC
10	NC	NC
11	NC	NC
12	NC	NC

**Recommended Voltage**

Item	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	4.75	5.0	5.25	V

**Mode Description**

Used mode	Pin 5 S/H SW
with S/H	GND
without S/H	V <sub>DD</sub>

**Input Clock Voltage Condition\*1**

Item	Symbol	Min.	Typ.	Max.	Unit
High level	V <sub>IH</sub>	4.5	V <sub>DD</sub>	V <sub>DD</sub> + 0.5	V
Low level	V <sub>IL</sub>	0	—	0.5	V

\*1 This is applied to the all external pulses. (φCLK, φROG)

**Input Pin Capacity**

Item	Symbol	Min.	Typ.	Max.	Unit
Input capacity of φCLK pin	C <sub>φCLK</sub>	—	10	—	pF
Input capacity of φROG pin	C <sub>φROG</sub>	—	10	—	pF

**Electrooptical Characteristics**

(Ta = 25°C, VDD = 5V, Data rate = 1MHz, Without S/H mode, Light source = 3200K, IR cut filter CM-500S (t = 1mm))

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Sensitivity	R	13.3	19.0	24.7	V/(lx · s)	Note 1
Sensitivity nonuniformity	PRNU	—	5.0	12.0	%	Note 2
Saturation output voltage	VSAT	0.6	0.8	—	V	—
Dark voltage average	VDRK	—	0.3	2.0	mV	Note 3
Dark signal nonuniformity	DSNU	—	0.5	3.0	mV	Note 3
Image lag	IL	—	0.02	—	%	Note 4
Dynamic range	DR	—	2666	—		Note 5
Saturation exposure	SE	—	0.042	—	lx · s	Note 6
Current consumption	IVDD	—	5.0	10.0	mA	—
Total transfer efficiency	TTE	92.0	98.0	—	%	—
Output impedance	Zo	—	350	—	Ω	—
Offset level	Vos	—	3.8	—	V	Note 7

**Note)**

1. For the sensitivity test light is applied with a uniform intensity of illumination.
2. PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 1.

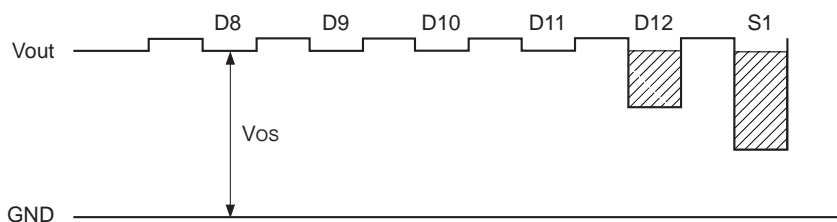
$$PRNU = \frac{(V_{MAX} - V_{MIN})/2}{V_{AVE}} \times 100 [\%]$$

The maximum output of the 256 pixels is set to V<sub>MAX</sub>, the minimum output to V<sub>MIN</sub> and the average output to V<sub>AVE</sub>.

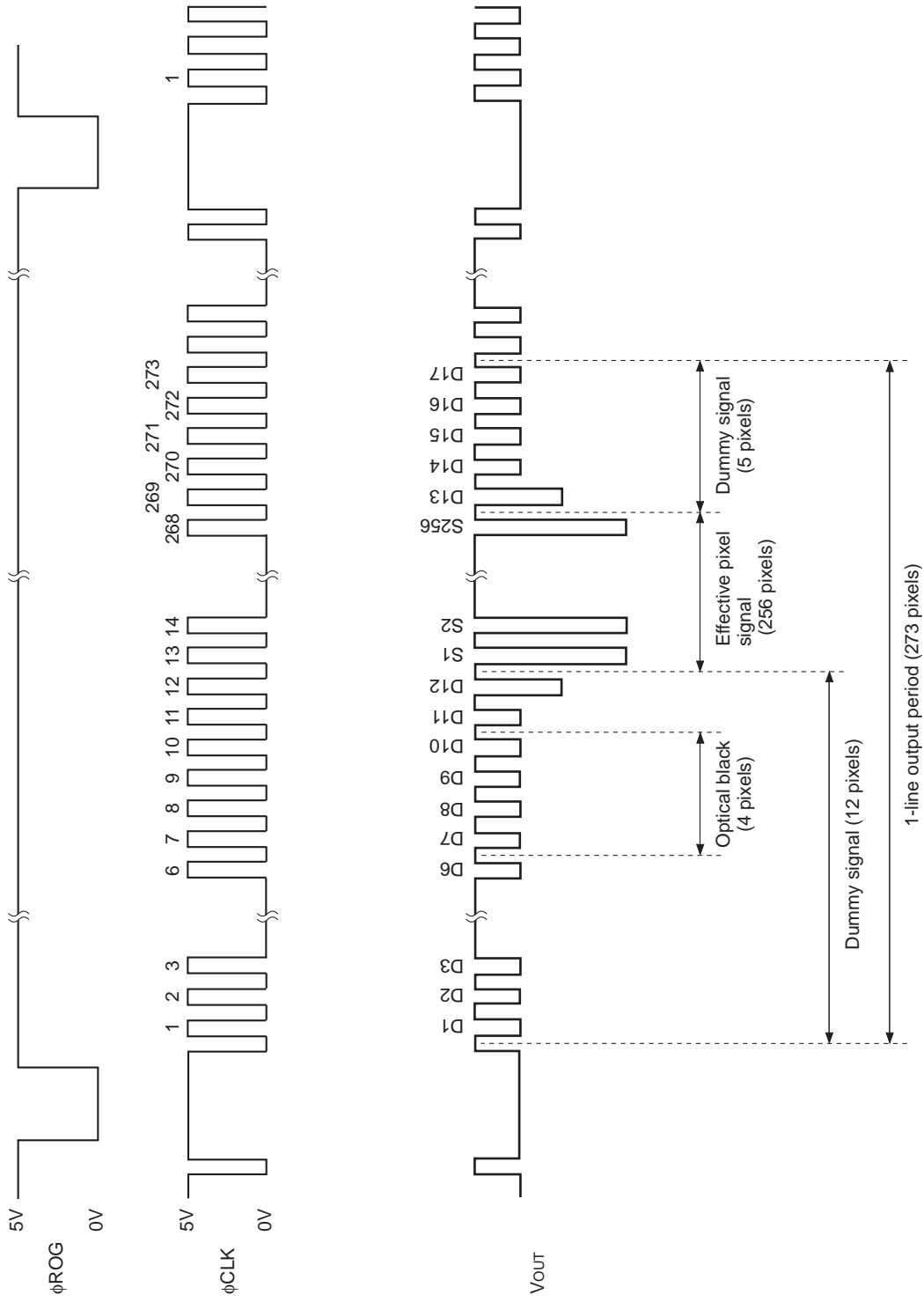
3. Integration time is 10ms.
4. V<sub>OUT</sub> = 500mV.
5. DR = VSAT/VDRK

When optical integration time is shorter, the dynamic range sets wider because dark output voltage is in proportion to optical integration time.

6. SE = VSAT/R1
7. Vos is defined as indicated below.

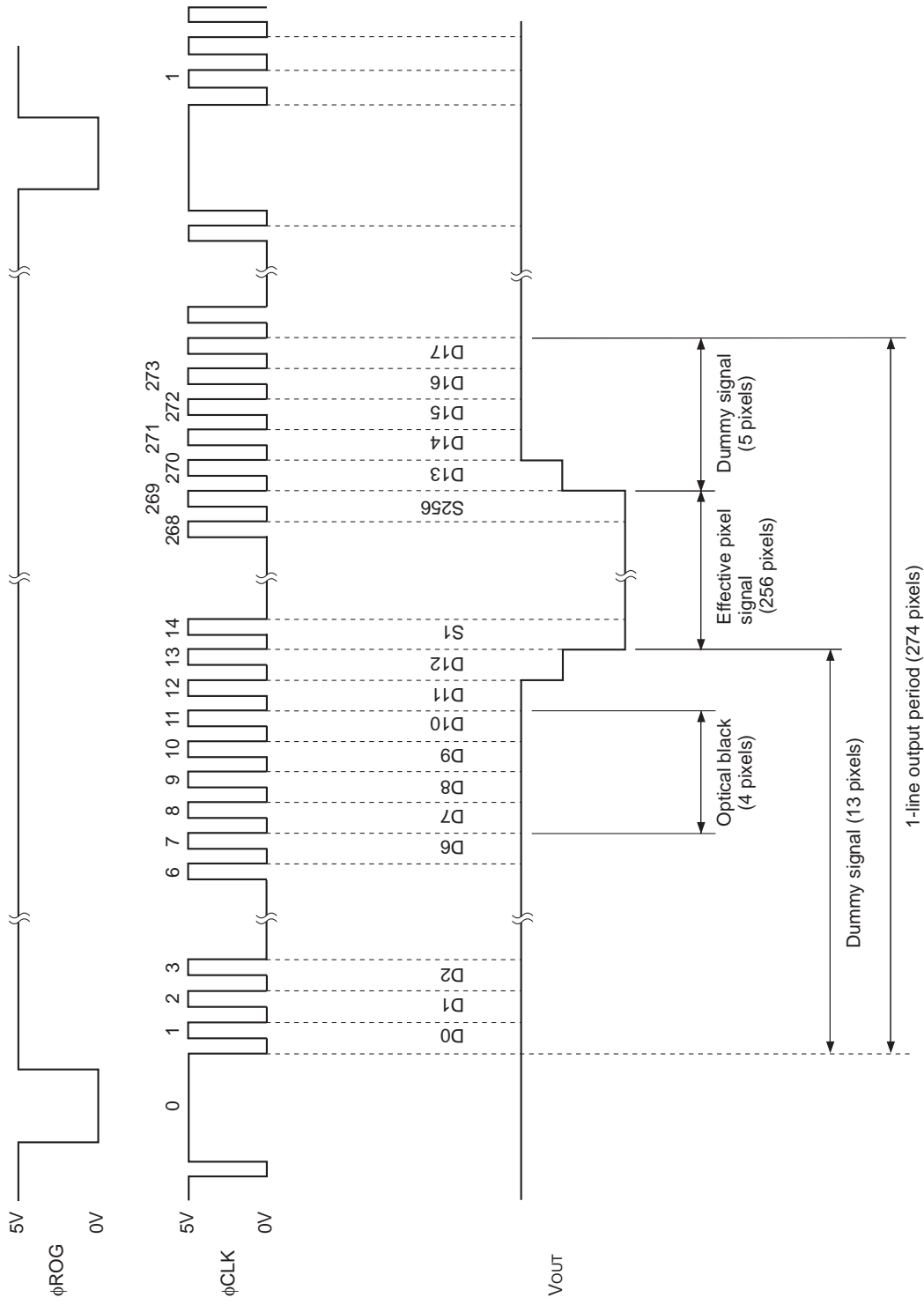


**Clock Timing Diagram (without internal S/H mode)**



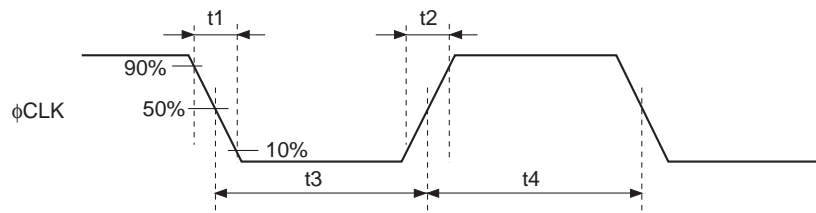
Note) 280 or more clock pulses are required.

**Clock Timing Diagram (with internal S/H mode)**



Note) 280 or more clock pulses are required.

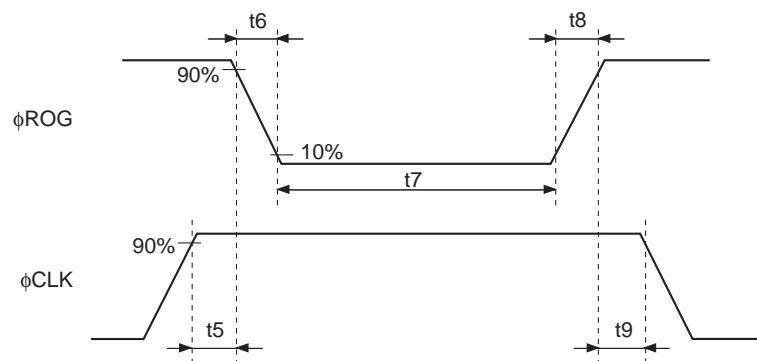
$\phi$ CLK Timing (For all modes)



Item	Symbol	Min.	Typ.	Max.	Unit
$\phi$ CLK pulse rise/fall time	t1, t2	0	10	100	ns
$\phi$ CLK pulse Duty*1	—	40	50	60	%

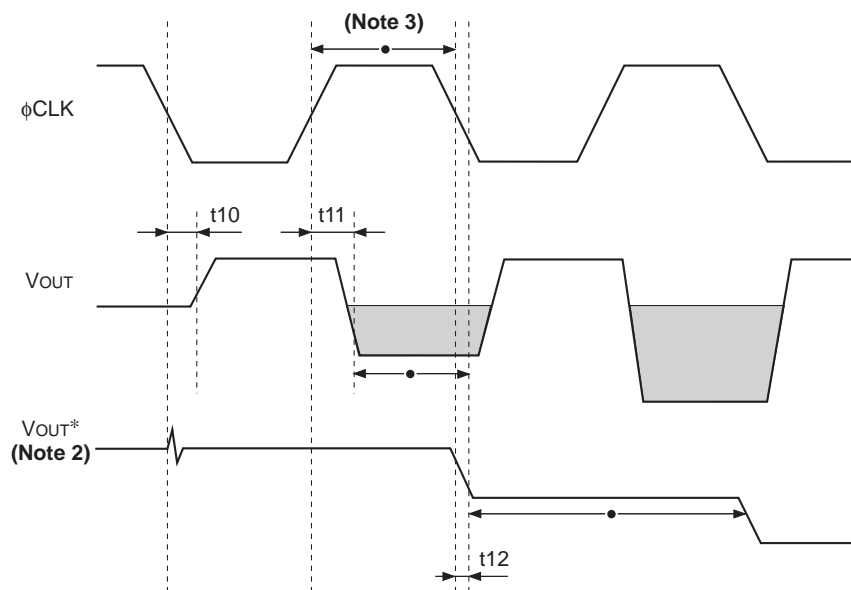
\*1  $100 \times t4 / (t3 + t4)$

$\phi$ ROG,  $\phi$ CLK Timing



Item	Symbol	Min.	Typ.	Max.	Unit
$\phi$ ROG, $\phi$ CLK pulse timing 1	t5	500	1000	—	ns
$\phi$ ROG, $\phi$ CLK pulse timing 2	t9	500	1000	—	ns
$\phi$ ROG pulse rise/fall time	t6, t8	0	10	—	ns
$\phi$ ROG pulse period	t7	500	1000	—	ns

$\phi$ CLK Output Signal Timing (Note 1)



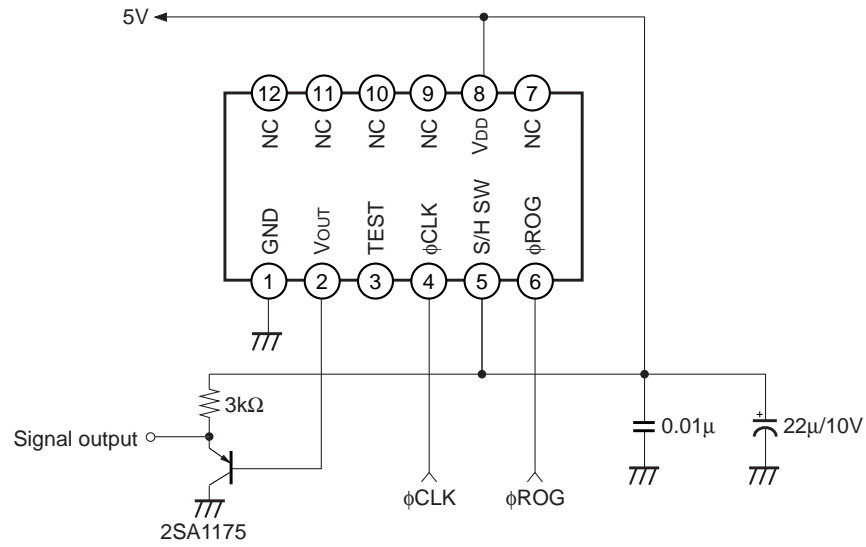
Item	Symbol	Min.	Typ.	Max.	Unit
$\phi$ CLK – $V_{OUT}$ output delay time 1	t10	—	150	—	ns
$\phi$ CLK – $V_{OUT}$ output delay time 2	t11	—	220	—	ns
$\phi$ CLK – $V_{OUT}^*$ (with S/H) output delay time	t12	—	110	—	ns

**Note 1)**  $f_{clk} = 1\text{MHz}$ ,  $\phi$ CLK pulse Duty = 50%,  $\phi$ CLK pulse rise/fall time = 10ns

**Note 2)** Output waveform when internal S/H circuit is used.

**Note 3)** • is data period.

Application Circuit (without internal S/H mode)

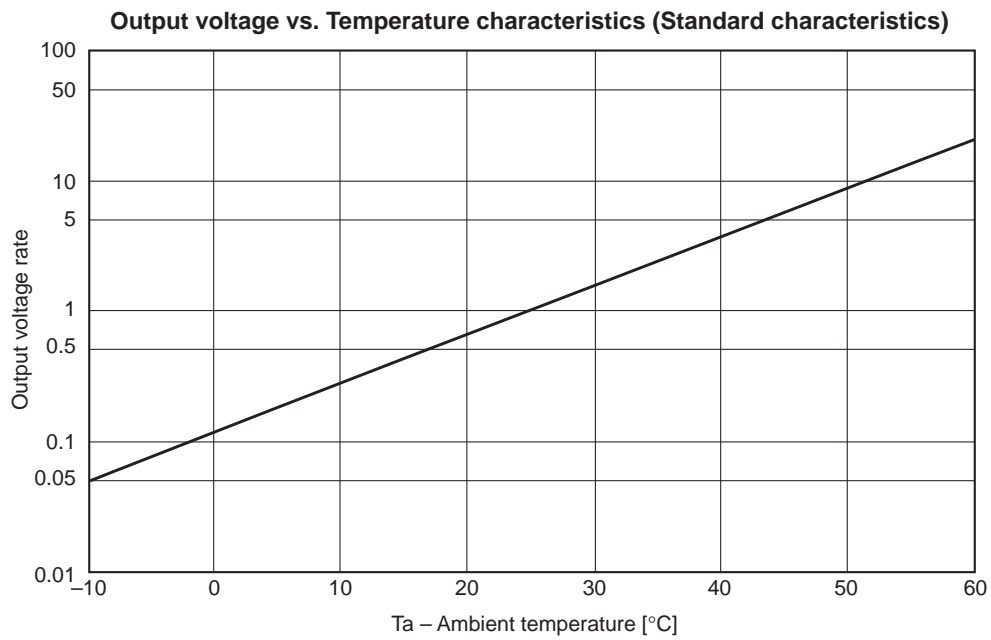
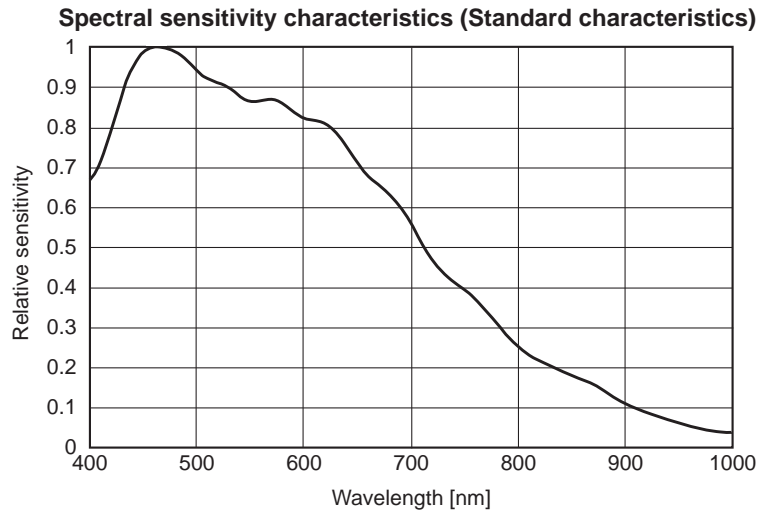


Note) This circuit diagram is the case when internal S/H mode is not used.  
Connect Pin 5 to GND when internal S/H mode is used.

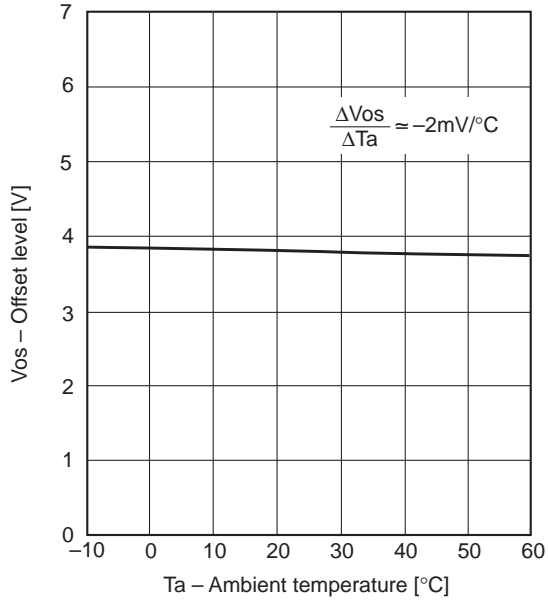
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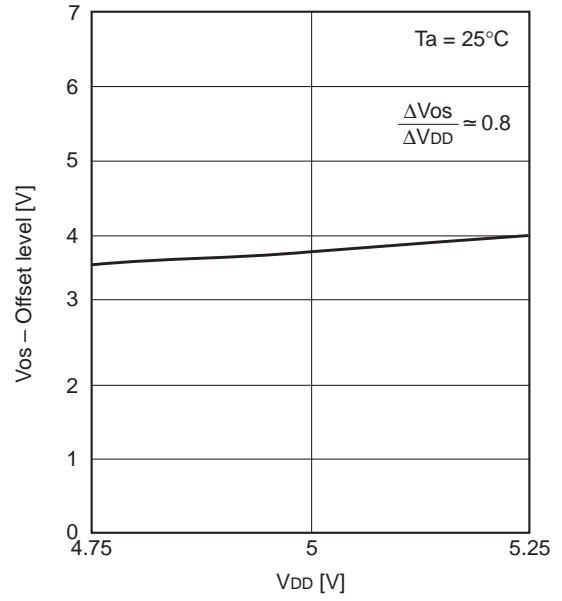
Example of Representative Characteristics



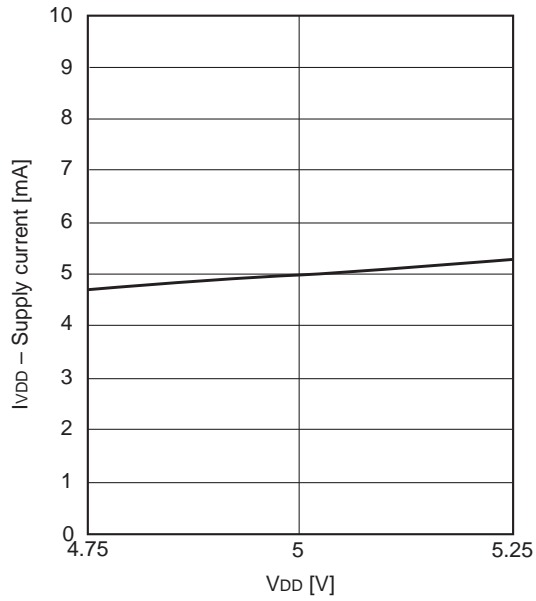
**Offset level vs. Temperature characteristics  
(Standard characteristics)**



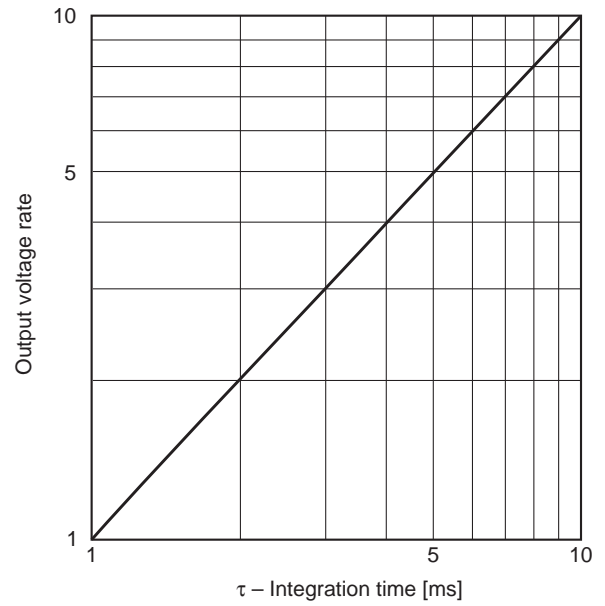
**Offset level vs. VDD characteristics  
(Standard characteristics)**



**Supply current vs. VDD characteristics  
(Standard characteristics)**



**Output voltage vs. Integration time  
(Standard characteristics)**



**Notes on Handling**

## 1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

- a) Either handle bare handed or use non-chargeable gloves, clothes or material. Also use conductive shoes.
- b) When handling directly use an earth band.
- c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
- d) Ionized air is recommended for discharge when handling CCD image sensors.
- e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

## 2) Soldering

- a) Make sure the package temperature does not exceed 80°C.
- b) Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
- c) To dismount an image sensor, do not use solder suction equipment. When using an electric desoldering tool, ground the controller. For the temperature control system, use a zero-cross type.

## 3) Dust and dirt protection

- a) Operate in clean environments.
- b) Do not either touch mirror surfaces by hand or have any object come in contact with mirror surfaces. Should dirt stick to a mirror surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
- c) Clean with a cotton bud and ethyl alcohol if the mirror surfaces are grease stained. Be careful not to scratch the mirror surfaces.
- d) Keep in a case to protect from dust and dirt. To prevent dew condensation on the mirror surfaces, preheat or precool when moving to a room with great temperature differences.

## 4) Do not expose to intense light for long periods.

## 5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

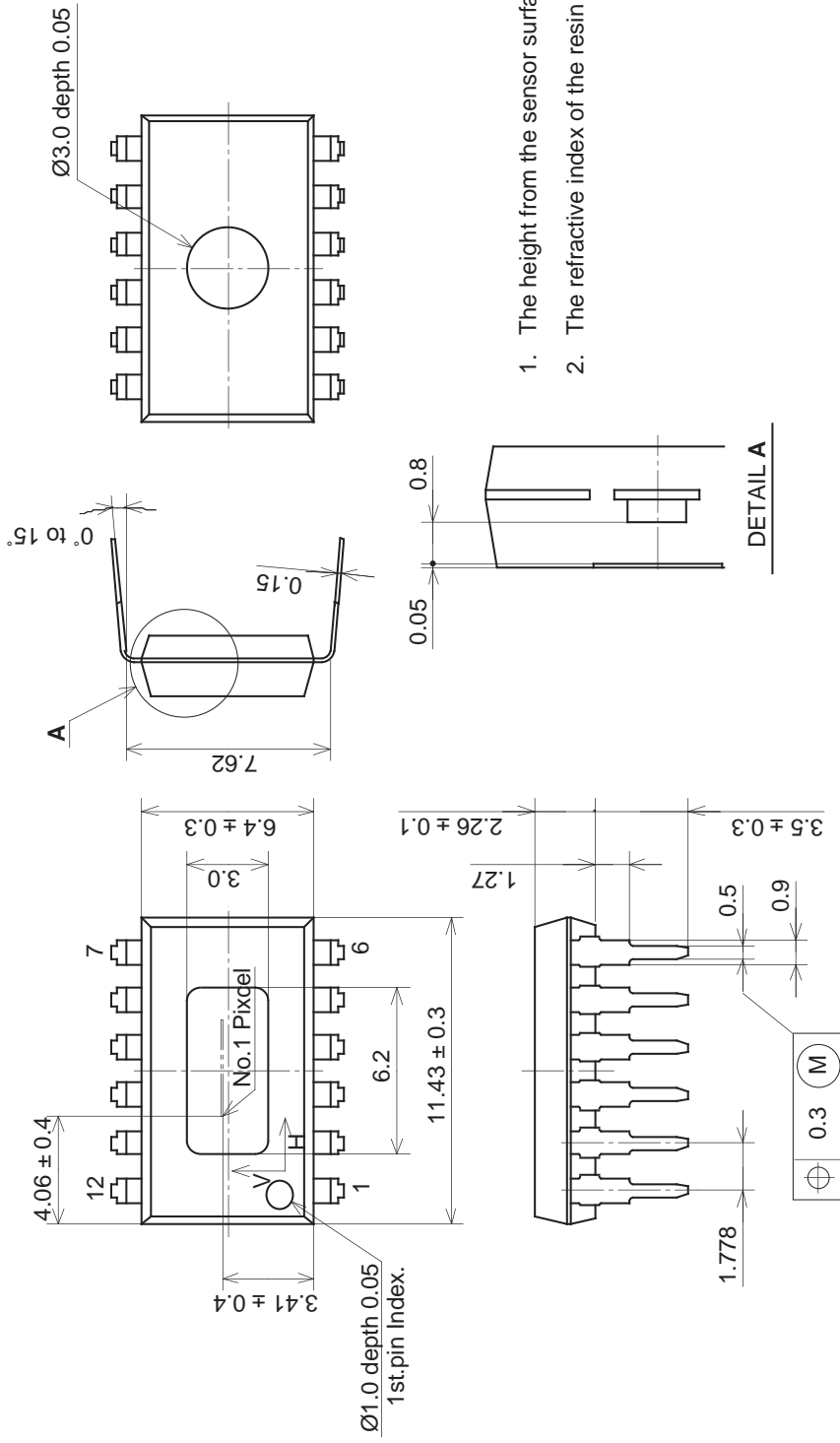
## 6) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

## 7) Normal output signal is not obtained immediately after device switch on.

Package Outline

Unit: mm

12pin DIP (300mil)



1. The height from the sensor surface is  $1.41 \pm 0.3$ mm.
2. The refractive index of the resin is 1.57.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Plastic
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42ALLOY
PACKAGE MASS	0.28g
DRAWING NUMBER	LS-F5(E)