VORTEX CHIP SET

S/UNI - DUPLEX™ PM7350

S/UNI - VORTEX™ PM7351

S/UNI - APEX™ PM7326

S/UNI - ATLAS™ PM7324

INTRODUCTION

PRELIMINARY INFORMATION

ISSUE 1: JULY 1999

REVISION HISTORY

Issue No.	Issue Date	Details of Change
1	July 1999	Document created.

CONTENTS

FIGURES

1 PURPOSE AND SCOPE OF THIS DOCUMENT

PMC-Sierra has introduced the Industry's first standard product chip set designed from the ground up to satisfy requirements of the newest and fastest growing network access applications:

- Digital Subscriber Line Access Multiplexers -- DSLAMs.
- Third generation digital wireless base stations and base station controllers.
- Multi-service access multiplexers.

This paper discusses how and why PMC-Sierra implemented a system level solution to satisfy the unique requirements of this marketplace. We first analyze the requirements driving Digital Subscriber Line Access Multiplexer (DSLAM) market and describe how the features of the VORTEX chip set meet these requirements. We then expand the discussion to include third generation CDMA wireless equipment (hereafter called 3G Wireless) and multi-service access platforms capable of supporting ATM, frame, and TDM interfaces.

2 VORTEX CHIP SET OVERVIEW

The VORTEX chip set is optimized for use in carrier grade, full-featured access equipment delivering high speed Internet and voice services to end customers. As shown in the following table, its feature set has been carefully crafted to minimize the entire life cycle cost of access platforms targeted to mass market service deployment.

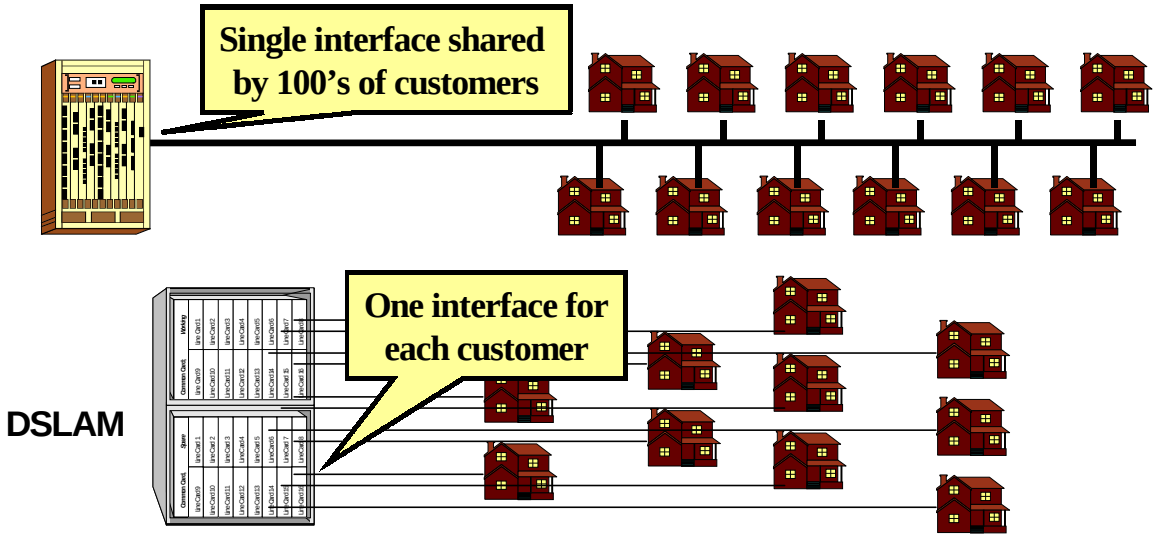
VORTEX chip set Feature	Impact on equipment life cycle
Centralized switching and traffic management for 2048 subscriber lines, eliminating the need for expensive and complex traffic management functions on the line card.	System hardware and software design is greatly simplified, thereby reducing development costs and speeding time to market.
Reduced system software complexity by eliminating the need for software intelligence on the line cards.	Future in-field upgrades of software and hardware will not impact the line cards (which are the most numerous cards in the system). This extends the system's lifetime and reduces ongoing maintenance costs.
Class of Service (CoS) differentiated traffic buffering and scheduling is implemented on each of the 2048 lines, and on the WAN up-link. Traffic shaping is implemented on the WAN up-link ports.	Service providers can offer differentiated services to address specific needs of distinct market segments. CoS processing is handled centrally, thereby ensuring fairness across all customers regardless of system size.
Low Voltage Differential Signal (LVDS) serial interconnect between the DSLAM subscriber line cards and the centralized switch card. In an architecture based on a parallel bus backplane the entire backplane can be taken out of service by a failure on one line card. With the serial point-to-point backplane implemented by the VORTEX chip set, failures on one line card do not impact other line cards.	Designing for fault tolerance is greatly simplified, reducing development costs and improving time to market. In-field operating costs are lowered due to improved reliability and simplified servicing that results from line card independence.
LVDS operates over the backplane or between shelves on twisted pair cabling, and is "hot-swap" capable. The physical location of the line card – whether it is on the same or a different shelf from the switching card -–is hidden from the traffic management device.	This architecture directly scales to large, multi-shelf systems without increasing the cost or complexity of the traffic management hardware and software. In-field expansion from single to multi-shelf configurations is directly supported with no impact on the system software.
Optional 1:1 redundancy of the common equipment.	Directly supports "carrier grade" reliability, greatly simplifying system design and reducing time to market. In-field upgrades from unprotected to 1:1 protected systems can be done without taking equipment out of service.

3 TAKING XDSL SERVICES TO THE MASS MARKET

Access services based on ADSL, SDSL, HDSL, and G.Lite have moved rapidly from trial to deployment. The current focus of many of these service offerings is the business customer, with deployment for residential customers to follow. However, to be successful in the higher volume, lower margin residential access services the service provider must be supported by network equipment capable of competitive mass market deployment.

In the residential market the main competition in the broadband Internet access market are cable modems. Where it is available, Internet access delivered over the cable television plant has often been priced lower -- sometimes significantly lower -- than xDSL based services. Price is almost always a significant factor in the mass market, and the shared nature of the cable plant reduces the electronic equipment dedicated to each customer. As shown in Figure 1, the cable head end equipment is fully shared across all subscribers, while the DSLAM must provide a dedicated line interface for each customer.

Figure 1 - Cable Modem Infrastructure compared to xDSL Infrastructure



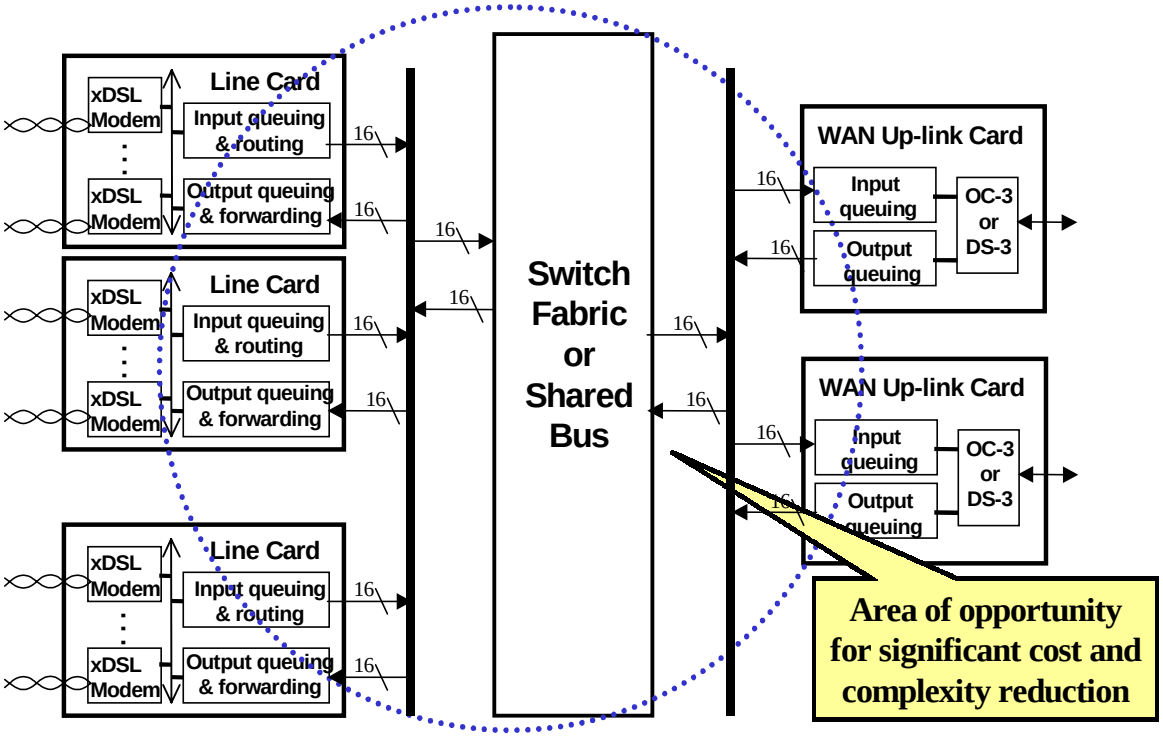
The shared cable can create traffic bottlenecks as high speed services grow in popularity. This is often cited as a key technical advantage of xDSL based services, but the reduced complexity at the head-end does create a cost advantage for cable modems in terms of the amount of electronics needed. However, this competitive advantage of cable modem based services is neutralized when the per-customer cost of the DSLAM is significantly reduced by deploying fully optimized DSLAM platforms.

Current DSLAM solutions such as shown in Figure 2 typically employ distributed traffic management and control functions that span the line cards and the central switch -- the same architecture used to implement traditional ATM access multiplexers and switches.

Traditional ATM core equipment is designed for a relatively small number of high speed ports and does not take advantage of the different traffic characteristics exhibited by lower speed xDSL ports versus higher speed optical ports.

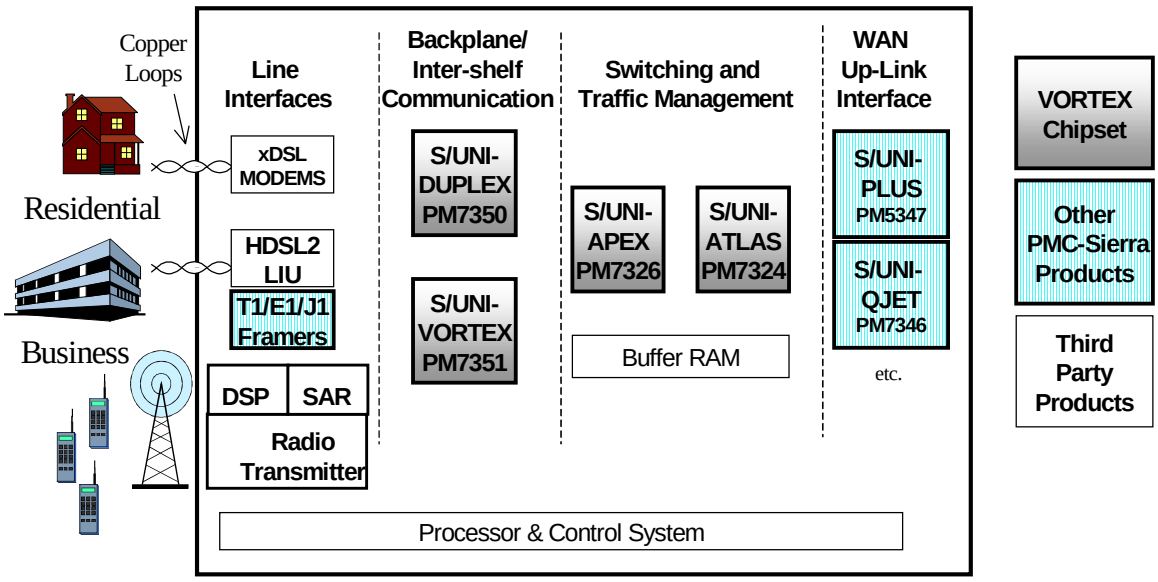
Since currently available traffic management devices typically support 32 ports, the traditional approach works well for implementing line cards with a few high speed ports (DS-3s and OC-3s). However, this approach is not optimal for terminating the numerous relatively low speed interfaces provided by xDSL, T1, E1, and HDSL2 interfaces.

Figure 2 - Typical ATM Switch or Shared Bus DSLAM



Attempts to incrementally improve the traditional architecture, such as by placing more modems on each line card, tend not to scale well and often run into physical and thermal limits. To properly address system level complexity it is necessary to implement system level solutions. As shown in Figure 3 the VORTEX chip set is the first in the world to provide the system-scale integration needed to fully address these requirements.

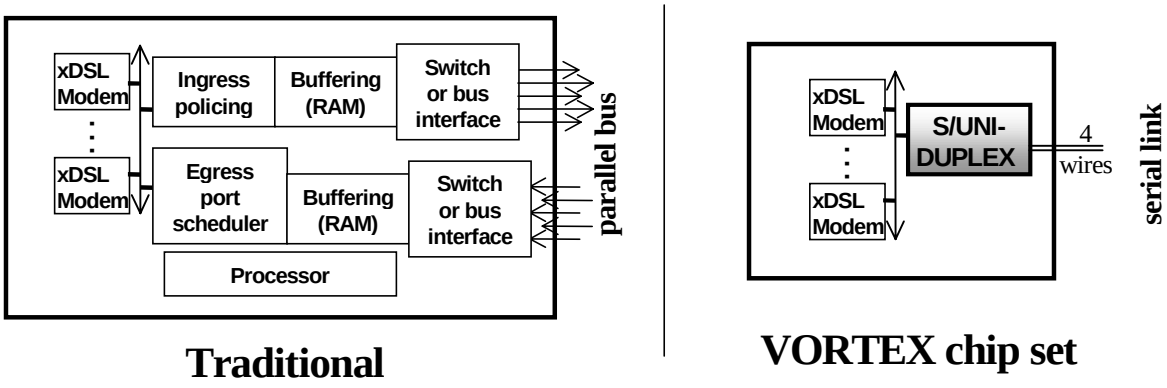
Figure 3 - The Access Multiplexer Silicon Map



Current DSLAM solutions typically employ widely distributed traffic management, switching, buffering, and control functions that span the line interface cards and the network interface card. The cards that interface to the customer's access line are the most numerous and hence cost sensitive card in the system. By applying system level integration across a family of devices the VORTEX chip set eliminates the need for traffic management, buffering and control functions on the line cards.

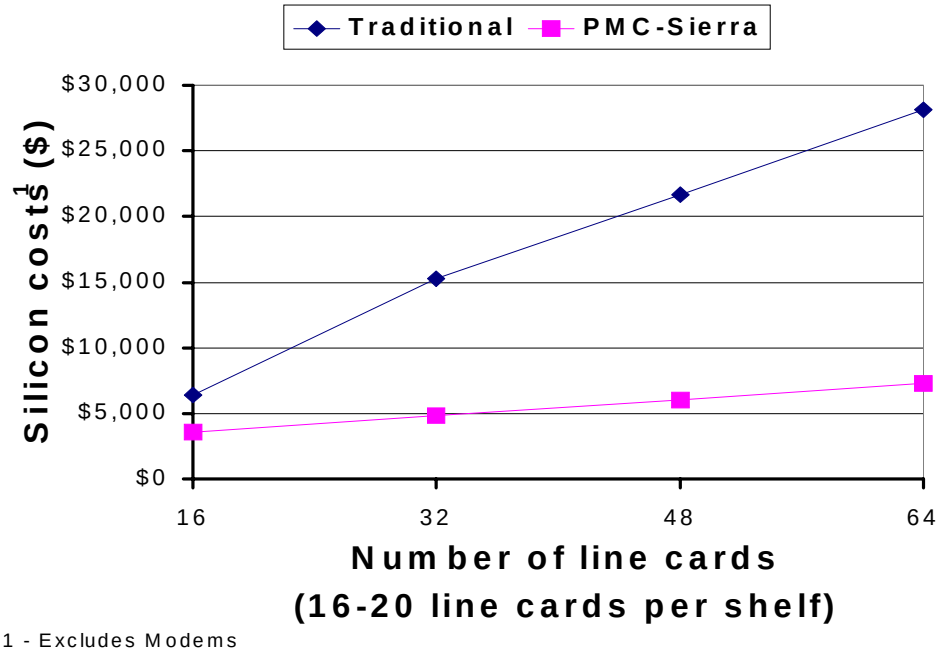
As shown in Figure 4, this reduces the line card's complexity and cost while increasing the card's reliability. The traditional interfaces to a shared bus or centralized switch fabric, typically via a parallel bus interface, are replaced by a simple serial interface, with built in protection switching capability. The traditional complex traffic management required on the card -- including packet discard, congestion control, policing, QoS support, etc. – is centralized in a common card where its costs can be spread across the maximum number of paying customers! This also eliminates complex traffic management software from the line card, making the line card's processor optional.

Figure 4 - Line Card Complexity Comparison



As modem technology matures the cost of ADSL, G.Lite, and other xDSL modems is decreasing rapidly. By remaining independent of any modem technology, equipment based on the VORTEX chip set can take full advantage of these cost reductions. Also, as modem costs decline the cost of the rest of the devices become an increasingly larger fraction of the equipment cost. As shown in the graph in Figure 5, as access equipment moves to mass market scale it becomes increasingly important to have selected the right system architecture.

Figure 5 - DSLAM System Silicon Cost

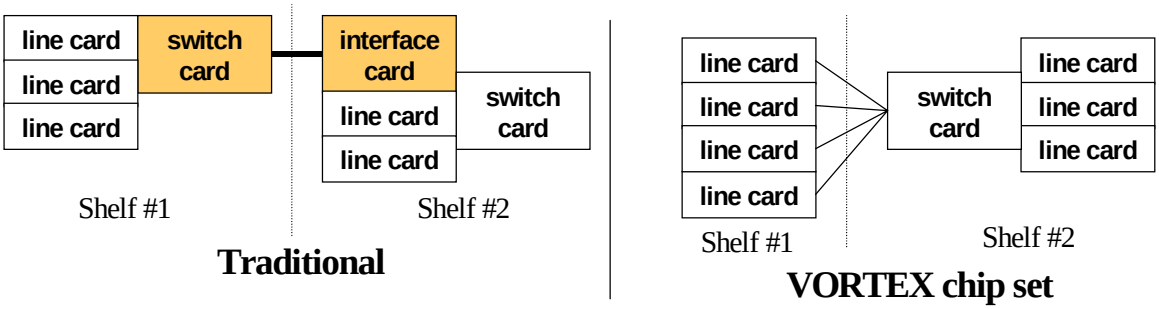


1 - Excludes Modems

The cost savings shown are derived from two main sources:

- The cost of each line card is reduced significantly as discussed previously,
- and as shown in Figure 6, traditional architectures use multiple stages of switching to tie together multiple shelves. This becomes complex and costly, especially when redundancy is used to improve fault tolerance.

Figure 6 - Multi-shelf Architecture Comparison



In the traditional architecture each shelf requires its own dedicated switch, plus an interface card on the main shelf. In this architecture maintaining fairness and QoS across all interfaces is difficult. There is also an increase in cross-switch transit delay due to the multiple switching stages -- potentially degrading voice service quality. Software complexity is high, increasing development costs and greatly increasing the risk of programming errors.

In the VORTEX chip set architecture serial point to point connections are used between the line cards and the switching card. Switching and traffic management functionality is not impacted by the physical location of the line card because to the switch card a multi-shelf configuration appears simply to be a single, very large shelf!

Software development costs and ongoing maintenance can be a significant portion of the platforms life-cycle costs. Since the VORTEX chip set eliminates the need for “intelligent” line interface cards there is a dramatic reduction in software complexity, as show by the table in Figure 7. Here we see that as the DSLAM grows the traditional architecture experiences a large increase in the number of “intelligent” elements that will require programming and software updates. An architecture based on a more centralized traffic management function, such as implemented by the VORTEX chip set, experiences very little growth in complexity even as the DSLAM grows to many racks of equipment.

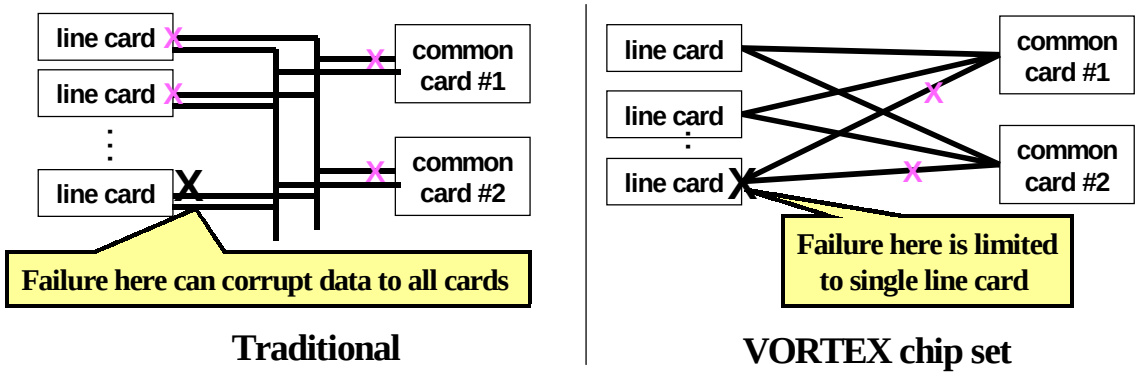
Figure 7 - Access Equipment Software Complexity

# shelves	# line cards	Traditional Architecture Complexity	VORTEX Chip Set Complexity
1	16	**17**	**1**
2	32	**34**	**1**
3	48	**51**	**1**
4	64	**68**	**1**
5	80	**85**	**2**
6	96	**102**	**2**
7	112	**119**	**2**
8	128	**136**	**2**
9	144	**153**	**3**
10	160	**170**	**3**
11	176	**187**	**3**
12	192	**204**	**3**
13	208	**221**	**4**
14	224	**238**	**4**
15	240	**255**	**4**
16	256	**272**	**4**

A key requirement that a mass market capable DSLAM must fulfil is “Carrier Grade” reliability and fault tolerance. As shown in Figure 8, with the traditional architecture the shared parallel bus allows a mechanical or device failure to corrupt all traffic on the bus. As well, the high component count on the line cards reduces reliability and software complexity is high, greatly increasing the risk of programming errors.

With the VORTEX chip set architecture the S/UNI-DUPLEX and S/UNI-VORTEX implement a high speed point-to-point serial LVDS backplane. Communication links are not shared, so failure on one line card cannot corrupt traffic to the other line cards. Direct support for duplicated common cards ensures no single failure can disable a large number of subscribers.

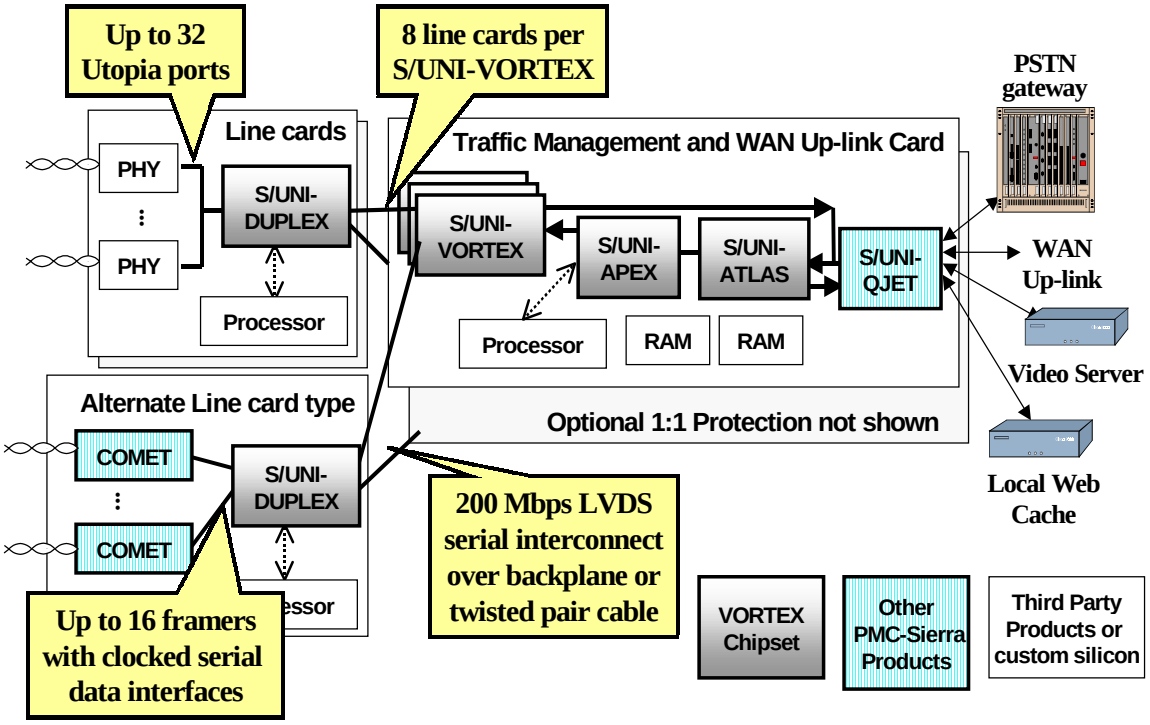
Figure 8 - Fault Tolerance Comparison



4 EXAMPLE APPLICATIONS OF THE VORTEX CHIP SET

4.1 ATM DSLAM

Figure 9 - VORTEX Chip Set Based ATM DSLAM



In an ATM DSLAM the S/UNI-VORTEX and S/UNI-DUPLEX devices work together to create an interconnect architecture in which up to 2048 modems, framers, or PHY devices are connected to working and protection common cards. Interconnect between line cards and the common card is point-to-point 4-wire serial LVDS running at 200 Mbps. S/UNI-VORTEX and S/UNI-DUPLEX are mixed signal devices and require no external analog components. They connect directly to backplane traces or up to 10 meters of inter-shelf twisted pair cabling in multi-shelf architectures.

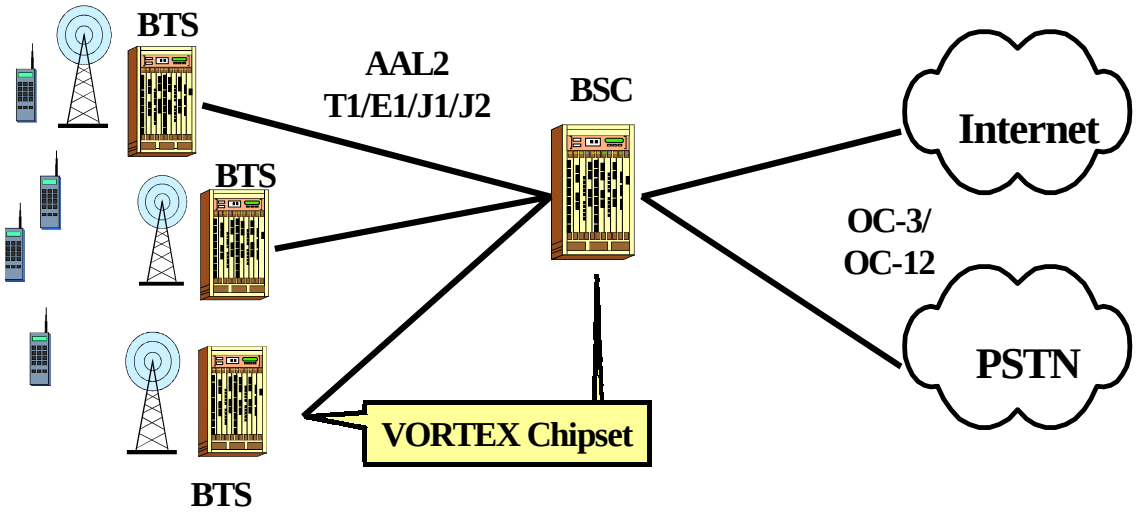
The S/UNI-ATLAS handles ingress and egress policing, address lookup/translation (i.e. switch tag generation), statistics gathering, I.610 FM & PM OAM .

The S/UNI-APEX provides per VC queuing, scheduling, and switching functions for up to 2K logical PHYs on the line side and up to four physical high speed PHYs on the WAN side. The S/UNI-APEX provides QoS parameter configuration with EPD/PPD processing for up to 64K connections.

4.2 3G Wireless

Figure 10 shows a typical network configuration for 3G wireless systems. These next generation wireless networks are being specified with ATM and AAL2 between the Base Station Controller (BSC) and the Base Transceiver Station (BTS). The links between BTS and BSC are typically multiple T1/E1/J1/J2 (often with Inverse Multiplexing over ATM or IMA). The links may also be STS-1 or OC-3, although the bandwidth actually used will normally be significantly less than 155 Mbps.

Figure 10 - 3rd Generation Wireless Network



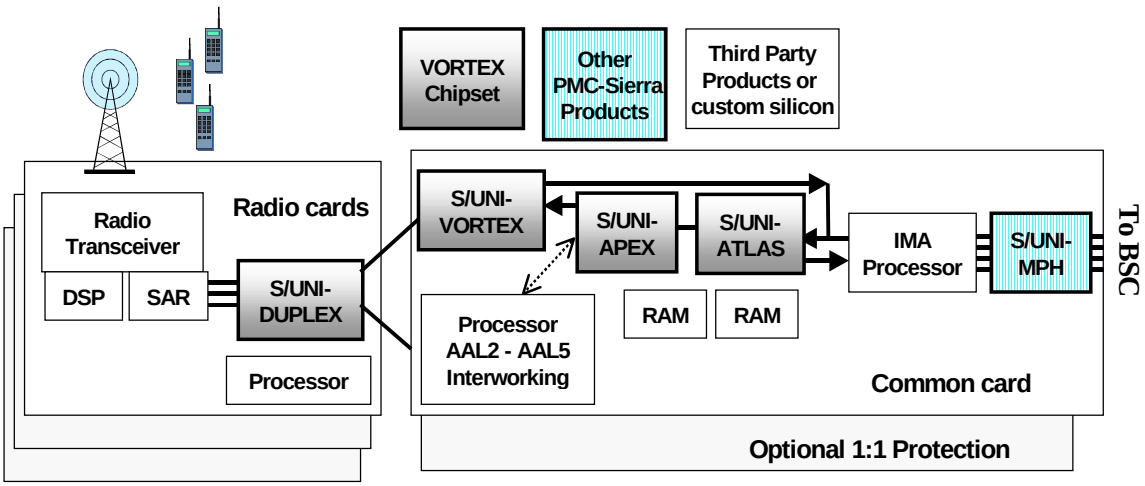
An example configuration for a BTS is shown in Figure 11. This architecture takes advantage of the serial backplane, protection switching (for large base stations), policing, traffic management, and VC switching capabilities of the VORTEX chip set. It also takes advantage of the 32 bit wide, 66 MHz, burst transfer capable microprocessor port on the S/UNI-APEX in order to attach a microprocessor to assist in the AAL2 switching needed to route AAL2 information packets to the appropriate radio cards.

In the downstream (to the radio) direction there are two cases to consider. If the AAL2 cell only contains information relevant to a single radio card then the entire cell can be directly routed to that card by the VORTEX chip set. However, if the AAL2 cell contains AAL2 packets relevant to two or more radio cards it is necessary to split the cell into its "per radio card" components before it can be routed to those cards. In this latter case the microprocessor accepts AAL2 cells from the up-link, splits them into individual cell streams per radio card, and sends them back to the S/UNI-APEX to be routed to the appropriate radio card.

In the upstream direction (to the BSC) it is likely that each radio card's AAL2 cells can be switched directly by the S/UNI-APEX since, in general, all AAL2 traffic will be heading to the BSC.

Note that all non-AAL2 traffic – for example signaling traffic encapsulated in AAL5 cells -- need not be routed through the microprocessor since this type of traffic can be switched directly by the S/UNI-APEX. The S/UNI-APEX is programmed to guarantee minimal delay of the AAL2 voice traffic plus CoS aware buffering and congestion management of the bursty AAL5 traffic.

Figure 11 - Radio Base Transceiver Station



The Downstream traffic flow has several potential paths:

AAL2 Voice: if AAL2 cell contains information for several radio cards:
MPH-IMA→Atlas→Apex→microprocessor
→Apex→Vortex→Duplex #1→SAR→DSP→Radio
→Apex→Vortex→Duplex #2→SAR→DSP→Radio
→…
or if the AAL2 cell contains information for a single radio card:
MPH-IMA→Atlas→Apex→Vortex→Duplex→SAR→DSP→Radio

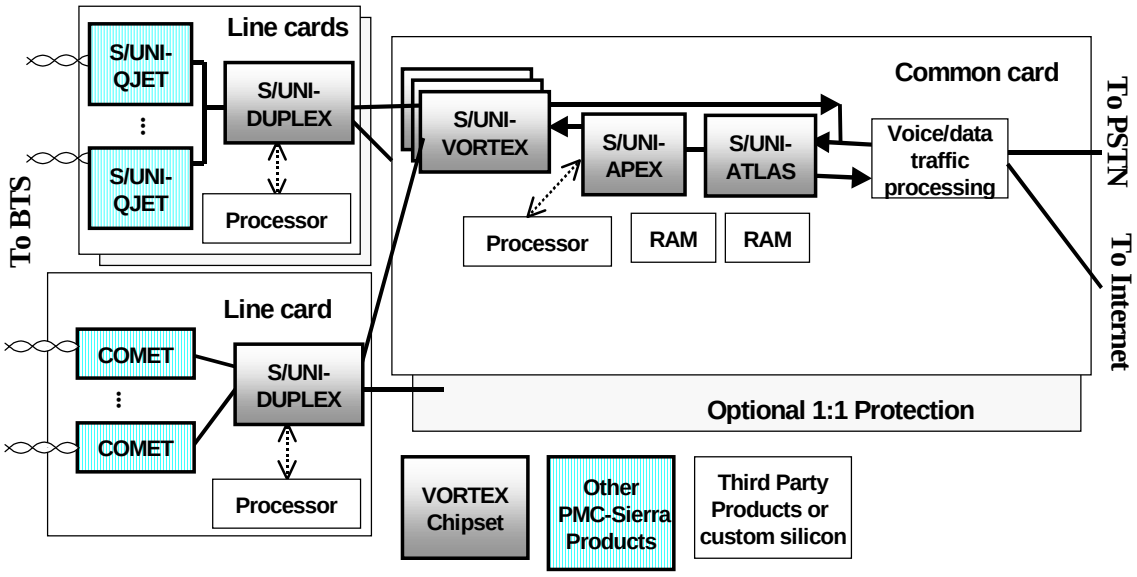
AAL5 Signaling: MPH-IMA→Atlas→Apex→Common Card Micro, or
MPH-IMA→Atlas→Apex→Vortex→Duplex→Radio Card Micro, or
Common Card Micro→Apex→Vortex→Duplex→Radio Card Micro

The Upstream traffic flow has similar options:

AAL2 Voice: Radio→DSP→SAR→Duplex→Vortex→Apex→Atlas→IMA→MPH

AAL5 Signaling: Common Card Micro→Apex→Atlas→IMA→MPH, or
R.C. Micro→Duplex→Vortex→Atlas→Apex→Atlas→IMA→MPH, or
R.C. Micro→Duplex→Vortex→Atlas→Apex→Common Card micro

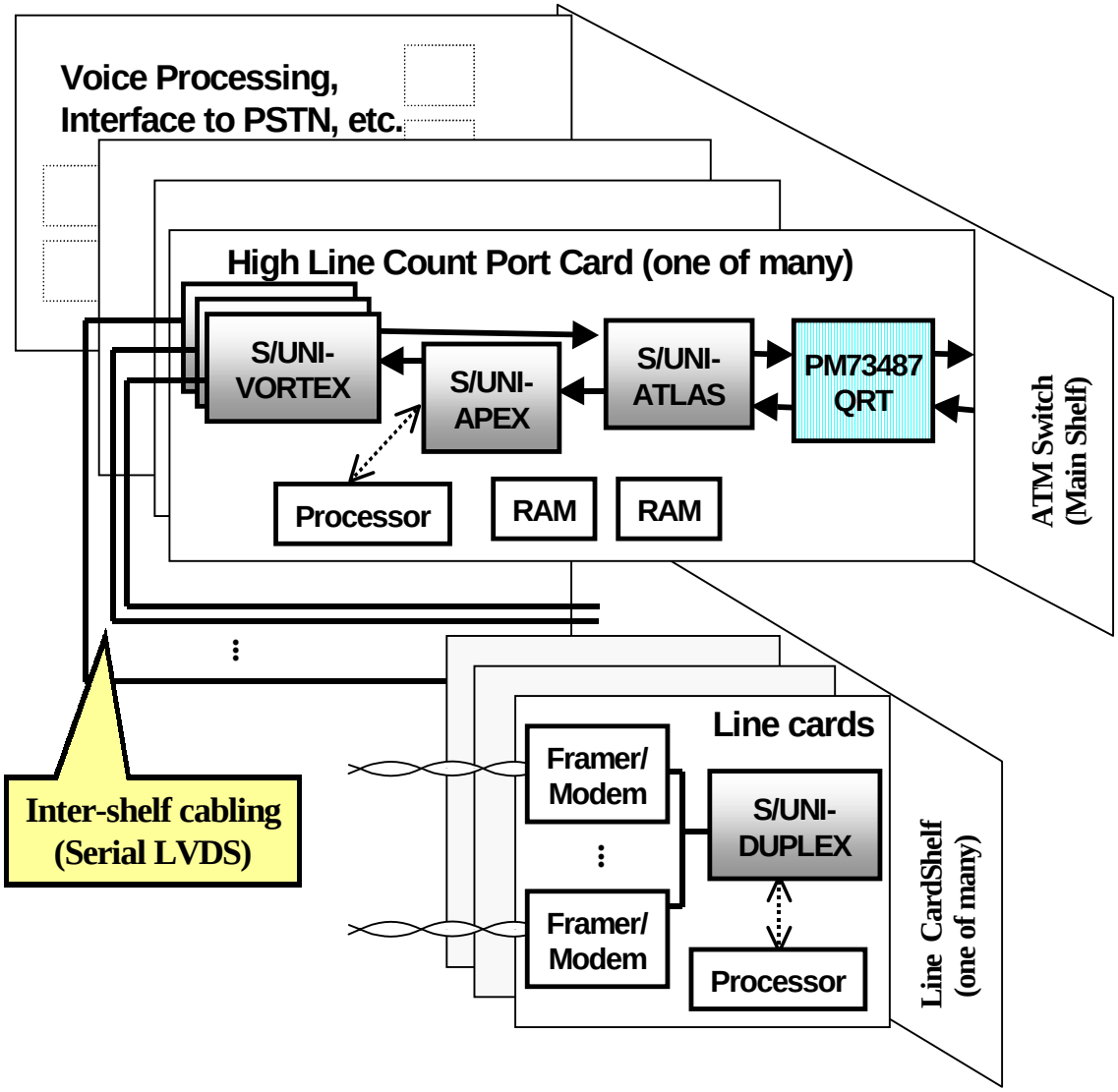
Figure 12 - Small Radio Base Station Controller



As shown in Figure 12, the “front end” portion of a small Radio Base Station Controller (BSC) handles the ATM traffic from the Base Transceiver Stations (BTS). This portion of the BSC can be built much like a DSLAM. The key function of the front end is to terminate the numerous T1/E1 or DS-3 lines and switch the traffic to and from the voice processors and data network interface.

Figure 13 shows a much larger BSC in which the Vortex Chip Set is used to create several multi-shelf, high line count port cards connected to an underlying high bandwidth ATM switching platform such as can be built with PMC-Sierra’s QRT and QSE ATM switching devices. In this example the voice processing is centralized on server cards and the ATM switch provides the necessary inter-card connections and traffic switching. The use of the VORTEX chip set in a high line count ATM switch is described further in Section 4.3.

Figure 13 - Large BSC using ATM Switch



4.3 Multi-service Access Switches

Figure 14 provides an example of a “frame at the edge, cells in the core” architecture that takes advantage of the packet contiguous switching capabilities of the S/UNI-APEX. A SAR is used to convert from frames to cells, but the SAR’s reassembly functionality is greatly simplified because all cells arrive at the SAR in packet contiguous order, meaning, packet reassembly does not have to span multiple packet streams.

Figure 15 is an example of a high line count OC-12 switch port in a multi-gigabit ATM switch. This example is similar to that shown in Figure 13. The port card handles the egress traffic for a large number of low speed interfaces that are terminated on numerous line cards located in the same or separate shelves. The S/UNI-APEX is

acting strictly as an OC-12 uni-directional egress traffic scheduler. Although another ATM switching device could be used (e.g. if the customer has existing switch frabric ASICs), in this example the OC-12 ingress traffic buffering is handled by another PMC-Sierra ATM switching device, the PM73487 QRT. Combined with the PM73488 QSE switching device (not shown), the QRT/QSE combination can be used to implement a highly scalable high speed ATM switch architecture. See the PMC-Sierra web site for details about the QRT and QSE devices.

Figure 14 - High Density Frame Relay Port Card

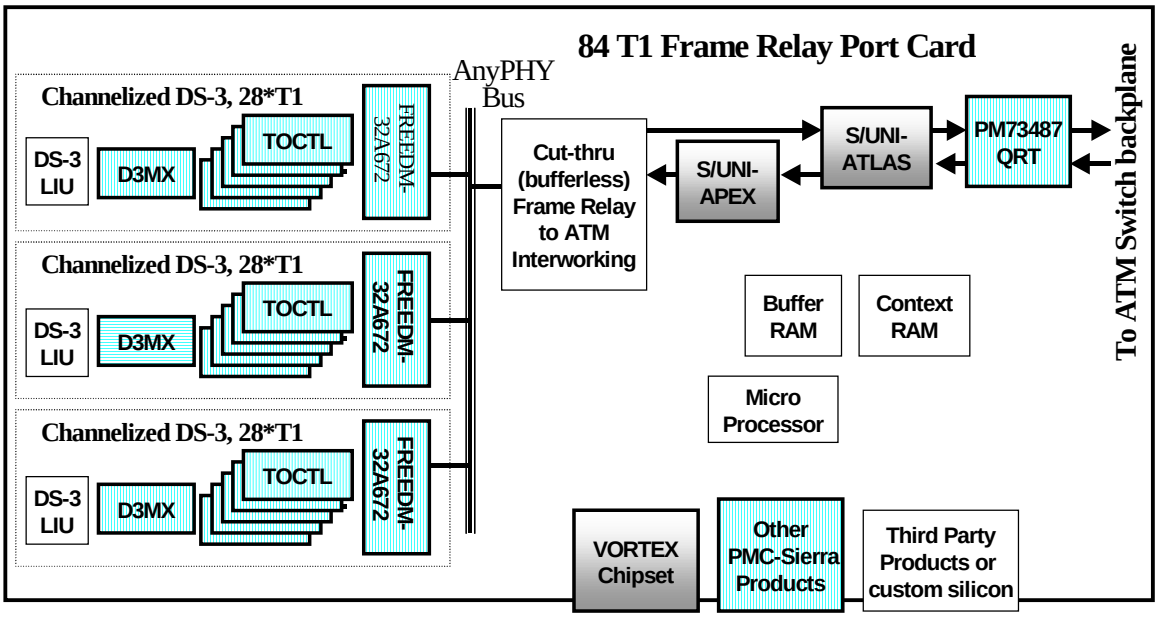
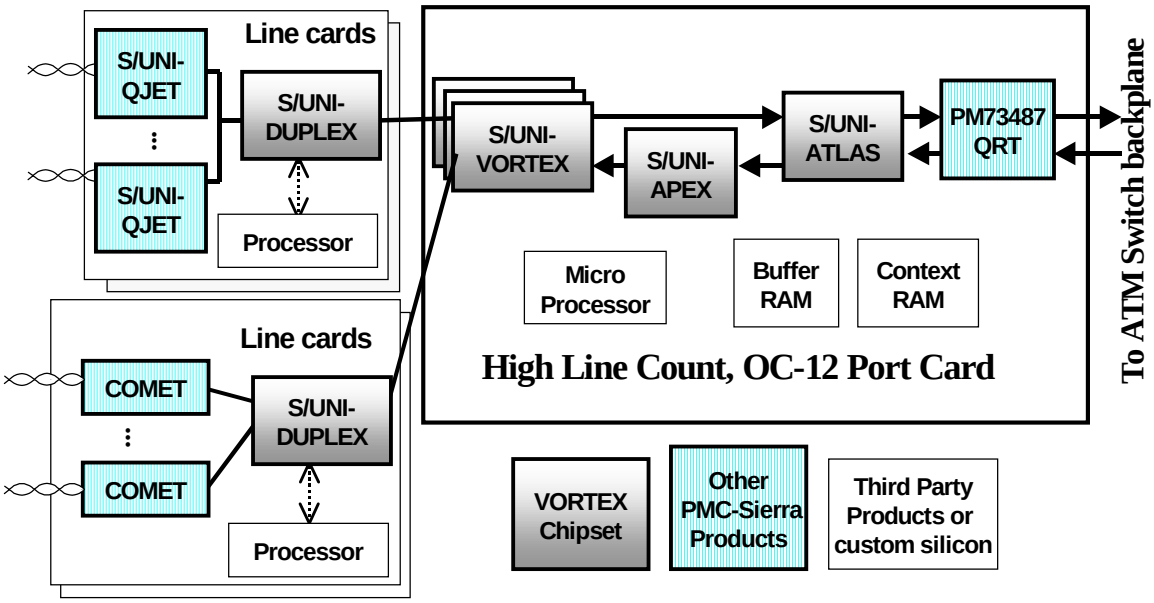


Figure 15 - High Line Count OC-12 ATM Switch Port



5 CONCLUSION

The VORTEX chip set fully addresses the data path requirements for the exploding markets of wireline and wireless network access. The key requirements of these markets are:

- efficient processing of voice and data traffic from hundreds or even thousands of lines or channels,
- full featured quality of service differentiation on every port,
- built in fault tolerance and protection switching of common components,
- simplified software architecture, and
- support for simple in-field upgrades.

There is a single phrase that summarizes PMC-Sierra's goal in developing the VORTEX chip set:

A mass market architecture for mass market deployment of 3G wireless and high speed access services

NOTES

CONTACTING PMC-SIERRA, INC.

PMC-Sierra, Inc.
105-8555 Baxter Place Burnaby, BC
Canada V5A 4V7

Tel: (604) 415-6000

Fax: (604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Application Information: apps@pmc-sierra.com
Web Site: http://www.pmc-sierra.com

PMC-990712 (P1) Issue date: July 1999