CMOS 16-bit Microcontrollers

TMP93CS42AF

1. Outline and Device Characteristics

The TMP93CS42A is high-speed advanced 16-bit microcontroller developed for controlling medium to large-scale equipment. The TMP93CS42A has a built-in ROM.
The TMP93CS42AF is housed in 100-pin flat package.
The device characteristics are as follows:

(1) Original 16-bit CPU (900/L CPU)

- TLCS-90 instruction mnemonic upward compatible
- 16 M-byte linear address space
- General-purpose registers and register bank system
- 16-bit multiplication/division and bit transfer/arithmetic instructions
- Micro DMA : 4 channels (1.6 μs / 2 bytes at 20 MHz)

(2) Minimum instruction execution time : 200 ns at 20 MHz

(3) Internal RAM : 2 Kbytes
Internal ROM : 64 Kbytes

(4) External memory expansion

- Can be expanded up to 16 M-bytes (for both programs and data).
- Can mix 8- and 16-bit external data buses.
  ···Dynamic data bus sizing

(5) 8-bit timer : 2 channels

(6) 8-bit PWM timer : 2 channels

(7) 16-bit timer : 2 channels

(8) Serial interface : 2 channels

(9) 10-bit AD converter : 5 channels

(10) Watchdog timer

(11) Chip select/wait controller : 3 blocks

(12) Interrupt functions : 29

- 9 CPU interrupts ……SWI instruction, and Illegal instruction
- 12 internal interrupts
- 8 external interrupts

} 7-level priority can be set.

(13) I/O ports :

80 pins

(14) Standby function :

4 halt modes (RUN, IDLE2, IDLE1, STOP)

(15) Clock gear function

- Clock can be changed fc to fc/16.

(16) Operating voltage

- Vcc = 4.5 to 5.5 V

(17) Package

- P-QFP100-1414-0.50

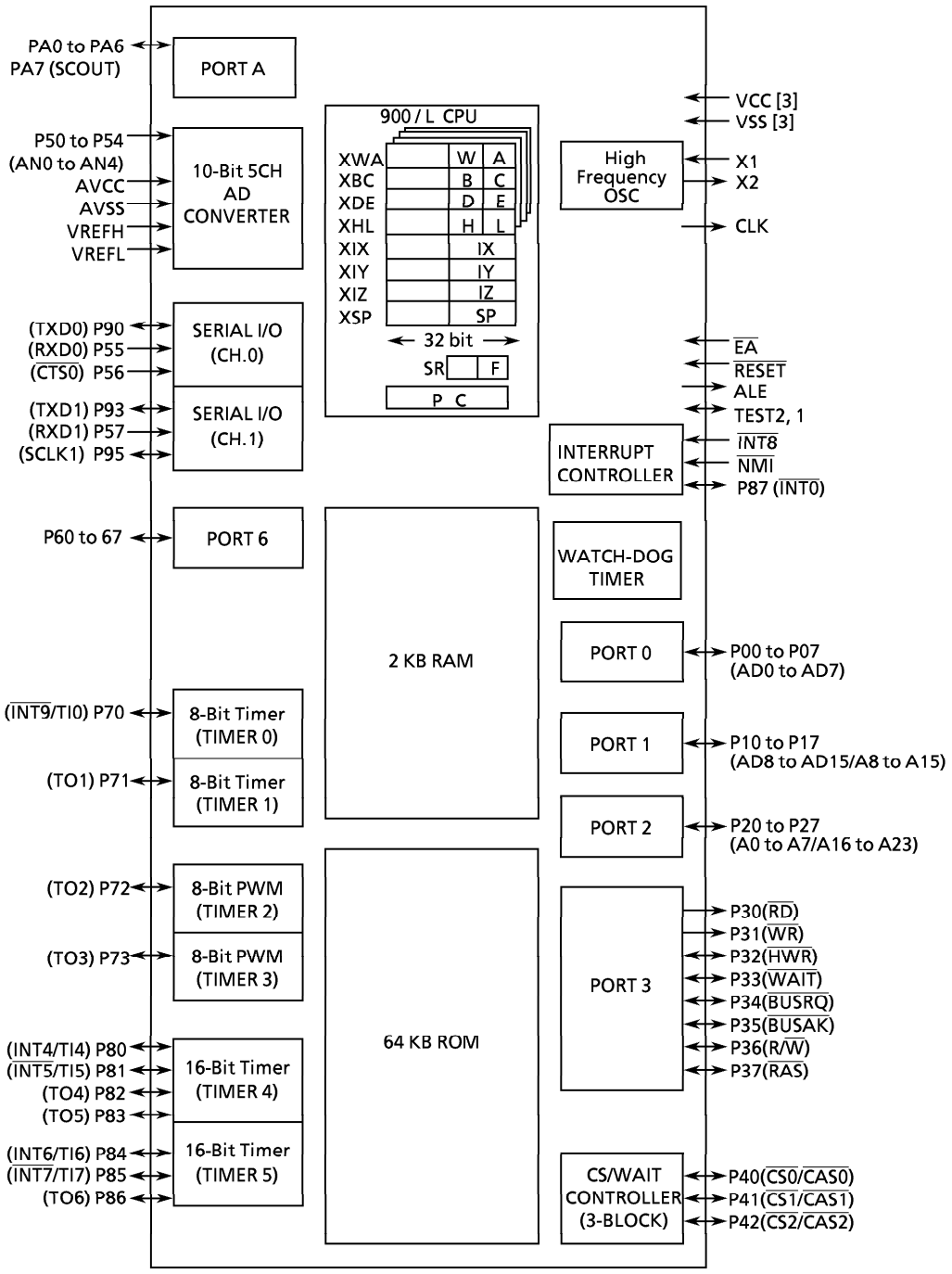


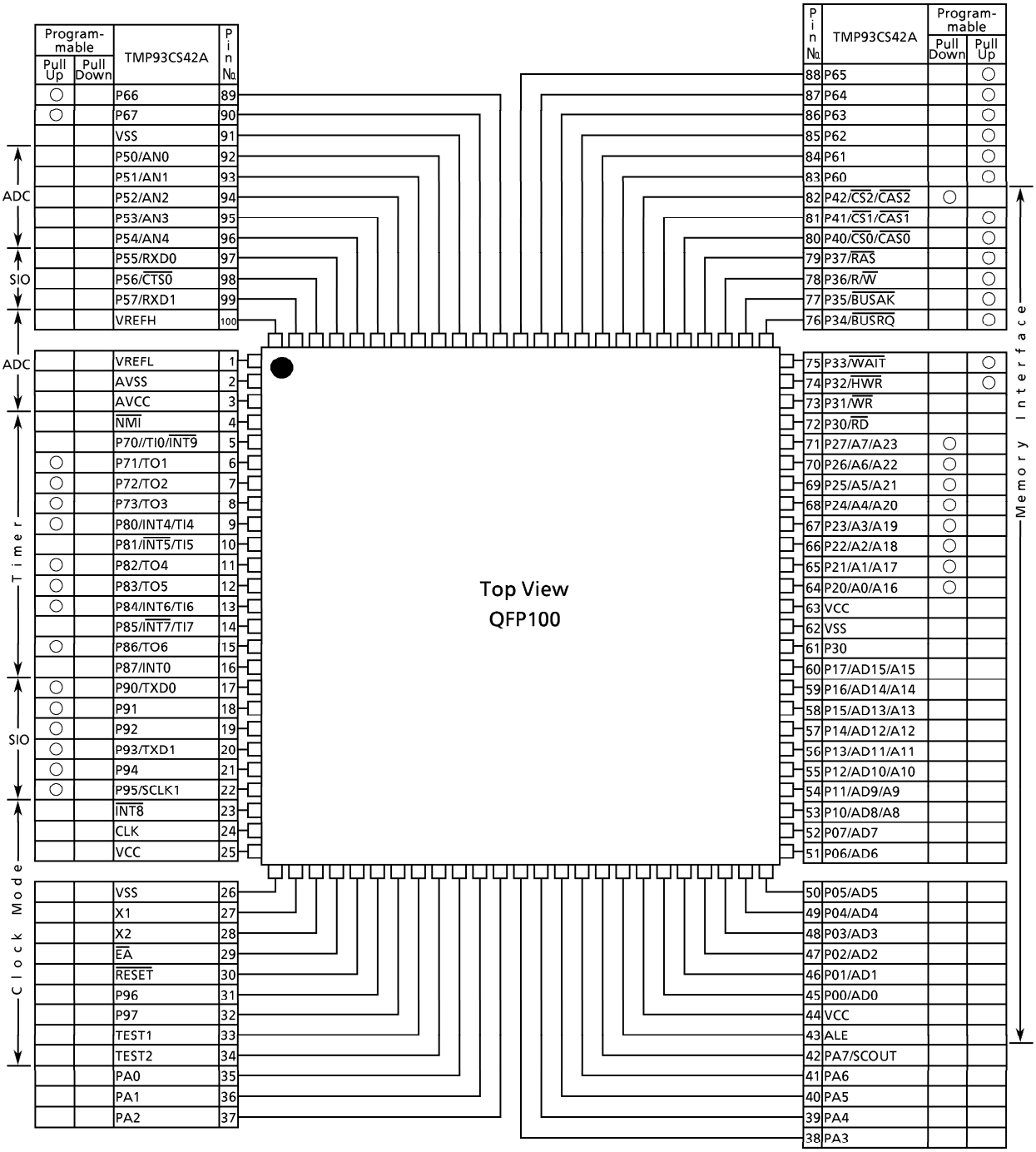
Figure 1.1 TMP93CS42A Block Diagram

2. Pin Assignment and Function

The assignment of input/output pins for the TMP93CS42A, their names and outline functions are described below.

2.1 Pin Assignment

Figure 2.1.1 shows pin assignment of the TMP93CS42AF.



Programmable Pull Up	Programmable Pull Down	TMP93CS42A	Pin No.
○		P66	89
○		P67	90
		VSS	91
		P50/AN0	92
		P51/AN1	93
		P52/AN2	94
		P53/AN3	95
		P54/AN4	96
		P55/RXD0	97
		P56/$\overline{CTS0}$	98
		P57/RXD1	99
		VREFH	100
		VREFL	1
		AVSS	2
		AVCC	3
		$\overline{NMI}$	4
		P70//TI0/$\overline{INT9}$	5
○		P71/TO1	6
○		P72/TO2	7
○		P73/TO3	8
○		P80/INT4/TI4	9
		P81/$\overline{INT5}$/TI5	10
○		P82/TO4	11
○		P83/TO5	12
○		P84/INT6/TI6	13
		P85/$\overline{INT7}$/TI7	14
○		P86/TO6	15
		P87/INT0	16
○		P90/TXD0	17
○		P91	18
○		P92	19
○		P93/TXD1	20
○		P94	21
○		P95/SCLK1	22
		$\overline{INT8}$	23
		CLK	24
		VCC	25
		VSS	26
		X1	27
		X2	28
		$\overline{EA}$	29
		$\overline{RESET}$	30
		P96	31
		P97	32
		TEST1	33
		TEST2	34
		PA0	35
		PA1	36
		PA2	37

Pin No.	TMP93CS42A	Programmable Pull Down	Programmable Pull Up
88	P65		○
87	P64		○
86	P63		○
85	P62		○
84	P61		○
83	P60		○
82	P42/$\overline{CS2}$/$\overline{CAS2}$	○	
81	P41/$\overline{CS1}$/$\overline{CAS1}$		○
80	P40/$\overline{CS0}$/$\overline{CAS0}$		○
79	P37/$\overline{RAS}$		○
78	P36/R/$\overline{W}$		○
77	P35/$\overline{BUSAK}$		○
76	P34/$\overline{BUSRQ}$		○
75	P33/$\overline{WAIT}$		○
74	P32/$\overline{HWR}$		○
73	P31/$\overline{WR}$		
72	P30/$\overline{RD}$		
71	P27/A7/A23	○	
70	P26/A6/A22	○	
69	P25/A5/A21	○	
68	P24/A4/A20	○	
67	P23/A3/A19	○	
66	P22/A2/A18	○	
65	P21/A1/A17	○	
64	P20/A0/A16	○	
63	VCC		
62	VSS		
61	P30		
60	P17/AD15/A15		
59	P16/AD14/A14		
58	P15/AD13/A13		
57	P14/AD12/A12		
56	P13/AD11/A11		
55	P12/AD10/A10		
54	P11/AD9/A9		
53	P10/AD8/A8		
52	P07/AD7		
51	P06/AD6		
50	P05/AD5		
49	P04/AD4		
48	P03/AD3		
47	P02/AD2		
46	P01/AD1		
45	P00/AD0		
44	VCC		
43	ALE		
42	PA7/SCOUT		
41	PA6		
40	PA5		
39	PA4		
38	PA3		

Figure 2.1.1 shows pin assignment of TMP93CS42AF.

2.2 Pin Names and Functions

Table 2.2.1 Pin Names and Functions.

Table 2.2.1 Pin Names and Functions (1/4)

Pin name	Number of pins	I/O	Function
P00 to P07 AD0 to AD7	8	I/O Tri-state	Port 0: I/O port that allows selection of I/O on a bit basis Address/data (lower): Bits 0 to 7 of address/data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O Tri-state Output	Port 1: I/O port that allows selection of I/O on a bit basis Address data (upper): Bits 8 to 15 of address/data bus Address: Bits 8 to 15 of address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows selection of I/O on a bit basis (with pull-down resistor) Address: Bits 0 to 7 of address bus Address: Bits 16 to 23 of address bus
P30 $\overline{RD}$	2 1	Output Output	Port 30: Output port. 72 pin is also used as $\overline{RD}$, 61 pin is used only for P30. Read: Strobe signal for reading external memory
P31 $\overline{WR}$	1	Output Output	Port 31: Output port Write: Strobe signal for writing data on pins AD0 to 7
P32 $\overline{HWR}$	1	I/O Output	Port 32: I/O port (with pull-up resistor) High write: Strobe signal for writing data on pins AD8 to 15
P33 $\overline{WAIT}$	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: Pin used to request CPU bus wait
P34 $\overline{BUSRQ}$	1	I/O Input	Port34: I/O port (with pull-up resistor) Bus request: Pin used to request bus release
P35 $\overline{BUSAK}$	1	I/O Output	Port 35: I/O port (with pull-up resistor) Bus acknowledge: Pin used to acknowledge bus release
P36 R/$\overline{W}$	1	I/O Output	Port 36: I/O port (with pull-up resistor) Read/write: 1 represents read or dummy cycle; 0, write cycle.
P37 $\overline{RAS}$	1	I/O Output	Port 37: I/O port (with pull-up resistor) Row address strobe: Outputs $\overline{RAS}$ strobe for DRAM.
P40 $\overline{CS0}$ $\overline{CAS0}$	1	I/O Output Output	Port 40: I/O port (with pull-up resistor) Chip select 0: Outputs 0 when address is within specified address area. Column address strobe 0: Outputs $\overline{CAS}$ strobe for DRAM when address is within specified address area.

Note : This device's built-in memory or built-in I/O cannot be accessed with the external DMA controller using the $\overline{BUSRQ}$ and $\overline{BUSAK}$ signals.

Table 2.2.1 Pin Names and Functions (2/4)

Pin name	Number of pins	I/O	Function
P41 $\overline{CS1}$ $\overline{CAS1}$	1	I/O Output Output	Port 41: I/O port (with pull-up resistor) Chip select 1: Outputs 0 if address is within specified address area. Column address strobe 1: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P42 $\overline{CS2}$ $\overline{CAS2}$	1	I/O Output Output	Port 42: I/O port (with pull-down resistor) Chip select 2: Outputs 0 if address is within specified address area. Column address strobe 2: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P50 to P57 AN0 to AN4 RXD0 $\overline{CTS0}$ RXD1	8	Input Input Input Input Input	Port 5: Input port Analog input: Analog signal input for AD converter Serial receive data 0 Serial data send enable 0 (Clear to Send) Serial receive data 1
VREFH	1	Input	Pin for high level reference voltage input to AD converter
VREFL	1	Input	Pin for low level reference voltage input to AD converter
P60 to P67	8	I/O	Ports 60 to 67: I/O ports that allow selection of I/O on a bit basis (with pull-up resistor)
P70 TI0 $\overline{INT9}$	1	I/O Input Input	Port 70: I/O port (with pull-up resistor) Timer input 0: Timer 0 input Interrupt request pin 9: Interrupt request pin with falling edge. (TTL level)
P71 TO1	1	I/O Output	Port 71: I/O port (with pull-up resistor) Timer output 1: Timer 0 or 1 output
P72 TO2	1	I/O Output	Port 72: I/O port (with pull-up resistor) PWM output 2: 8-bit PWM timer 2 output
P73 TO3	1	I/O Output	Port 73: I/O port (with pull-up resistor) PWM output 3: 8-bit PWM timer 3 output
P80 TI4 INT4	1	I/O Input Input	Port 80: I/O port (with pull-up resistor) Timer input 4: Timer 4 count / capture trigger signal input Interrupt request pin 4: Interrupt request pin with programmable rising / falling edge.
P81 TI5 $\overline{INT5}$	1	I/O Input Input	Port 81: I/O port Timer input 5: Timer 4 count / capture trigger signal input Interrupt request pin 5: Interrupt request pin with falling edge. (TTL level)
P82 TO4	1	I/O Output	Port 82: I/O port (with pull-up resistor) Timer output 4: Timer 4 output pin
P83 TO5	1	I/O Output	Port 83: I/O port (with pull-up resistor) Timer output 5: Timer 4 output pin

Table 2.2.1 Pin Names and Functions (3/4)

Pin name	Number of pins	I/O	Function
P84 TI6 INT6	1	I/O Input Input	Port 84: I/O port (with pull-up resistor) Timer input 6: Timer 5 count / capture trigger signal input Interrupt request pin 6: Interrupt request pin with programmable rising / falling edge
P85 TI7 $\overline{INT7}$	1	I/O Input Input	Port 85: I/O port (with pull-up resistor) Timer input 7: Timer 5 count / capture trigger signal input Interrupt request pin 7: Interrupt request pin with falling edge (TTL level)
P86 TO6	1	I/O Output	Port 86: I/O port (with pull-up resistor) Timer output 6: Timer 5 output pin
P87 $\overline{INT0}$	1	I/O Input	Port 87: I/O port (with pull-up resistor) Interrupt request pin 0 : Interrupt request pin with programmable level/falling edge (TTL level)
P90 TXD0	1	I/O Input	Port 90: I/O port (with pull-up resistor) Serial send data 0
P91	1	I/O	Port 91: I/O port (with pull-up resistor)
P92	1	I/O	Port 92: I/O port (with pull-up resistor)
P93 TXD1	1	I/O Output	Port 93: I/O port (with pull-up resistor) Serial send data 1
P94	1	I/O	Port 94: I/O port (with pull-up resistor)
P95 SCLK1	1	I/O I/O	Port 95: I/O port (with pull-up resistor) Serial clock I/O 1
P96	1	I/O	Port 96: I/O port (Open Drain Output)
P97	1	I/O	Port 97: I/O port (Open Drain Output)
PA0 to PA6	7	I/O	Port A0 to A6 : I/O ports
PA7 SCOUT	1	I/O Output	Port A7: I/O port System Clock Output: Outputs f_{FPH} or f_{SYS} clock
$\overline{INT8}$	1	Input	Interrupt request pin 8 : Interrupt request pin with falling edge. (TTL level)
$\overline{NMI}$	1	Input	Non-maskable interrupt request pin : Interrupt request pin with programmable falling/rising edge
CLK	1	Output	Clock output: Outputs [f_{SYS}] Clock. Pulled-up during reset. can be disabled for reducing noise.
$\overline{EA}$	1	Input	External access: "1" should be inputted. (See Note on usage ⑭ in section 7.)
ALE	1	Output	Address Latch Enable (Can be disabled for reducing noise.)
$\overline{RESET}$	1	Input	Reset: Initializes TMP93CS42A. (with pull-up resistor)
X1/X2	2	I/O	High Frequency Oscillator connecting pin
TEST1 / TEST2	2	Output / Input	TEST1 Should be connected with TEST2 pin.

Table 2.2.1 Pin Names and Functions (4/4)

Pin name	Number of pins	I/O	Function
VCC	3		Power supply pin (All VCC pins are connected to the power supply source.)
VSS	3		GND pin (All VSS pins are connected with GND (0 V).)
AVCC	1		Power supply pin for AD converter
AVSS	1		GND pin for AD converter (0 V)

Note : Built-in pull-up / pull-down resistors can be released from the pins other than the $\overline{\text{RESET}}$ pin by software.

3. Operation

This section describes the functions and basic operational blocks of the TMP93CS42A devices.
See the「7. Points of Concern and Restrictions」for the using notice and restrictions for each block.

3.1 CPU

The TMP93CS42A device has a built-in high-performance 16-bit CPU (900/L CPU). (For CPU operation, see TLCS-900/L CPU in the previous section).
This section describes CPU functions unique to the TMP93CS42A that are not described in the previous section.

3.1.1 Reset

To reset the TMP93CS42A, the $\overline{\text{RESET}}$ input must be kept at 0 for at least 10 system clocks (Resetting initializes the clock gear to 1/16. : 16 μs at 20 MHz) within the operating voltage range and with a stable oscillation.
When reset is accepted, the CPU sets as follows :

- Program Counter (PC) according to Reset Vector that is stored 8000H to 8002H.
  PC (7 - 0) ← stored data to 8000H
  PC (15 - 8) ← stored data to 8001H
  PC (23 - 16) ← stored data to 8002H
- Stack pointer (XSP) for system mode to 100H.
- Status register <IFF2-0> to 111. (Sets mask register to interrupt level 7.)
- Status register <MAX> to 1. (Sets to maximum mode)
- Status register <REP2-0> to 000. (Sets register banks to 0.)

When reset is released, instruction execution starts from PC (reset vector). CPU internal registers other than the above are not changed.
When reset is accepted, processing for built-in I/Os, ports, and other pins are as follows

- Initializes built-in I/O registers as per specifications.
- Sets port pins (including pins also used as built-in I/Os) to general-purpose input / output port mode.
- Watchdog timer is set to enable.
- Pulls up the CLK pin to 1.
- Sets the ALE pin to High Impeadance (High-z)

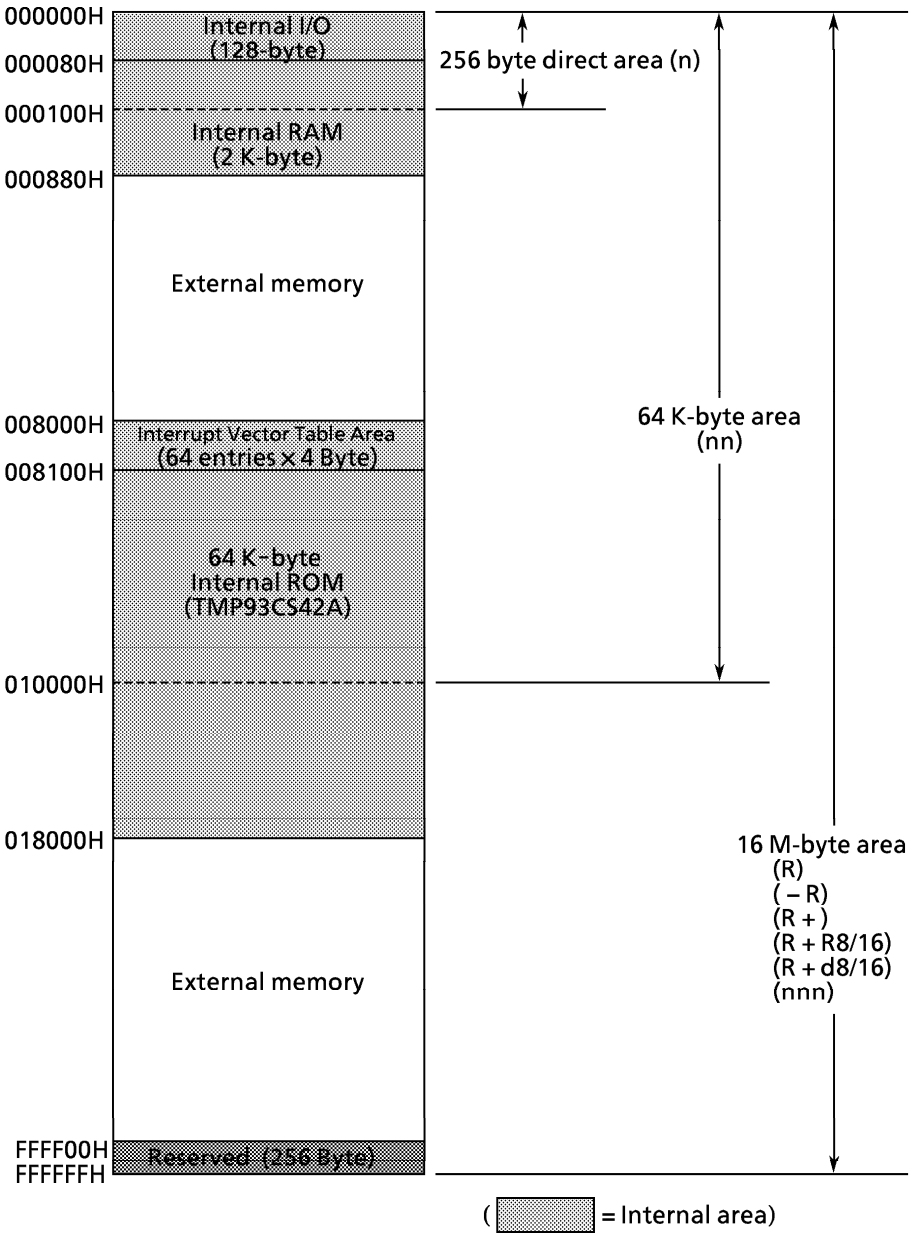
Note 1 : By resetting, register in the CPU except program counter (PC), status register (SR) and stack pointer (XSP) and the data in internal RAM are not changed.

Note 2 : The CLK pin is pulled up during reset. When the voltage is externally put down, there is possible to cause malfunctions.

Figure 3.1.1 shows the reset timing chart of TMP93CS42A.

3.2 Memory Map

Figure 3.2.1 is a memory map of the TMP93CS42A.



Note : The 256 Byte Area from FFFF00H to FFFFFFH can not be used.

Figure 3.2.1 Memory map

4. Electrical Characteristics

4.1 Absolute Maximum Ratings (TMP93CS42AF)

"X" used in an expression shows a frequency of clock f_{PH} selected by SYSCR1<SYSCK>. If a clock gear is selected, a value of "X" is different. The value as an example is calculated at fc, *gear* = 1/fc (SYSCR1<SYSCK, GEAR 2 to 0> = "0000").

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	− 0.5 to 6.5	V
Input Voltage	V_{IN}	− 0.5 to V_{CC} + 0.5	V
Output Current (total)	ΣI_{OL}	120	mA
Output Current (total)	ΣI_{OH}	− 80	mA
Power Dissipation (Ta = 85℃)	P_D	600	mW
Soldering Temperature (10 s)	T_{SOLDER}	260	℃
Storage Temperature	T_{STG}	− 65 to 150	℃
Operating Temperature	T_{OPR}	− 40 to 85	℃

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Characteristics (1/2)

Parameter		Symbol	Condition	Min	Typ. (Note)	Max	Unit
Power Supply Voltage ($AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS} = 0$ V)		V_{CC}	fc = 4 to 20 MHz	4.5		5.5	V
Input Low Voltage	AD0 to 15	V_{IL}	V_{CC} = 5 V ± 10%	−0.3		0.8	V
	Port2 to A (except P87, P5)	V_{IL1}				0.3 V_{CC}	
	RESET, NMI	V_{IL2}				0.25 V_{CC}	
	EA	V_{IL3}				0.3	
	X1	V_{IL4}				0.2 V_{CC}	
	INT0, INT5, INT7, INT8, INT9	V_{IL5}				0.8	
Input High Voltage	AD0 to 15	V_{IH}	V_{CC} = 5 V ± 10%	2.2		V_{CC} + 0.3	
	Port2 to A (except P87)	V_{IH1}		0.7 V_{CC}			
	RESET, NMI	V_{IH2}		0.75 V_{CC}			
	EA	V_{IH3}		V_{CC} − 0.3			
	X1	V_{IH4}		0.8 V_{CC}			
	INT0, INT5, INT7, INT8, INT9	V_{IH5}		2.8			
Output Low Voltage		V_{OL}	I_{OL} = 1.6 mA (V_{CC} = 5 V ± 10%)			0.45	V
Output High Voltage		V_{OH}	I_{OH} = − 400 μA (V_{CC} = 5 V ± 10%)	4.2			

Note : Typical values are for Ta = 25 °C and V_{CC} = 5 V unless otherwise noted.

4.2 DC Characteristics (2/2)

Parameter	Symbol	Condition	Min	Typ.(Note1)	Max	Unit
Darlington Drive Current (8 Output Pins Max)	I_{DAR} (Note2)	V_{EXT} = 1.5 V R_{EXT} = 1.1 kΩ V_{CC} = 5 V ± 10%	– 1.0		– 3.5	mA
Input Leakage Current	I_{LI}	$0.0 \leqq V_{IN} \leqq V_{CC}$		0.02	± 5	μA
Output Leakage Current	I_{LO}	$0.2 \leqq V_{IN} \leqq V_{CC} - 0.2$		0.05	± 10	
Power Down Voltage (at STOP, RAM Back up)	V_{STOP}	V_{IL2} = 0.2 V_{CC}, V_{IH2} = 0.8 V_{CC}	2.0		6.0	V
$\overline{\text{RESET}}$ Pull Up Resister	R_{RST}	V_{CC} = 5 V ± 10%	50		150	kΩ
Pin Capacitance	C_{IO}	fc = 1 MHz			10	pF
Schmitt Width $\overline{\text{RESET}}$, NMI	V_{TH}		0.4	1.0		V
Programmable Pull Down Resistor	R_{KL}	V_{CC} = 5 V ± 10%	10		80	kΩ
Programmable Pull Up Resistor	R_{KH}	V_{CC} = 5 V ± 10%	50		150	
NORMAL (Note3)	I_{CC}	V_{CC} = 5 V ± 10% fc = 20 MHz		19	25	mA
NORMAL2 (Note4)				24	30	
RUN				17	25	
IDLE2				10	15	
IDLE1				3.5	5	
STOP		V_{CC} = 5 V ± 10%		0.2	10	μA

Note 1 : Typical values are for Ta = 25°C and Vcc = 5 V unless otherwise noted.
Note 2 : I_{DAR} is guaranteed for total of up to 8 ports.
Note 3 : The condition of measurement of Icc (NORMAL).
Operates only CPU, output ports are open and input ports fixed.
Note 4 : The condition of measurement of Icc (NORMAL2).
Operates all functions, output ports are open and input port fixed.

4.3 AC Characteristics

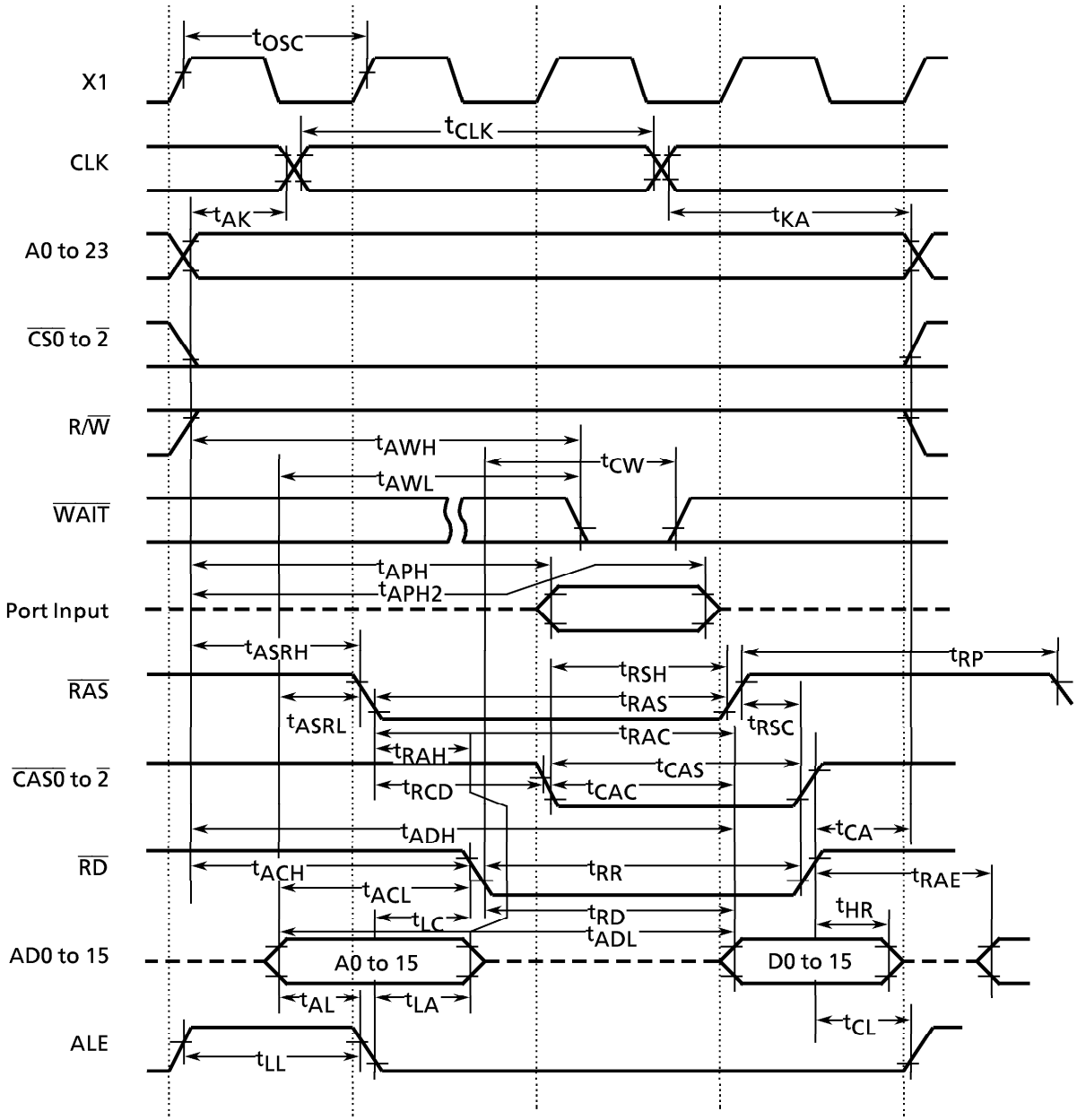
V_{CC} = 5 V ± 10%

No.	Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Osc. Period (= x)	t_{OSC}	50	31250	62.5		50		ns
2	CLK pulse width	t_{CLK}	2x – 40		85		60		ns
3	A0 to 23 Valid→ CLK Hold	t_{AK}	0.5x – 20		11		5		ns
4	CLK Valid→ A0 to 23 Hold	t_{KA}	1.5x – 70		24		5		ns
5	A0 to 15 Valid→ ALE fall	t_{AL}	0.5x – 15		16		10		ns
6	ALE fall→ A0 to 15 Hold	t_{LA}	0.5x – 20		11		5		ns
7	ALE High pulse width	t_{LL}	x – 40		23		10		ns
8	ALE fall→ $\overline{RD}$/$\overline{WR}$ fall	t_{LC}	0.5x – 25		6		0		ns
9	$\overline{RD}$/$\overline{WR}$ rise→ ALE rise	t_{CL}	0.5x – 20		11		5		ns
10	A0 to 15 Valid→ $\overline{RD}$/$\overline{WR}$ fall	t_{ACL}	x – 25		38		25		ns
11	A0 to 23 Valid→ $\overline{RD}$/$\overline{WR}$ fall	t_{ACH}	1.5x – 50		44		25		ns
12	$\overline{RD}$/$\overline{WR}$ rise→ A0 to 23 Hold	t_{CA}	0.5x – 25		6		0		ns
13	A0 to 15 Valid→ D0 to 15 input	t_{ADL}		3.0x – 55		133		95	ns
14	A0 to 23 Valid→ D0 to 15 input	t_{ADH}		3.5x – 65		154		110	ns
15	$\overline{RD}$ fall → D0 to 15 input	t_{RD}		2.0x – 60		65		40	ns
16	$\overline{RD}$ Low pulse width	t_{RR}	2.0x – 40		85		60		ns
17	$\overline{RD}$ rise→ D0 to 15 Hold	t_{HR}	0		0		0		ns
18	$\overline{RD}$ rise→ A0 to 15output	t_{RAE}	x – 15		48		35		ns
19	$\overline{WR}$ Low pulse width	t_{WW}	2.0x – 40		85		60		ns
20	D0 to 15 Valid→ $\overline{WR}$ rise	t_{DW}	2.0x – 55		70		45		ns
21	$\overline{WR}$ rise →D0 to 15 Hold	t_{WD}	0.5x – 15		16		10		ns
22	A0 to 23 Valid→ $\overline{WAIT}$ input $\left(\begin{smallmatrix}2WAIT\\+n\ mode\end{smallmatrix}\right)$	t_{AWH}		5.5x – 90		254		185	ns
23	A0 to 15 Valid→ $\overline{WAIT}$ input $\left(\begin{smallmatrix}2WAIT\\+n\ mode\end{smallmatrix}\right)$	t_{AWL}		5.0x – 80		223		170	ns
24	$\overline{RD}$/$\overline{WR}$ fall→$\overline{WAIT}$ Hold $\left(\begin{smallmatrix}2WAIT\\+n\ mode\end{smallmatrix}\right)$	t_{CW}	4.0x + 0		250		200		ns
25	A0 to 23 Valid→ PORT input	t_{APH}		2.5x – 120		36		5	ns
26	A0 to 23 Valid→ PORT Hold	t_{APH2}	2.5x + 50		206		175		ns
27	$\overline{WR}$ rise→ PORT Valid	t_{CP}		200		200		200	ns
28	A0 to 23 Valid→ $\overline{RAS}$ fall	t_{ASRH}	1.0x – 40		23		10		ns
29	A0 to 15 Valid→ $\overline{RAS}$ fall	t_{ASRL}	0.5x – 15		16		10		ns
30	$\overline{RAS}$ fall→ D0 to 15 input	t_{RAC}		2.5x – 70		86		55	ns
31	$\overline{RAS}$ fall→ A0 to 15 Hold	t_{RAH}	0.5x – 15		16		10		ns
32	$\overline{RAS}$ Low pulse width	t_{RAS}	2.0x – 40		85		60		ns
33	$\overline{RAS}$ High pulse width	t_{RP}	2.0x – 40		85		60		ns
34	$\overline{CAS}$ fall→ $\overline{RAS}$ rise	t_{RSH}	1.0x – 40		23		10		ns
35	$\overline{RAS}$ rise→ $\overline{CAS}$ rise	t_{RSC}	0.5x – 25		6		0		ns
36	$\overline{RAS}$ fall→ $\overline{CAS}$ fall	t_{RCD}	1.0x – 40		23		10		ns
37	$\overline{CAS}$ fall→ D0 to 15 input	t_{CAC}		1.5x – 65		29		10	ns
38	$\overline{CAS}$ Low pulse width	t_{CAS}	1.5x – 30		64		40		ns

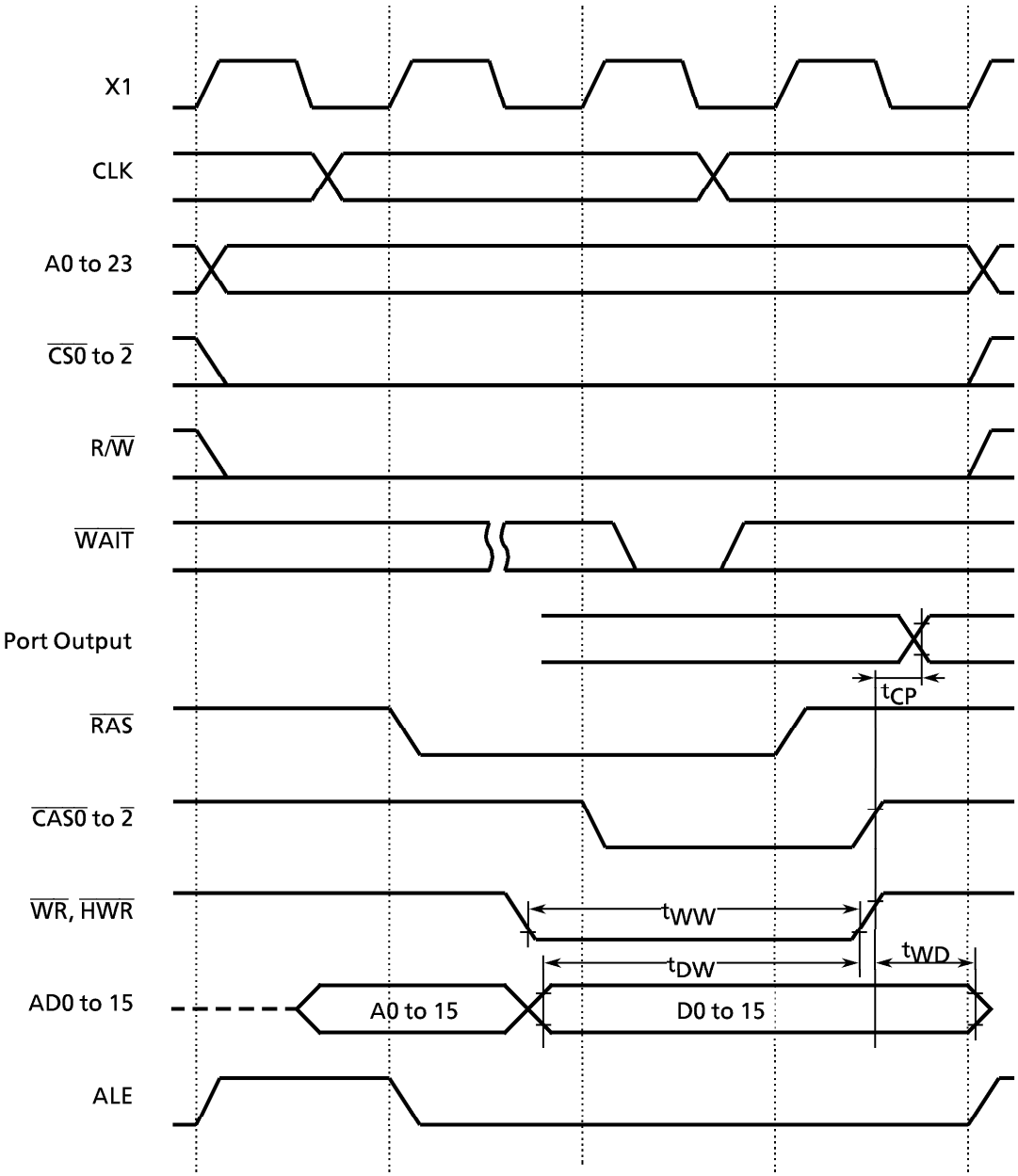
AC Measuring Conditions

- Output Level : High 2.2 V / Low 0.8 V, CL = 50 pF
  (However CL = 100 pF for AD0 to AD15, A0 to A23, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, CLK, $\overline{RAS}$, $\overline{CAS0}$ to $\overline{CAS2}$)
- Input Level : High 2.4 V / Low 0.45 V (AD0 to AD15)
  High 0.8 × V_{CC} / Low 0.2 × V_{CC} (Except for AD0 to AD15)

(1) Read Cycle


X1
CLK
A0 to 23
CS0 to 2
R/W
WAIT
Port Input
RAS
CAS0 to 2
RD
AD0 to 15
ALE
tOSC
tCLK
tAK
tKA
tAWH
tAWL
tCW
tAPH
tAPH2
tASRH
tASRL
tRSH
tRAS
tRAC
tRAH
tRCD
tCAS
tCAC
tRSC
tRP
tADH
tACH
tACL
tLC
tRR
tRD
tADL
tCA
tRAE
tHR
A0 to 15
D0 to 15
tAL
tLA
tLL
tCL

(2) Write Cycle



4.4 AD Conversion Characteristics

$AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS}$

Parameter	Symbol	Power Supply	Min	Typ	Max	Unit
Analog reference voltage (+)	V_{REFH}	V_{CC} = 5 V ± 10%	V_{CC} – 1.5 V	V_{CC}	V_{CC}	V
Analog reference voltage (–)	V_{REFL}		V_{SS}	V_{SS}	V_{SS} + 0.2 V	
Analog input voltage range	V_{AIN}		V_{REFL}		V_{REFH}	
Analog current for analog reference voltage <VREFON> = 1	I_{REF} (V_{REFL} = 0 V)			0.5	1.5	mA
<VREFON> = 0				0.02	5.0	μA
Error (excluding quantizing error)	—			± 1.0	± 3.0	LSB

Note 1 : $1LSB = (V_{REFH} - V_{REFL}) / 2^{10}$

Note 2 : The operation above is guaranteed with $f_{FPH} \geqq 4$ MHz.

Note 3 : The value I_{CC} includes the current which flows through AVCC pin.

4.5 Serial Channel Timing

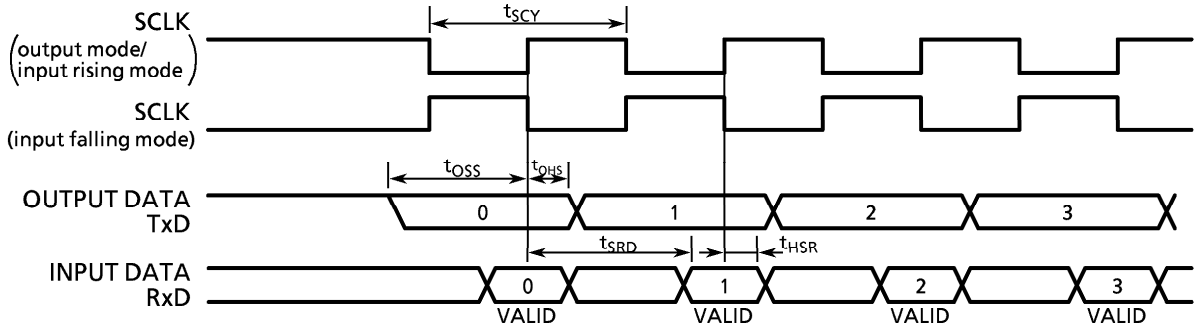
① SCLK Input Mode

Parameter	Symbol	Variable		20 MHz		Unit
		Min	Max	Min	Max	
SCLK cycle	t_{SCY}	16x		0.8		μs
Output Data → SCLK rising/falling timing*	t_{OSS}	$t_{SCY}/2 - 5x - 50$		100		ns
SCLK rising/falling timing* → Output Data hold	t_{OHS}	5x – 100		150		ns
SCLK rising/falling timing* → Input Data hold	t_{HSR}	0		0		ns
SCLK rising/falling timing* → effective data input	t_{SRD}		$t_{SCY} - 5x - 100$		450	ns

*) SCLK rising/falling timing ··· SCLK rising in the rising mode of SCLK, SCLK falling in the falling mode of SCLK.

② SCLK Output Mode

Parameter	Symbol	Variable		20 MHz		Unit
		Min	Max	Min	Max	
SCLK cycle (programmable)	t_{SCY}	16x	8192x	0.8	409.6	μs
Output Data → SCLK rising edge	t_{OSS}	$t_{SCY} - 2x - 150$		550		ns
SCLK rising edge → Output Data hold	t_{OHS}	2x – 80		20		ns
SCLK rising edge → Input Data hold	t_{HSR}	0		0		ns
SCLK rising edge → effective data input	t_{SRD}		$t_{SCY} - 2x - 150$		550	ns



4.6 Timer/Counter Input Clock (TI0, TI4, TI5, TI6, TI7)

Parameter	Symbol	Variable		20 MHz		Unit
		Min	Max	Min	Max	
Clock Cycle	t_{VCK}	8X + 100		500		ns
Low level clock Pulse width	t_{VCKL}	4X + 40		240		ns
High level clock Pulse width	t_{VCKH}	4X + 40		240		ns

4.7 Interrupt and Capture

(1) $\overline{NMI}$, $\overline{INT0}$

Parameter	Symbol	Variable		20 MHz		Unit
		Min	Max	Min	Max	
$\overline{NMI}$, $\overline{INT0}$ Low level Pulse width	t_{INTAL}	4X		200		ns
$\overline{NMI}$, $\overline{INT0}$ High level Pulse width	t_{INTAH}	4X		200		ns

(2) INT4 to 9

INT4 to 9 input pulse width depends on the operation clock of CPU and Timer (9 bit prescaler). The following shows the pulse width for each clock.

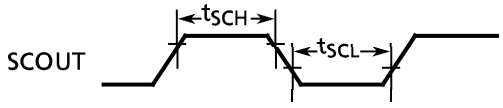
Clock selection for Prescaller <PRCK1, 0>	t_{INTBL} (INT4 to 9 Low level Pulse width)		t_{INTBH} (INT4 to 9 High level Pulse width)		Unit
	Variable	20 MHz	Variable	20 MHz	
	Min	Min	Min	Min	
00 (f_{FPH})	8X + 100	500	8X + 100	500	ns
10(fc/16)	128X + 0.1	6.5	128X + 0.1	6.5	μs

4.8 SCOUT pin AC characteristics

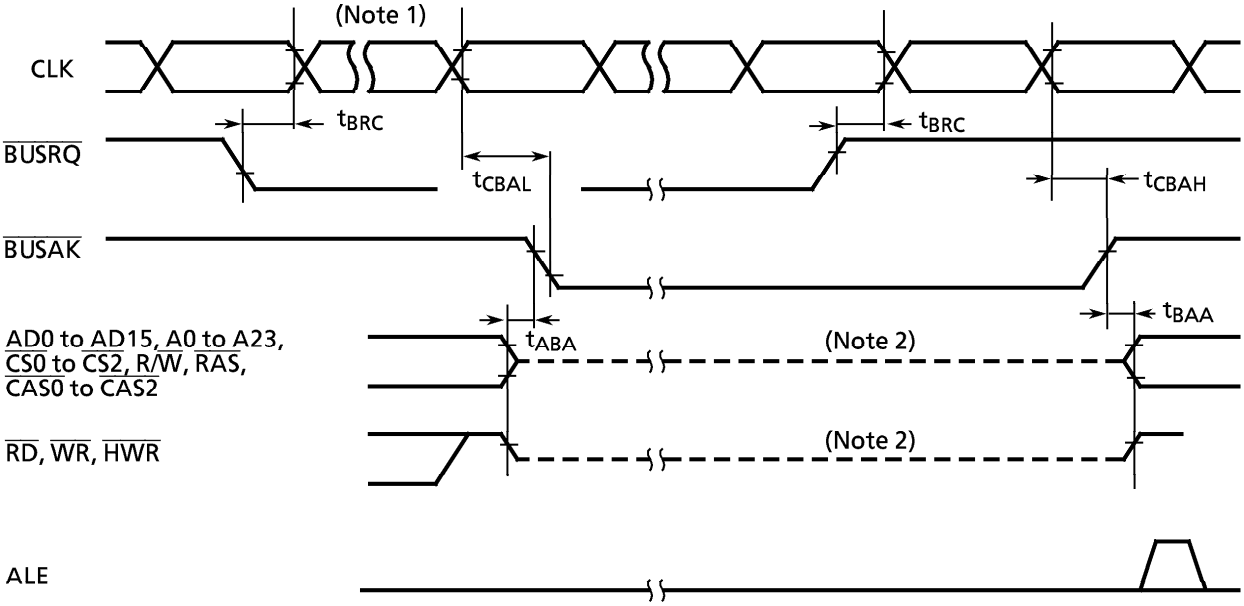
Parameter	Symbol	Variable		20 MHz	
		Min	Max	Min	Max
High-level pulse width VCC = 5V ± 10%	t_{SCH}	0.5X–10		15	
Low-level pulse width VCC = 5V ± 10%	t_{SCL}	0.5X–10		15	

Measurement condition

- Output level : High 2.2 V / Low 0.8 V, CL = 10 pF



4.9 Timing Chart for Bus Request/Bus Acknowledge



Parameter	Symbol	Variable		20 MHz		Unit
		Min	Max	Min	Max	
$\overline{BUSRQ}$ set-up time to CLK	t_{BRC}	120		120		ns
CLK→ $\overline{BUSAK}$ falling edge	t_{CBAL}		1.5x + 120		195	ns
CLK→ $\overline{BUSAK}$ rising edge	t_{CBAH}		0.5x + 40		65	ns
Output Buffer is off to $\overline{BUSAK}$	t_{ABA}	0	80	0	80	ns
$\overline{BUSAK}$ to Output Buffer is on.	t_{BAA}	0	80	0	80	ns

Note 1: The Bus will be released after the $\overline{WAIT}$ request is inactive, when the $\overline{BUSRQ}$ is set to "0" during "Wait" cycle.

Note 2: This line only shows the output buffer is off-state.
It doesn't indicate the signal level is fixed.
Just after the bus is released, the signal level which is set before the bus is released is kept dynamically by the external capacitance. Therefore, to fix the signal level by an external resistor during bus releasing, designing is executed carefully because the level-fix will be delayed.
The internal programmable pull-up / pull-down resistor is switched active / non-active by an internal signal.