

August 1997

## 6-Bit, 20 MSPS, Video A/D Converter (CMOS)

### Features

- Resolution ..... 6-Bit
- Maximum Sampling Frequency ..... 20 MSPS
- Low Power Consumption at 20 MSPS (Typ)  
(Reference Current Excluded) .....40mW
- Built-In Sample and Hold Circuit
- Three-State TTL Compatible Output
- Power Supply .....5V Single
- Low Input Capacitance .....4pF
- Reference Impedance .....250Ω (Typ)

### Applications

- Video Digitizing
- Wireless Communications

### Description

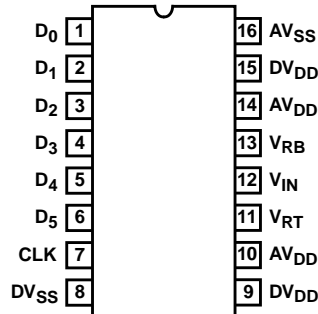
HI1172 is a 6-bit, CMOS A/D converter for video use. The adoption of a 2-step parallel conversion achieves speeds of 20 MSPS minimum, 35 MSPS typical.

### Ordering Information

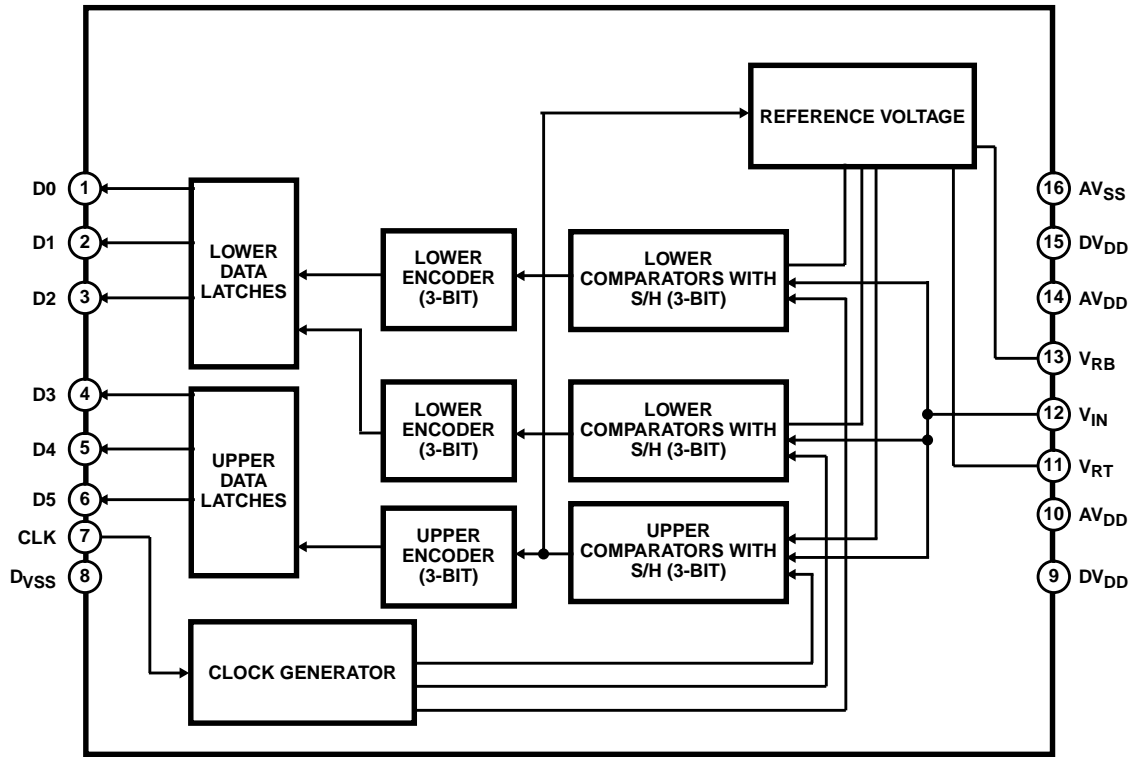
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI1172JCP	-20 to 75	16 Ld PDIP	E16.3A-S
HI1172JCB	-20 to 75	16 Ld SOIC	M16.2-S

### Pinout

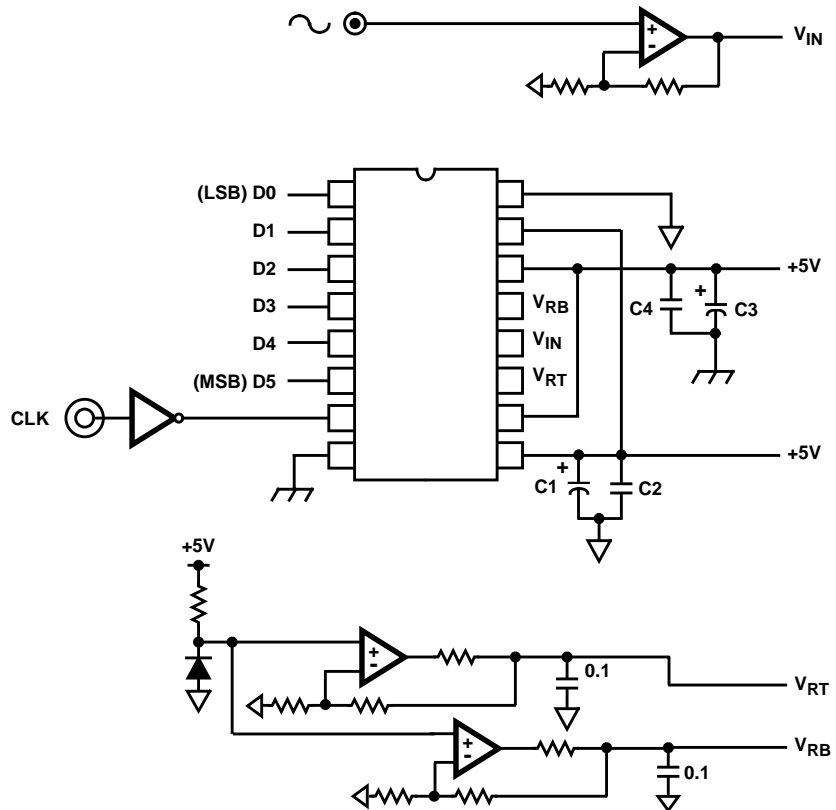
HI1172  
(PDIP, SOIC)  
TOP VIEW



**Functional Block Diagram**



**Typical Application Circuit**



**Pin Descriptions**

NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1 to 6	D0 to D5		D0 (LSB) to D5 (MSB) Output.
7	CLK		Clock Input.
8	DVSS		Digital GND.
9, 15	DVDD		Digital +5V.
10, 14	AVDD		Analog +5V.
11	V <sub>RT</sub>		Reference Voltage (Top).
13	V <sub>RB</sub>		Reference Voltage (Bottom).
12	V <sub>IN</sub>		Analog Input.
16	AVSS		Analog GND.

# HI1172

## Absolute Maximum Ratings $T_A = 25^\circ\text{C}$

Supply Voltage ( $V_{DD}$ )	7V
Reference Voltage ( $V_{RT}, V_{RB}$ )	$V_{DD}$ to $V_{SS}$
Analog Input Voltage ( $V_{IN}$ )	$V_{DD}$ to $V_{SS}$
Digital Input Voltage (CLK)	$V_{DD}$ to $V_{SS}$
Digital Output Voltage ( $V_{OH}, V_{OL}$ )	$V_{DD}$ to $V_{SS}$

## Operating Conditions

Supply Voltage Range, $AV_{DD}, AV_{SS}$	4.75V to 5.25V
Reference Voltage, $DV_{DD}, DV_{SS}$	
$V_{RT}$	0.9V to 5V
$V_{RB}$	0V to 4.1V
$V_{RT} - V_{RB}$	0.9V to $AV_{DD}$
Analog Input Voltage ( $V_{IN}$ )	$V_{RB}$ to $V_{RT}$
Clock Pulse Width	
$t_{PW1}$	25ns (Min)
$t_{PW0}$	25ns (Min)
Temperature Range	$-20^\circ\text{C}$ to $75^\circ\text{C}$

## Thermal Information

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ ( $^\circ\text{C}/\text{W}$ )
SOIC Package	120
PDIP Package	94
Maximum Junction Temperature (Plastic Package)	$150^\circ\text{C}$
Maximum Storage Temperature Range	$-65^\circ\text{C}$ to $150^\circ\text{C}$
Maximum Lead Temperature (Soldering 10s)	$300^\circ\text{C}$ (SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications $V_{DD} = +5\text{V}, V_{RB} = 1\text{V}, V_{RT} = 2\text{V}, T_A = 25^\circ\text{C}$

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Conversion Speed, $f_C$	$f_C$	$V_{IN} = 1\text{V}$ to $2\text{V}$ $f_{IN} = 1\text{kHz}$ Ramp		0.5	-	20	MSPS
Integral Non-Linearity	$E_L$	$f_C = 20$ MSPS $V_{IN} = 1\text{V}$ to $2\text{V}$		-	$\pm 0.3$	$\pm 0.5$	LSB
Differential Non-Linearity	$E_D$	$f_C = 20$ MSPS $V_{IN} = 1\text{V}$ to $2\text{V}$		-	$\pm 0.3$	$\pm 0.5$	LSB
Supply Current	$I_{DD}$	$f_C = 20$ MSPS NTSC Ramp Wave Input		-	7	12	mA
Reference Pin Current	$I_{REF}$			3	4	5.7	mA
Analog Input (-1dB)	BW			-	18	-	MHz
Analog Input Capacitance	$C_{IN}$	$V_{IN} = 1.5\text{V} + 0.07V_{RMS}$		-	4	-	pF
Reference Resistance ( $V_{RT}$ to $V_{RB}$ )	$R_{REF}$			175	250	325	$\Omega$
Offset Voltage	$E_{OT}$			0	-20	-40	mV
	$E_{OB}$			15	35	55	mV
Digital Input Voltage	$V_{IH}$			4.0	-	-	V
	$V_{IL}$			-	-	1.0	V
Digital Input Current	$I_{IH}$	$V_{DD} = \text{Max}$	$V_{IH} = V_{DD}$	-	-	5	$\mu\text{A}$
	$I_{IL}$		$V_{IL} = 0\text{V}$	-	-	5	$\mu\text{A}$
Digital Output Current	$I_{OH}$	$V_{DD} = \text{Min}$	$V_{OH} = V_{DD} = 0.5\text{V}$	-1.1	-	-	mA
	$I_{OL}$		$V_{OL} = 0.4\text{V}$	3.7	-	-	mA
Output Data Delay	$T_{DL}$	With TTL 1 Gate and 10pF Load		-	18	30	ns
Differential Gain Error	DG	NTSC 40 IRE Mod		-	1.0	-	%
Differential Phase Error	DP	Ramp, $f_C = 14.3$ MSPS		-	1.0	-	deg
Aperture Jitter	$t_{AJ}$			-	40	-	ps
Sampling Delay	$t_{SD}$			-	4	-	ns

Test Circuits

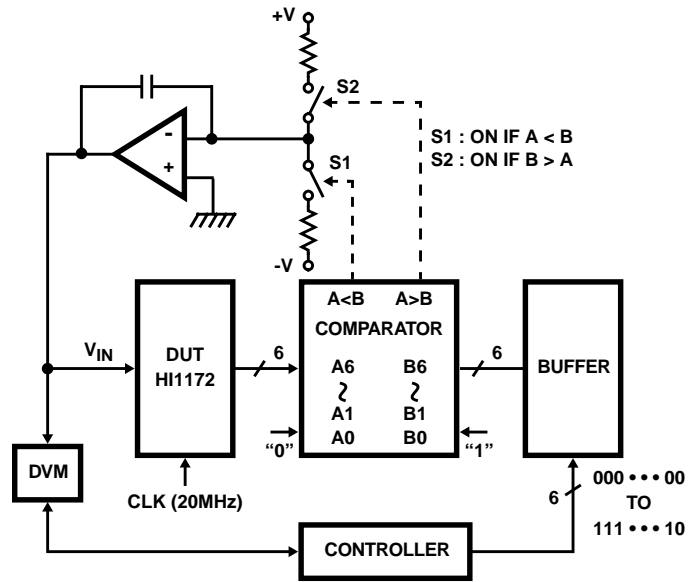


FIGURE 1. INTEGRAL NON-LINEARITY ERROR, DIFFERENTIAL NON-LINEARITY, OFFSET VOLTAGE

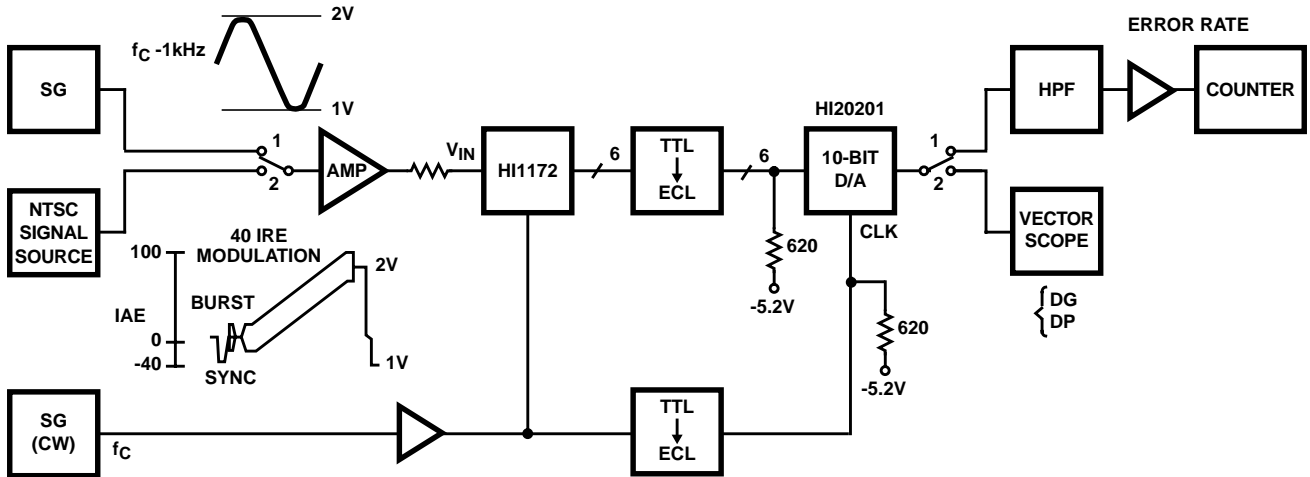


FIGURE 2. MAXIMUM OPERATIONAL SPEED, DIFFERENTIAL GAIN ERROR, DIFFERENTIAL PHASE ERROR

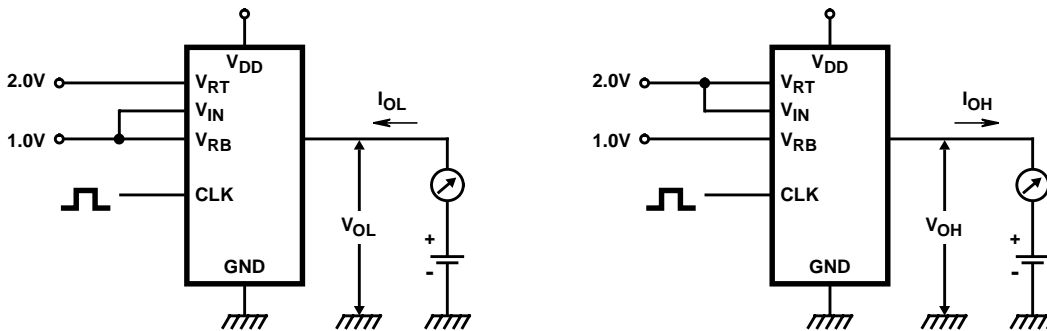


FIGURE 3. DIGITAL OUTPUT CURRENT TEST CIRCUIT

Timing Diagrams

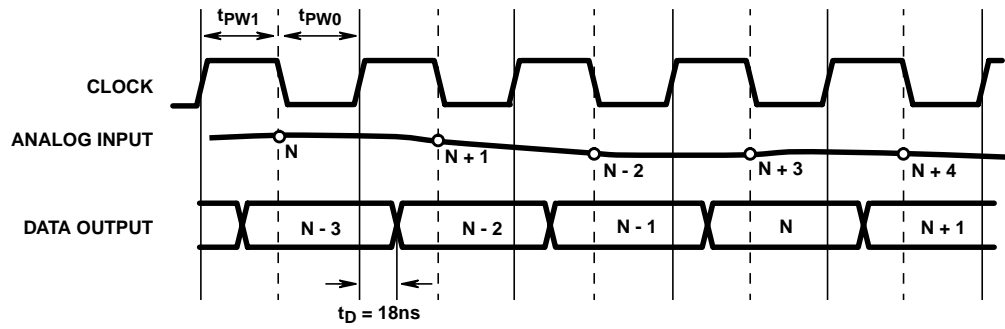


FIGURE 4. TIMING CHART 1

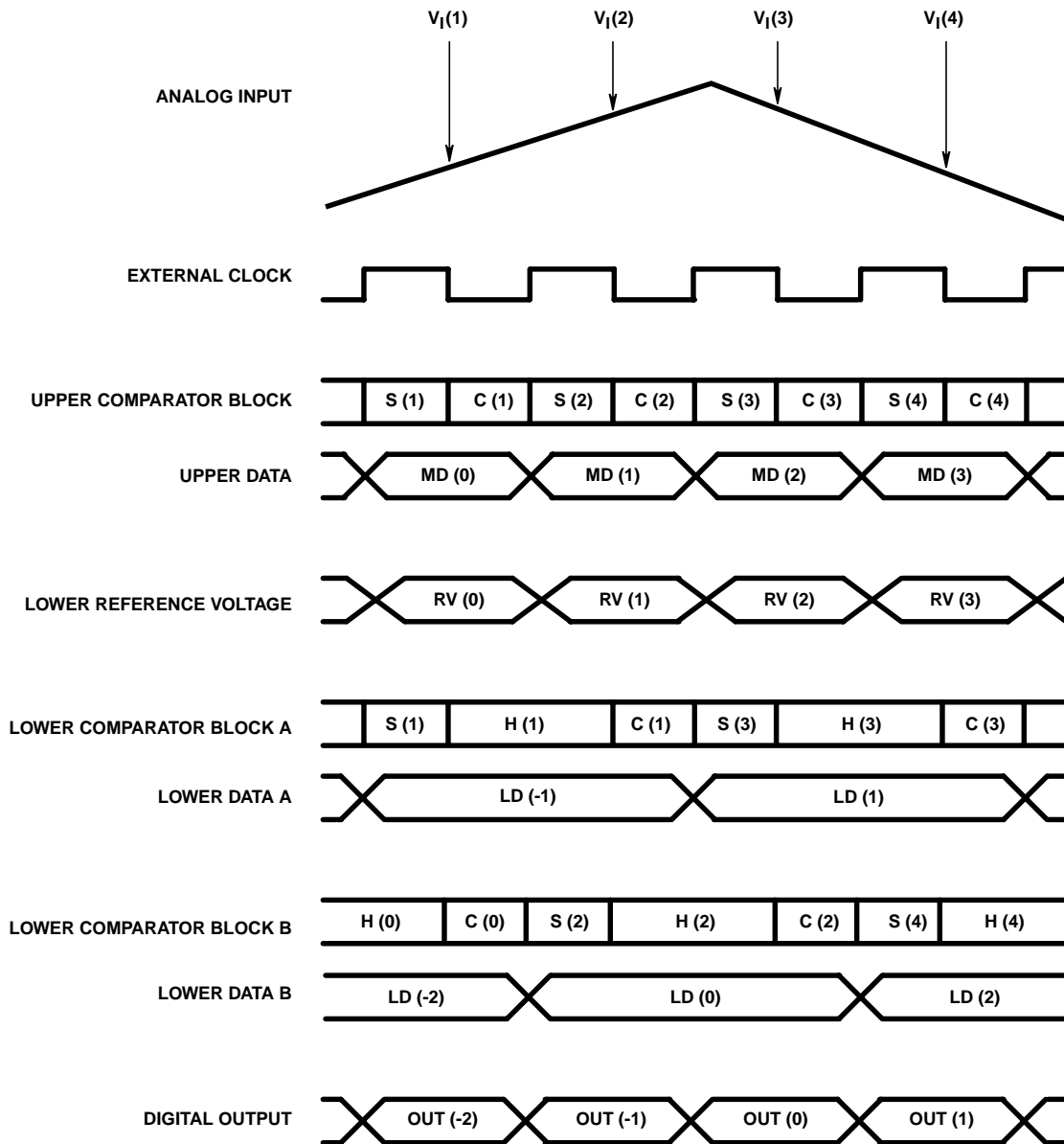


FIGURE 5. TIMING CHART 2

## Digital Output

Compatibility between analog input voltage and the digital output code is indicated in the chart below.

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE					
		MSB			LSB		
$V_{RT}$	0	1	1	1	1	1	1
•	•				•		
•	•				•		
•	•				•		
•	31	1	0	0	0	0	1
•	32	0	1	1	1	1	1
•	•				•		
•	•				•		
•	•				•		
$V_{RB}$	63	0	0	0	0	0	0

## Operation (See Block Diagram and Waveform)

The HI1172 is a 2-step parallel system A/D converter featuring a 3-bit upper comparators group and 2 lower comparators groups of 3-bit each. The reference voltage that is equal to the voltage between  $V_{RT}$ - $V_{RB}/8$  is constantly applied to the upper 3-bit comparator block. Voltage that corresponded to the upper data is fed through the reference supply to the lower data.

This IC uses an offset cancel type comparator and operates synchronously with an external clock. It features the following operating modes which are respectively indicated on the timing chart with S, H, C symbols, i.e., input sampling (auto zero) mode, input hold mode and comparison mode.

The operation of respective parts is as indicated in the chart. Input voltage  $V_i$  (1) is sampled with the falling edge of the first clock by means of the upper comparator block and the lower comparator A block.

The upper comparators block finalizes comparison data MD (1) with the rising edge of the first clock. simultaneously the reference supply generates the lower reference voltage RV (1) that corresponded to the upper results. The lower comparator block finalizes comparison data LD (1) with the rising edge of the second clock. MD (1) and LD (1) are combined and output as Out (1) with the rising edge of the 3rd clock. Accordingly there is a 2.5 clock delay from the analog input sampling point to the digital data output.

## Notes On Operation

- $V_{DD}$ ,  $V_{SS}$  - To reduce noise effects, separate the analog and digital systems close to the device. For both the digital and analog  $V_{DD}$  pins, use a ceramic capacitor of about 0.1 $\mu$ F set as close as possible to the pin to bypass to the respective GNDs.
- Analog Input - Compared with a flash type A/D converter, the input capacitance of the analog input is rather small. However it is necessary to drive with an amplifier featuring sufficient bandwidth and drive capability. When driving with an amplifier of low output impedance, parasitic oscillation may occur. That may be prevented by inserting a resistance of about 100 $\Omega$  in series between the amplifier output and A/D input.
- Clock Input - The clock line wiring should be as short as possible. Also, to avoid any interference with other signals, separate it from the other circuits.
- Reference Input - Voltage between  $V_{RT}$  to  $V_{RB}$  is compatible with the dynamic range of the analog input. By bypassing  $V_{RT}$  and  $V_{RB}$  pins to GND with a capacitor of about 0.1 $\mu$ F, stable characteristics are obtained.
- Timing - Analog input is sampled with the falling edge of CLK and output as digital data with a delay of 2.5 clocks and with the following rising edge. The delay from the clock rising edge to the data output is about 18ns.
- About Latch Up - It is necessary that  $AV_{DD}$  and  $DV_{DD}$  pins to be the common source of power supply. This is to avoid latch up due to the voltage difference between  $AV_{DD}$  and  $DV_{DD}$  pins when power is ON.

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