



LC86P6548

8-Bit Single Chip Microcontroller with One-Time Programmable PROM

Preliminary

Overview

The LC86P6548 is a CMOS 8-bit single chip microcontroller with one-time PROM for the LC866500 series. This microcontroller has the function and the pin description of the LC866500 series mask ROM version, and 48K-byte PROM.

Features

- (1) Option switching by PROM data

The option function of the LC866500 series can be specified by the PROM data.

LC86P6548 can be checked the function of the trial pieces using the mass production board.

- (2) Internal one-time PROM capacity : 49408 bytes
 (3) Internal RAM capacity : 1152 bytes

Used PROM or RAM capacity are equal ROM or RAM capacity of mask ROM version which applies LC86P6548.

| Mask ROM version | PROM capacity | RAM capacity |
|------------------|---------------|--------------|
| LC866548 | 49152 bytes | 1152 bytes |
| LC866540 | 40960 bytes | 1152 bytes |
| LC866532 | 32768 bytes | 1152 bytes |
| LC866528 | 28672 bytes | 896 bytes |
| LC866524 | 24576 bytes | 896 bytes |

Programming service

We offers various services at nominal charges. These include the ROM writing, the ROM reading, the package stamping and the screening. Contact our representative for further information.

- Any and all SANYO products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO representative nearest you before using any SANYO products described or contained herein in such applications.
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LC86P6548

- (4) Operating supply voltage : 4.5V to 6.0V
- (5) Instruction cycle time : 1.0 μ s to 366 μ s
- (6) Operating temperature : -30°C to +70°C
- (7) The pin and the package compatible with the LC866500 series mask ROM devices
- (8) Applicable mask ROM version : LC866548/LC866540//LC866532/LC866528/LC866524

Notice for use

LC86P6548 is provided for the first release and small shipping of the LC866500 series.
At using, take notice of the followings.

- (1) A point of difference LC86P6548 and LC866500 series

| Item | LC86P6548 | LC866548/40/32/28/24 |
|--------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Operation after reset releasing | The option is specified until 3ms after going to a 'H' level to the reset terminal by dgreees. The program is executed from 00H of the program counter. | The program is executed from 00H of the program counter immediately after going to a 'H' level to reset terminal. |
| Pull-down resistor of the following pins •S0/T0 – S6/T6 •S7/T7 – S15/T15 •S16 – S31 •S32 – S47 •S48 – S51 | Pull-down resistor provided/not provided Not provided Provided (fixed) Provided (fixed) Not provided Not provided | Pull-down resistor provided/not provided Specified by the option Provided (fixed) Specified by the option Specified by the option Not provided |
| Power dissipation | Refer to 'electrical characteristics' on the semiconductor news. | |

LC86P6548 uses 256 bytes that is addressed on FF00H to FFFFH in the program memory as the option configuration data area. This option configuration cannot execute all options which LC866500 series have. Next tables show the options that correspond and not correspond to LC86P6548.

- A kind of the option corresponding of the LC86P6548

| A kind of option | Pins, Circuits | Contents of the option |
|-----------------------------------------|------------------------------------|-----------------------------------------------------------------------------|
| Input/output form of Input/output ports | Port 0 | 1. N-channel open drain output |
| | | 2. CMOS output *1 |
| | 3. Pull-up MOS Tr. provided | |
| | 4. Pull-up MOS Tr. not provided *2 | |
| | Port 1 | 1. Input : Programmable pull-up MOS Tr. Output : N-channel open drain |
| | *1 | 2. Input : Programmable pull-up MOS Tr. Output : CMOS |
| | Port 3 | 1. Input : No Programmable pull-up MOS Tr. Output : N-channel open drain |
| | *1 | 2. Input : Programmable pull-up MOS Tr. Output : CMOS |

*1) Specified in a bit

*2) Specified in nibble unit. The port of N-channel open drain output does not have the Pull-up MOS Tr..

- A kind of the option not corresponding of the LC86P6548

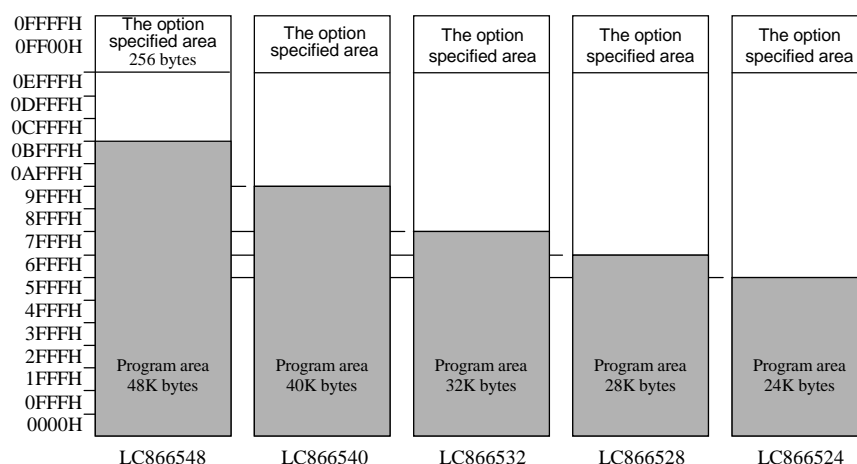
| A kind of option | Pins, Circuits | LC86P6548 | LC866548/40/32/28/24 |
|----------------------------------------|--------------------------------|----------------------------------|----------------------------------------------------|
| Pull-down resistor of the high voltage | •S0/T0 to S6/T6 •S16 to S31 | Not provided Provided (fixed) | Specified by the option Specified by the option |
| Withstand output terminals | •S32 to S47 | Not provided | Specified by the option |

(2) Option

The option data is created by the option specified program “SU86K.EXE”. The created option data is linked to the program area by linkage loader “L86K.EXE”.

(3) ROM space

LC86P6548 and LC866500 series use 256 bytes that is addressed on 0FF00H to 0FFFFH in the program memory as the option specified data area. These program memory capacity are 49152 bytes that is addressed on 0000H to BFFFH.



(4) Ordering information

1. When ordering the identical mask ROM and PROM devices simultaneously.
Provide an EPROM containing the target memory contents together with the separate order forms for each of the mask ROM and PROM versions.
2. When ordering a PROM device.
Provide an EPROM containing the target memory contents together with an order form.

How to use

(1) Specification of option

Programming data for PROM of the LC86P6548 is required.

Debugged evaluation file (EVA file) must be converted to an INTEL-HEX formatted file (HEX file) with file converter program, EVA2HEX.EXE. The HEX file is used as the programming data for the LC86P6548.

(2) How to program for the PROM

LC86P6548 can be programmed by the EPROM programmer with attachment ; W86EP6548Q.

- Recommended EPROM programmer

| Producter | EPROM programmer |
|--------------------|---------------------|
| Advantest | R4945, R4944, R4943 |
| Andou | AF-9704 |
| AVAL | PKW-1100, PKW-3000 |
| Minato electronics | MODEL 1890A |

- “27512 (Vpp=12.5V) Intel high speed programming” mode available. The address must be set to “0 to 0FFFFH” and a jumper (DASEC) must be set to ‘OFF’ at programming.

(3) How to use the data security function

“Data security” is the disabled function to read the data of the PROM.

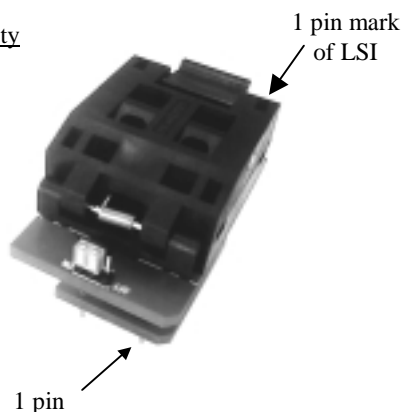
The following is the process in order to execute the data security.

1. Set ‘ON’ the jumper of attachment.
2. Program again. Then EPROM programmer displays the error. The error means normally activity of the data security. It is not a trouble of the EPROM programmer or the LSI.

Notes

- Data security is not executed when the data of all address have ‘FFH’ at the sequence 2 above.
- The programming by a sequential operation “BLANK⇒PROGRAM⇒VERIFY” cannot be executed data security at the sequence 2 above.
- Set to ‘OFF’ the jumper after executing the data security.

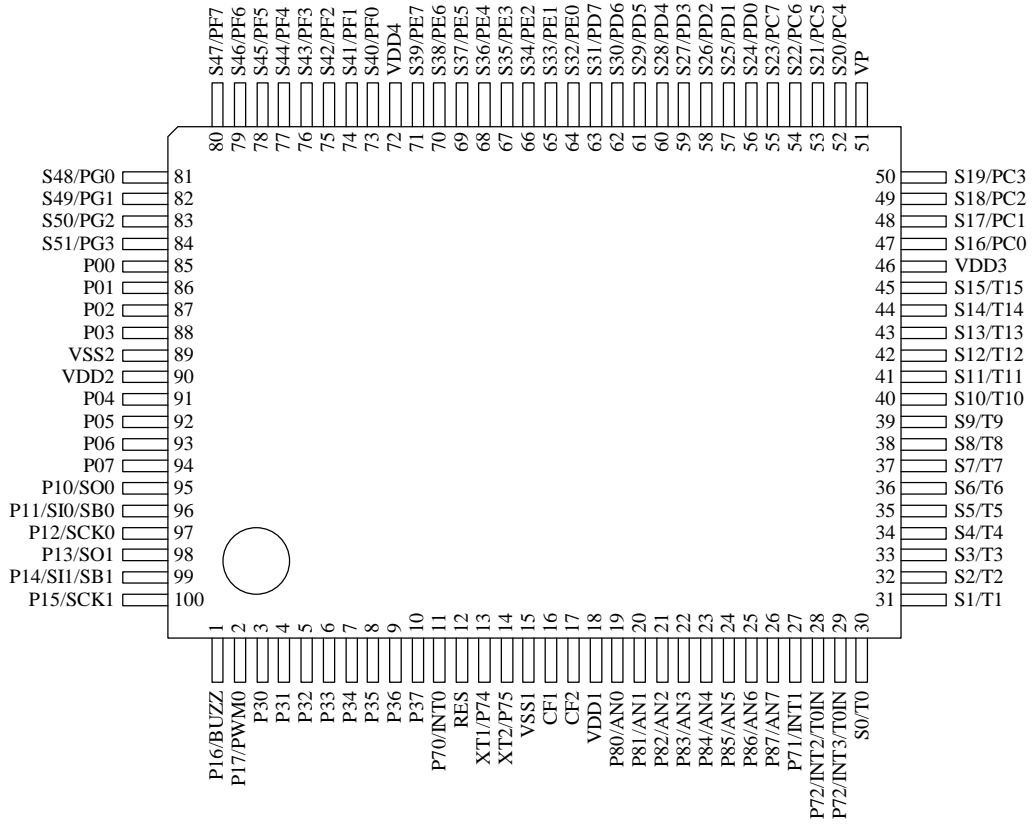
Data security



Not data security

W86EP6548Q

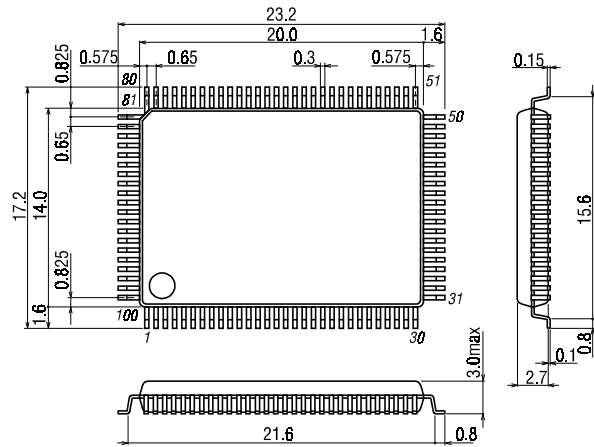
Pin Assignment



Package Dimension

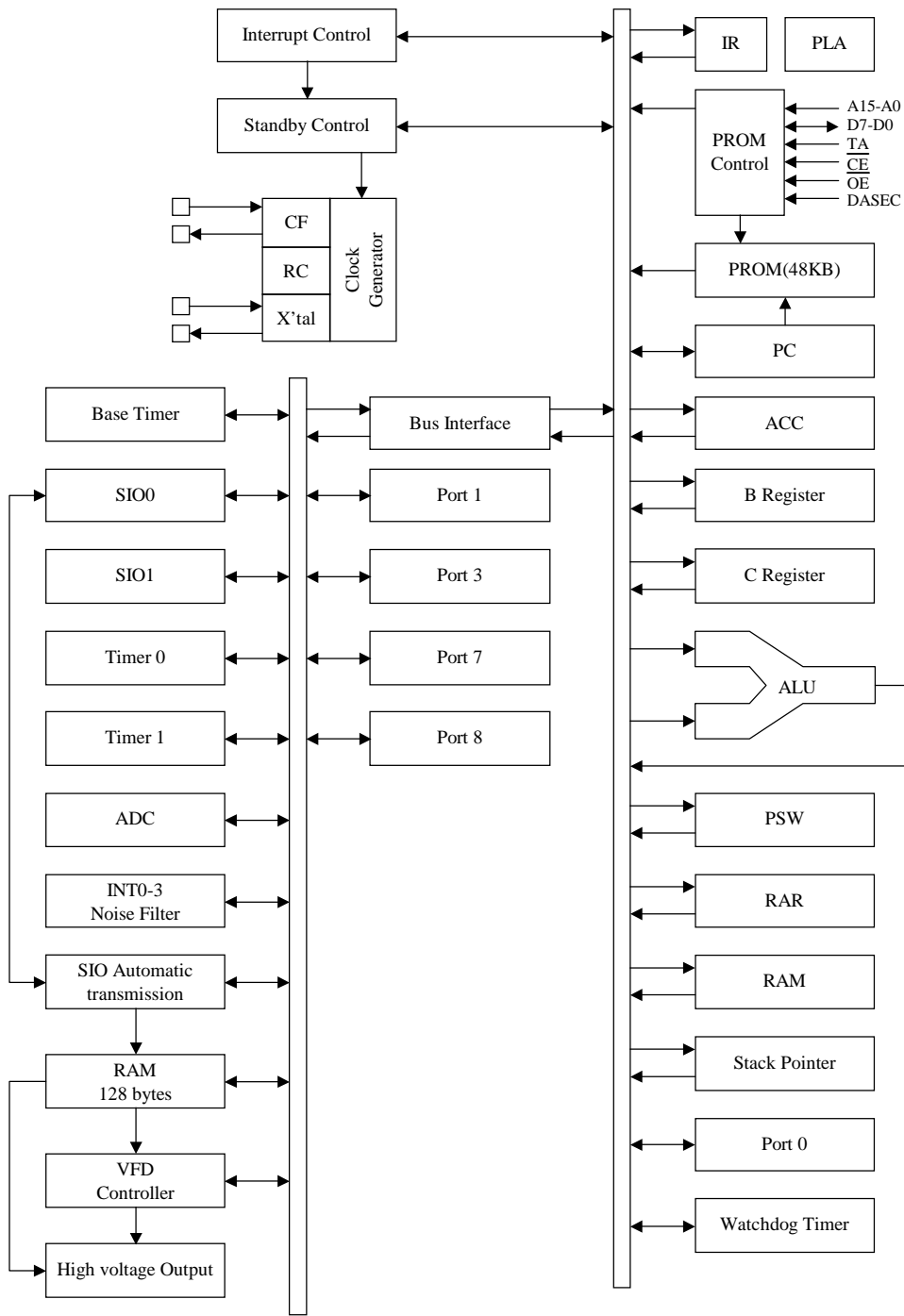
(unit : mm)

3151



SANYO : QIP-100E

System Block Diagram



LC86P6548 Pin Description

| Pin name | I/O | Function description | Option | PROM mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------------------------------------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|-----------|------------------|------------|-----------|--------|------|--------|--------|---------|--------|--------|-----|------|--------|--------|---------|--------|--------|-----|------|--------|--------|--------|---------|---------|-----|------|--------|--------|--------|---------|---------|-----|--|------------------------------------------------------------------------------------|
| VSS1,2 | - | Power pin (-) *4 | - | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VDD1,2,3,4 | - | Power pin (+) *4 | - | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VP | - | Power pin (+) for the VFD output pull-down resist | - | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PORT0 P00 to P07 | I/O | <ul style="list-style-type: none"> •8-bit input/output port •Input for port 0 interrupt •Input/output in nibble units •Input for HOLD release •15V withstand at N-channel open drain output | <ul style="list-style-type: none"> •Pull-up resistor : Provided/Not provided (each nibble) •Output form : CMOS/N-channel open drain (each bit) | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PORT1 P10 to P17 | I/O | <ul style="list-style-type: none"> •8-bit input/output port •Input/output can be specified in a bit unit •Other pin functions P10 SIO0 data output P11 SIO0 data input/bus input/output P12 SIO0 clock input/output P13 SIO1 data output P14 SIO1 data input/bus input/output P15 SIO1 clock input/output P16 Buzzer output P17 Timer 1 output (PWM0 output) | <ul style="list-style-type: none"> •Output form : CMOS/N-channel open drain (each bit) | Data line D0 to D7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PORT3 P30 to P37 | I/O | <ul style="list-style-type: none"> •8-bit input/output port •Input/output in bit unit •15V withstand at N-channel open drain output | <ul style="list-style-type: none"> •Output form : CMOS/N-channel open drain (each bit) | - | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PORT7 P70 to P73 $\overline{P74}$ to P75 | I/O I | <ul style="list-style-type: none"> •4-bit input/output port •Input/output in bit unit •2-bit input port •Other pin functions P70 : INT0 input/HOLD release/N-channel Tr. output for watchdog timer P71 : INT1 input/HOLD release input P72 : INT2 input/timer 0 event input P73 : INT3 input with noise filter/timer 0 event input $\overline{P74}$: 32.768kHz crystal oscillation terminal XT1 P75 : 32.768kHz crystal oscillation terminal XT2 •Interrupt received forms, the vector addresses <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 5px;"> <thead> <tr> <th></th> <th>rising</th> <th>falling</th> <th>rising & falling</th> <th>high level</th> <th>low level</th> <th>vector</th> </tr> </thead> <tbody> <tr> <td>INT0</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> <td>03H</td> </tr> <tr> <td>INT1</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> <td>0BH</td> </tr> <tr> <td>INT2</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> <td>13H</td> </tr> <tr> <td>INT3</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> <td>1BH</td> </tr> </tbody> </table> | | rising | falling | rising & falling | high level | low level | vector | INT0 | enable | enable | disable | enable | enable | 03H | INT1 | enable | enable | disable | enable | enable | 0BH | INT2 | enable | enable | enable | disable | disable | 13H | INT3 | enable | enable | enable | disable | disable | 1BH | | PROM control signals DASEC (*1) \overline{OE} (*2) \overline{CE} (*3) |
| | rising | falling | rising & falling | high level | low level | vector | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| INT0 | enable | enable | disable | enable | enable | 03H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| INT1 | enable | enable | disable | enable | enable | 0BH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| INT2 | enable | enable | enable | disable | disable | 13H | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| INT3 | enable | enable | enable | disable | disable | 1BH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Continue.

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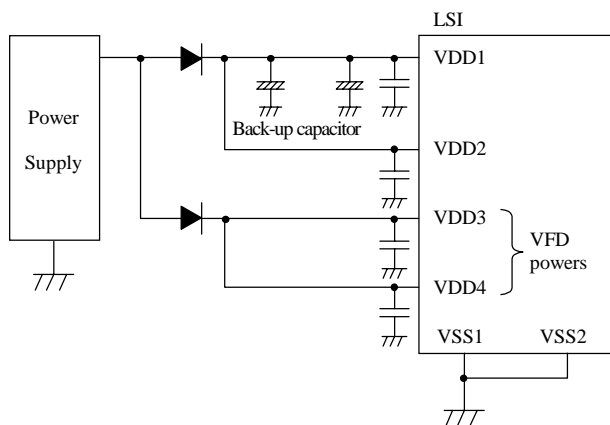
| Pin name | I/O | Function description | Option | PROM mode |
|---------------------------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------------------------|
| PORT8 P80 to 83 P84 to 87 | I I/O | <ul style="list-style-type: none"> •4-bit input port •Input/output in bit unit •4-bit input port •Other function AD input port (8 port pins) | - | - |
| S0/T0 to S6/T6 *6 | O | Output for VFD display controller segment/timing in common | - | - |
| S7/T7 to S15/T15 *7 | O | <ul style="list-style-type: none"> •Output for VFD display controller segment/timing with internal pull-down resistor in common •Internal pull-down resistor output | - | TA (*5) |
| S16 to S31 *8 | I/O | <ul style="list-style-type: none"> •Output for VFD display controller Segment output •Other function S16 : High voltage input port PC0 S17 : High voltage input port PC1 S18 : High voltage input port PC2 S19 : High voltage input port PC3 S20 : High voltage input port PC4 S21 : High voltage input port PC5 S22 : High voltage input port PC6 S23 : High voltage input port PC7 S24 : High voltage input port PD0 S25 : High voltage input port PD1 S26 : High voltage input port PD2 S27 : High voltage input port PD3 S28 : High voltage input port PD4 S29 : High voltage input port PD5 S30 : High voltage input port PD6 S31 : High voltage input port PD7 | - | •Address input A15 to A0 |
| S32 to S47 *9 | I/O | <ul style="list-style-type: none"> •Output for VFD display controller Segment •Other function S32 : High voltage input port PE0 S33 : High voltage input port PE1 S34 : High voltage input port PE2 S35 : High voltage input port PE3 S36 : High voltage input port PE4 S37 : High voltage input port PE5 S38 : High voltage input port PE6 S39 : High voltage input port PE7 S40 : High voltage I/O port PF0 S41 : High voltage I/O port PF1 S42 : High voltage I/O port PF2 S43 : High voltage I/O port PF3 S44 : High voltage I/O port PF4 S45 : High voltage I/O port PF5 S46 : High voltage I/O port PF6 S47 : High voltage I/O port PF7 | - | - |

Continue.

| Pin name | I/O | Function description | Option | PROM mode |
|-----------------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-----------|
| S48 to S51 *9 | I/O | <ul style="list-style-type: none"> •Output for VFD display controller Segment •Other function S48 : High voltage I/O port PG0 S49 : High voltage I/O port PG1 S50 : High voltage I/O port PG2 S51 : High voltage I/O port PG3 | - | - |
| RES | I | Reset pin | - | - |
| XT1/ $\overline{P74}$ | I | <ul style="list-style-type: none"> •Input pin for 32.768kHz crystal oscillation •Other function XT1 : Input port $\overline{P74}$ In case of non use, connect to VDD1. | - | - |
| XT2/P75 | O | <ul style="list-style-type: none"> •Output pin for 32.768kHz crystal oscillation •Other function XT2 : Input port P75 In case of non use, connect to VDD1 at using as port or unconnect at using as oscillation. | - | - |
| CF1 | I | Input pin for the ceramic resonator oscillation | - | - |
| CF2 | O | Output pin for the ceramic resonator oscillation | - | - |

◆ All of port options (except pull-up resistor of port 0) can be specified in bit unit.

- *1 Memory select input for data security
- *2 Output enable input
- *3 Chip enable input
- *4 Connect like the following figure to reduce noise into a VDD1 terminal.
Shorted the VSS1 terminal to the VSS2 terminal and to make the back-up time long.
- *5 TA → PROM control signal input
- *6 S0/T0 to S6/T6 : not provided the pull-down resistor
- *7 S7/T7 to S15/T15 : provided the pull-down resistor (fixed)
- *8 S16 to S31 : provided the pull-down resistor (fixed)
- *9 S32 to S51 : not provided the pull-down resistor



1. Absolute Maximum Ratings at VSS1=VSS2=0V and Ta=25°C

| Parameter | Symbol | Pins | Conditions | Ratings | | | unit | | |
|-----------------------------|---------------------------------------|------------------------------------------------------------------------------------------|------------------------------------------|-------------------------------|--------|------|-------------|------|----|
| | | | | VDD[V] | min. | typ. | | max. | |
| Supply voltage | VDDMAX | VDD1, VDD2 VDD3, VDD4 | VDD1=VDD2 =VDD3=VDD4 | | -0.3 | | +7.0 | V | |
| Input voltage | VI(1) | •Ports $\overline{74}, 75$ •Ports 80,81,82,83 •Port 8 • \overline{RES} | | | -0.3 | | VDD+ 0.3 | | |
| | VI(2) | VP | | | VDD-45 | | VDD+ 0.3 | | |
| Output voltage | VO(1) | S0/T0 to S15/T15 | | | VDD-45 | | VDD+ 0.3 | | |
| Input/Output voltage | VIO(1) | •Port 1 •Ports 70,71,72,73 •Ports 84,85,86,87 •Ports 0, 3 at CMOS output option | | | -0.3 | | VDD+ 0.3 | | |
| | VIO(2) | Ports 0, 3 at N-ch open drain output option | | | -0.3 | | 15 | | |
| | VIO(3) | S16 to S51 | | | VDD-45 | | VDD+ 0.3 | | |
| High level output current | Peak output current | IOPH(1) | Ports 0, 1, 3 | •CMOS output •At each pins | | | -10 | | mA |
| | | IOPH(2) | S0/T0 to S15/T15 | At each pins | | | -30 | | |
| | | IOPH(3) | S16 to S51 | At each pins | | | -15 | | |
| | Total output current | Σ IIOAH(1) | Port 0 | The total of all pins | | | -30 | | |
| | | Σ IIOAH(2) | Ports 1, 3 | The total of all pins | | | -30 | | |
| | | Σ IIOAH(3) | S0/T0 to S15/T15 | The total of all pins | | | -55 | | |
| | | Σ IIOAH(4) | S16 to S27 | The total of all pins | | | -60 | | |
| Σ IIOAH(5) | S28to S39 | The total of all pins | | | -60 | | | | |
| Σ IIOAH(6) | S40 to S51 | The total of all pins | | | -60 | | | | |
| Low level output current | Peak output current | IOPL(1) | Ports 0,1,3 | At each pins | | | 20 | | |
| | | IOPL(2) | •Ports 70,71,72,73 •Ports 84,85,86,87 | At each pins | | | 15 | | |
| | Total output current | Σ IIOAL(1) | Port 0 | The total of all pins | | | 60 | | |
| | | Σ IIOAL(2) | Ports 1,3,70 | The total of all pins | | | 50 | | |
| Σ IIOAL(3) | •Ports 71,72,73 •Ports 84,85,86,87 | The total of all pins | | | 20 | | | | |
| Maximum power dissipation | Pdmax | QFP100E | Ta=-30 to+70°C | | | | 500 | mW | |
| Operating temperature range | Topr | | | | -30 | | 70 | °C | |
| Storage temperature range | Tstg | | | | -55 | | 125 | | |

2. Recommended Operating Range at Ta=-30°C to +70°C, VSS1=VSS2=0V

| Parameter | Symbol | Pins | Conditions | Ratings | | | unit | |
|--------------------------|--------|------------------------------------------------------|---------------------------------------------------|------------|-----------------|------|----------------|------|
| | | | | VDD[V] | min. | typ. | | max. |
| Operating Supply voltage | VDD(1) | VDD1=VDD2 =VVDD3=VDD4 | 0.98μs ≤ tCYC tCYC ≤ 400μs | | 4.5 | | 6.0 | V |
| Hold voltage | VHD | VDD1=VDD2 | RAMs and the registers hold voltage at HOLD mode. | | 2.0 | | 6.0 | |
| Pull-down Voltage | VP | VP | | 4.5 to 6.0 | -35 | | VDD | |
| Input high voltage | VIH(1) | Port 0 at CMOS output | Output disable | 4.5 to 6.0 | 0.33VDD +1.0 | | VDD | |
| | VIH(2) | Port 0 at N-ch open drain output | Output disable | 4.5 to 6.0 | 0.75VDD | | 13.5 | |
| | VIH(3) | •Port 1 •Ports 72,73 •Port 3 at CMOS output | Output disable | 4.5 to 6.0 | 0.75VDD | | VDD | |
| | VIH(4) | •Port 3 at N-ch open drain output | Output disable Tr. OFF | 4.5 to 6.0 | 0.75VDD | | 13.5 | |
| | VIH(5) | •Port 70 Port input/interrupt •Port 71 •RES | Output disable | 4.5 to 6.0 | 0.75VDD | | VDD | |
| | VIH(6) | Port 70 Watchdog timer | Output disable | 4.5 to 6.0 | 0.9VDD | | VDD | |
| | VIH(7) | •Port 8 •Ports 74,75 | Output disable | 4.5 to 6.0 | 0.75VDD | | VDD | |
| | VIH(8) | S16 to S51 | Output P-channel Tr. OFF | 4.5 to 6.0 | 0.33VDD +1.0 | | VDD | |
| Input low voltage | VIL(1) | Port 0 at CMOS output option | Output disable | 4.5 to 6.0 | VSS | | 0.2VDD | |
| | VIL(2) | Port 0 at N-ch open drain output | Output disable | 4.5 to 6.0 | VSS | | 0.25VDD | |
| | VIL(3) | •Ports 1,3 •Ports 72,73 | Output disable | 4.5 to 6.0 | VSS | | 0.25VDD | |
| | VIL(4) | •Port 70 Port input/interrupt •Port 71 •RES | Output disable | 4.5 to 6.0 | VSS | | 0.25VDD | |
| | VIL(5) | Port 70 Watchdog timer | Output disable | 4.5 to 6.0 | VSS | | 0.8VDD -1.0 | |
| | VIL(6) | •Port 8 •Ports 74,75 | Output disable | 4.5 to 6.0 | VSS | | 0.25VDD | |
| | VIL(7) | S16 to S51 | Output P-channel Tr. OFF | 4.5 to 6.0 | VP | | 0.2VDD | |
| Operation cycle time | tCYC | | | 4.5 to 6.0 | 0.98 | | 400 | μs |

Continue.

| Parameter | Symbol | Pins | Conditions | Ratings | | | unit | |
|-------------------------------------------------|----------|----------|----------------------------------------------------------------|------------|------|--------|------|------|
| | | | | VDD[V] | min. | typ. | | max. |
| Oscillation frequency range (Note 1) | FmCF(1) | CF1, CF2 | •6MHz (ceramic resonator oscillation) •Refer to figure 1 | 4.5 to 6.0 | | 6 | | MHz |
| | FmCF(2) | CF1, CF2 | •3MHz (ceramic resonator oscillation) •Refer to figure 1 | 4.5 to 6.0 | | 3 | | |
| | FmRC | | RC oscillation | 4.5 to 6.0 | 0.3 | 0.8 | 3.0 | |
| | FsXtal | XT1, XT2 | •32.768kHz (crystal oscillation) •Refer to figure 2 | 4.5 to 6.0 | | 32.768 | | kHz |
| Oscillation stabilizing time period (Note 1) | tmsCF(1) | CF1, CF2 | •6MHz (ceramic resonator oscillation) •Refer to figure 3 | 4.5 to 6.0 | | | | ms |
| | tmsCF(2) | CF1, CF2 | •3MHz (ceramic resonator oscillation) •Refer to figure 3 | 4.5 to 6.0 | | | | |
| | tssXtal | XT1, XT2 | •32.768kHz (crystal oscillation) •Refer to figure 3 | 4.5 to 6.0 | | | | s |

(Note 1) The oscillation constant is shown on table 1.

3. Electrical Characteristics at Ta=-30°C to +70°C, VSS1=VSS2=0V

| Parameter | Symbol | Pins | Conditions | Ratings | | | unit | |
|--------------------------|--------|-----------------------------------------------|-----------------------------------------------------------------------------------------------------------|------------|---------|------|------|------|
| | | | | VDD[V] | min. | typ. | | max. |
| Input high current | IIH(1) | Ports 0,3 at open drain output | •Output disable •VIN=13.5V (including off-leakage current of the output Tr.) | 4.5 to 6.0 | | | 5 | μA |
| | IIH(2) | •Ports 1,3 •Port 0 without pull-up MOS Tr. | •Output disable •Pull-up MOS Tr. OFF. •VIN=VDD (including off-leakage current of the output Tr.) | 4.5 to 6.0 | | | 1 | |
| | IIH(3) | •Ports 70,71,72,73 •Port 8 | •Output disable •VIN=VDD (including off-leakage current of the output Tr.) | 4.5 to 6.0 | | | 1 | |
| | IIH(4) | $\overline{\text{RES}}$ | VIN=VDD | 4.5 to 6.0 | | | 1 | |
| | IIH(5) | Ports $\overline{74},75$ | VIN=VDD | 4.5 to 6.0 | | | 1 | |
| | IIH(6) | •S32 to S51 without pull-down resistor | •Output P-channel Tr. OFF. •VIN=VDD | 4.5 to 6.0 | | | 1 | |
| Input low current | IIL(1) | •Ports 1,3 •Port 0 without pull-up MOS Tr. | •Output disable •Pull-up MOS Tr. OFF. •VIN=VSS (including off-leakage current of the output Tr.) | 4.5 to 6.0 | -1 | | | |
| | IIL(2) | •Ports 70,71,72,73 •Port 8 | •Output disable •VIN=VSS (including off-leakage current of the output Tr.) | 4.5 to 6.0 | -1 | | | |
| | IIL(3) | $\overline{\text{RES}}$ | VIN=VSS | 4.5 to 6.0 | -1 | | | |
| | IIL(4) | Ports $\overline{74},75$ | VIN=VSS | 4.5 to 6.0 | -1 | | | |
| Output high voltage | VOH(1) | Ports 0,1,3 of | IOH=-1.0mA | 4.5 to 6.0 | VDD-1 | | | V |
| | VOH(2) | CMOS output | IOH=-0.1mA | 4.5 to 6.0 | VDD-0.5 | | | |
| | VOH(3) | S0/T0 to S15/T15 | IOH=-20mA | 4.5 to 6.0 | VDD-1.8 | | | |
| | VOH(4) | | •IOH=-1.0mA •The current of any unmeasurement pin is not over 1mA. | 4.5 to 6.0 | VDD-1 | | | |
| | VOH(5) | S16 to S51 | IOH=-5mA | 4.5 to 6.0 | VDD-1.8 | | | |
| | VOH(6) | | •IOH=-1.0mA •The current of any unmeasurement pins is not over 1mA. | 4.5 to 6.0 | VDD-1 | | | |
| Output low voltage | VOL(1) | Ports 0,1,3 | IOL=10mA | 4.5 to 6.0 | | | 1.5 | |
| | VOL(2) | | IOL=1.6mA | 4.5 to 6.0 | | | 0.4 | |
| | VOL(3) | Port 70 | IOL=1mA | 4.5 to 6.0 | | | 0.4 | |
| | VOL(4) | •Ports 71,72,73 •Ports 84,85,86,87 | IOL=1.6mA | 4.5 to 6.0 | | | 0.4 | |
| Pull-up MOS Tr. resistor | Rpu | Ports 0,1,3 | VOH=0.9VDD | 4.5 to 6.0 | 15 | 40 | 70 | KΩ |

Continue.

| Parameter | Symbol | Pins | Conditions | Ratings | | | unit | |
|--------------------------------------|----------------------|----------------------------------------------------------------|-----------------------------------------------------------------------------------------------------|------------|------|--------------------|------|------|
| | | | | VDD[V] | min. | typ. | | max. |
| Output off-leakage current | I _{OFF} (1) | •S0/T0 to S6/T6 •S32 to S51 (without pull-down resistor) | •Output P-channel Tr. OFF •V _{OUT} =V _{SS} | 4.5 to 6.0 | -1 | | | μA |
| | I _{OFF} (2) | | •Output P-channel Tr. OFF •V _{OUT} =V _{DD} -40V | 4.5 to 6.0 | -30 | | | |
| Resistance of The low level Hold Tr. | R _{inpd} | S16 to S51 | •Output P-channel Tr. OFF •Using as input ports | 4.5 to 6.0 | | 200 | | KΩ |
| High voltage Pull-down resistor | R _{pd} | •S7/T7 to S15/T15 •S16 to S31 | •Output P-channel Tr. OFF •V _{OUT} =3V •V _p =-30V | 5.0 | 60 | 100 | 200 | |
| VP pull-down resistor | R _{vppd} | V _p | •V _{SS} =GND •V _p =-30V | 5.0 | 60 | 100 | 200 | |
| Hysteresis voltage | V _{HIS} | •Port 1 •Ports 70,71,72,73,75 •RES | Output disable | 4.5 to 6.0 | | 0.1V _{DD} | | V |
| Pin capacitance | CP | All pins | •f=1MHz •V _{IN} =V _{SS} for all unmeasured terminals. •T _a =25°C | 4.5 to 6.0 | | 10 | | pF |

4. Serial Input/Output Characteristics at T_a=-30°C to +70°C, V_{SS1}=V_{SS2}=0V

| Parameter | Symbol | Pins | Conditions | Ratings | | | unit | | | |
|---------------|--------------------------------------------------------------------|------------------------|-----------------------|-------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|------------|------|----------------------|----|------|
| | | | | VDD[V] | min. | typ. | | max. | | |
| Serial clock | Input clock | Cycle | t _{CKCY} (1) | SCK0,SCK1 | Refer to figure 5 | 4.5 to 6.0 | 2 | | | tCYC |
| | | Low Level pulse width | t _{CKL} (1) | | | | 1 | | | |
| | | High Level pulse width | t _{CKH} (1) | | | | 1 | | | |
| | Output clock | Cycle | t _{CKCY} (2) | SCK0,SCK1 | •Use pull-up resistor (1kΩ) in the open drain output. •Refer to figure 5 | 4.5 to 6.0 | 2 | | | |
| | | Low Level pulse width | t _{CKL} (2) | | | | | 1/2t _{CKCY} | | |
| | | High Level pulse width | t _{CKH} (2) | | | | | 1/2t _{CKCY} | | |
| Serial input | Data set-up time | t _{ICK} | •SI0,SI1 •SB0,SB1 | •Data set-up to SCK0,1 •Data hold from SCK0,1 •Refer to figure 5 | 4.5 to 6.0 | 0.1 | | | μs | |
| | Data hold time | t _{ICKI} | | | | 0.1 | | | | |
| Serial output | Output delay time (External clock using for serial transfer clock) | t _{CKO} (1) | •SO0,SO1 •SB0,SB1 | •Use pull-up resistor (1kΩ) in the open drain output. •Data hold from SCK0,1 •Refer to figure 5 | 4.5 to 6.0 | | | 7/12 tCYC +0.2 | | |
| | Output delay time (Internal clock using for serial transfer clock) | t _{CKO} (2) | | | | | | 1/3 tCYC +0.2 | | |

5. Pulse Input Conditions at Ta=-30°C to +70°C, VSS1=VSS2=0V

| Parameter | Symbol | Pins | Conditions | Ratings | | | unit |
|----------------------------|--------------------|------------------------------------------------------------|--------------------------------------------|------------|------|------|------|
| | | | | VDD[V] | min. | typ. | |
| High/low level pulse width | tPIH(1) tPIL(1) | •INT0, INT1 •INT2/T0IN | •Interrupt acceptable •Timer0-countable | 4.5 to 6.0 | 1 | | tCYC |
| | tPIH(2) tPIL(2) | INT3/T0IN (The noise rejection clock selected to 1/1.) | •Interrupt acceptable •Timer0-countable | 4.5 to 6.0 | 2 | | |
| | tPIH(3) tPIL(3) | INT3/T0IN (The noise rejection clock selected to 1/16.) | •Interrupt acceptable •Timer0-countable | 4.5 to 6.0 | 32 | | |
| | tPIH(4) tPIL(4) | INT3/T0IN (The noise rejection clock selected to 1/64.) | •Interrupt acceptable •Timer0-countable | 4.5 to 6.0 | 128 | | |
| | tPIL(5) | RES | Reset acceptable | 4.5 to 6.0 | 200 | | |

6. AD Converter Characteristics at Ta=-30°C to +70°C, VSS1=VSS2=0V

| Parameter | Symbol | Pins | Conditions | Ratings | | | unit | |
|-----------------------------|--------|------------|------------------------------------------------------------|------------|-----------------------------|------|-----------------------------|------|
| | | | | VDD[V] | min. | typ. | | max. |
| Resolution | N | | | 4.5 to 6.0 | | 8 | bit | |
| Absolute precision (Note 2) | ET | | | 4.5 to 6.0 | | | ±1.5 LSB | |
| Conversion time | tCAD | | AD conversion time = 16 × tCYC (ADCR2=0) (Note 3) | 4.5 to 6.0 | 15.68 (tCYC= 0.98μs) | | 65.28 (tCYC= 4.08μs) | μs |
| | | | AD conversion time = 32 × tCYC (ADCR2=1) (Note 3) | | 31.36 (tCYC= 0.98 μs) | | 130.56 (tCYC= 4.08μs) | |
| Analog input voltage range | VAIN | AN0 to AN7 | | 4.5 to 6.0 | VSS | | VDD | V |
| Analog port input current | IAINH | | VAIN=VDD | 4.5 to 6.0 | | | 1 | μA |
| | IAINL | | VAIN=VSS | 4.5 to 6.0 | -1 | | | |

(Note 2) Absolute precision excepts the quantizing error (±1/2 LSB).

(Note 3) The conversion time means the time from executing the AD conversion instruction to setting the complete digital conversion value to the register.

7. Current Dissipation Characteristics at Ta=-30°C to +70°C, VSS1=VSS2=0V

| Parameter | Symbol | Pins | Conditions | Ratings | | | unit | |
|--------------------------------------------------------|----------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|------|------|------|------|
| | | | | VDD[V] | min. | typ. | | max. |
| Current dissipation during basic operation (Note 4) | IDDOP(1) | | <ul style="list-style-type: none"> •FmCF=6MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops •1/1 divided | 4.5 to 6.0 | | 14 | 33 | mA |
| | IDDOP(2) | | <ul style="list-style-type: none"> •FmCF=3MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops •1/2 divided | 4.5 to 6.0 | | 6 | 18 | |
| | IDDOP(3) | | <ul style="list-style-type: none"> •FmCF=0Hz (The oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation •1/2 divided | 4.5 to 6.0 | | 4 | 13 | |
| | IDDOP(4) | | <ul style="list-style-type: none"> •FmCF=0Hz (The oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : 32.768kHz •Internal RC oscillation stops •1/2 divided | 4.5 to 6.0 | | 3 | 10 | |

Continue.

| Parameter | Symbol | Pins | Conditions | Ratings | | | unit | |
|-------------------------------------------------|------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|------|------|------|------|
| | | | | VDD[V] | min. | typ. | | max. |
| Current dissipation in HALT mode (Note 4) | IDDHALT(1) | | <ul style="list-style-type: none"> •HALT mode •FmCF=6MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops •1/1 divided | 4.5 to 6.0 | | 5 | 14 | mA |
| | IDDHALT(2) | | <ul style="list-style-type: none"> •HALT mode •FmCF=3MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops •1/2 divided | 4.5 to 6.0 | | 2.2 | 7 | |
| | IDDHALT(3) | | <ul style="list-style-type: none"> •HALT mode FmCF=0Hz (The oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation •1/2 divided | 4.5 to 6.0 | | 400 | 1600 | μA |
| | IDDHALT(4) | | <ul style="list-style-type: none"> •HALT mode FmCF=0Hz (The oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : crystal oscillation •Internal RC oscillation stops •1/2 divided | 4.5 to 6.0 | | 25 | 100 | |
| Current dissipation in HOLD mode (Note 4) | IDDHOLD(1) | | HOLD mode | 4.5 to 6.0 | | 0.05 | 30 | |

(Note 4) The currents of the output transistors and the pull-up MOS transistors are ignored.

Table 1. Ceramic resonator oscillation recommended constant (main-clock)

| Oscillation type | Maker | Oscillator | C1 | C2 |
|------------------------------------|---------|------------|----|----|
| 6MHz ceramic resonator oscillation | Murata | | | |
| | Kyocera | | | |
| 3MHz ceramic resonator oscillation | Murata | | | |
| | Kyocera | | | |

* Both C1 and C2 must be use K rank ($\pm 10\%$) and SL characteristics.

Table 2. Crystal oscillation guaranteed constant (sub-clock)

| Oscillation type | Maker | Oscillator | C3 | C4 | Rd | Rf |
|-------------------------------|-------|------------|----|----|----|----|
| 32.768kHz crystal oscillation | | | | | | |
| | | | | | | |

* Both C3 and C4 must be use J rank ($\pm 5\%$) and CH characteristics.

(Not in need of high precision, use K rank ($\pm 10\%$) and SL characteristics.)

- (Notes)
- Please place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length since the circuit pattern affects the oscillation frequency.
 - If you use other oscillators herein, we provide no guarantee for the characteristics.

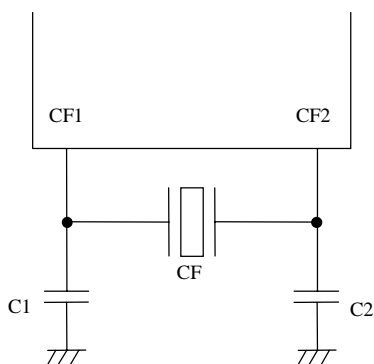


Figure 1 Main-clock circuit
Ceramic resonator oscillation

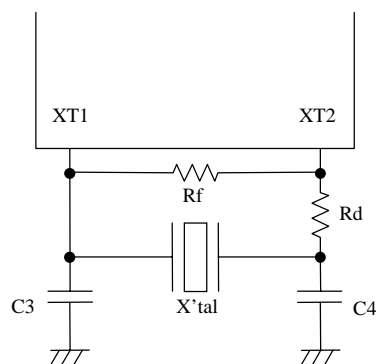


Figure 2 Sub-clock circuit
Crystal oscillation

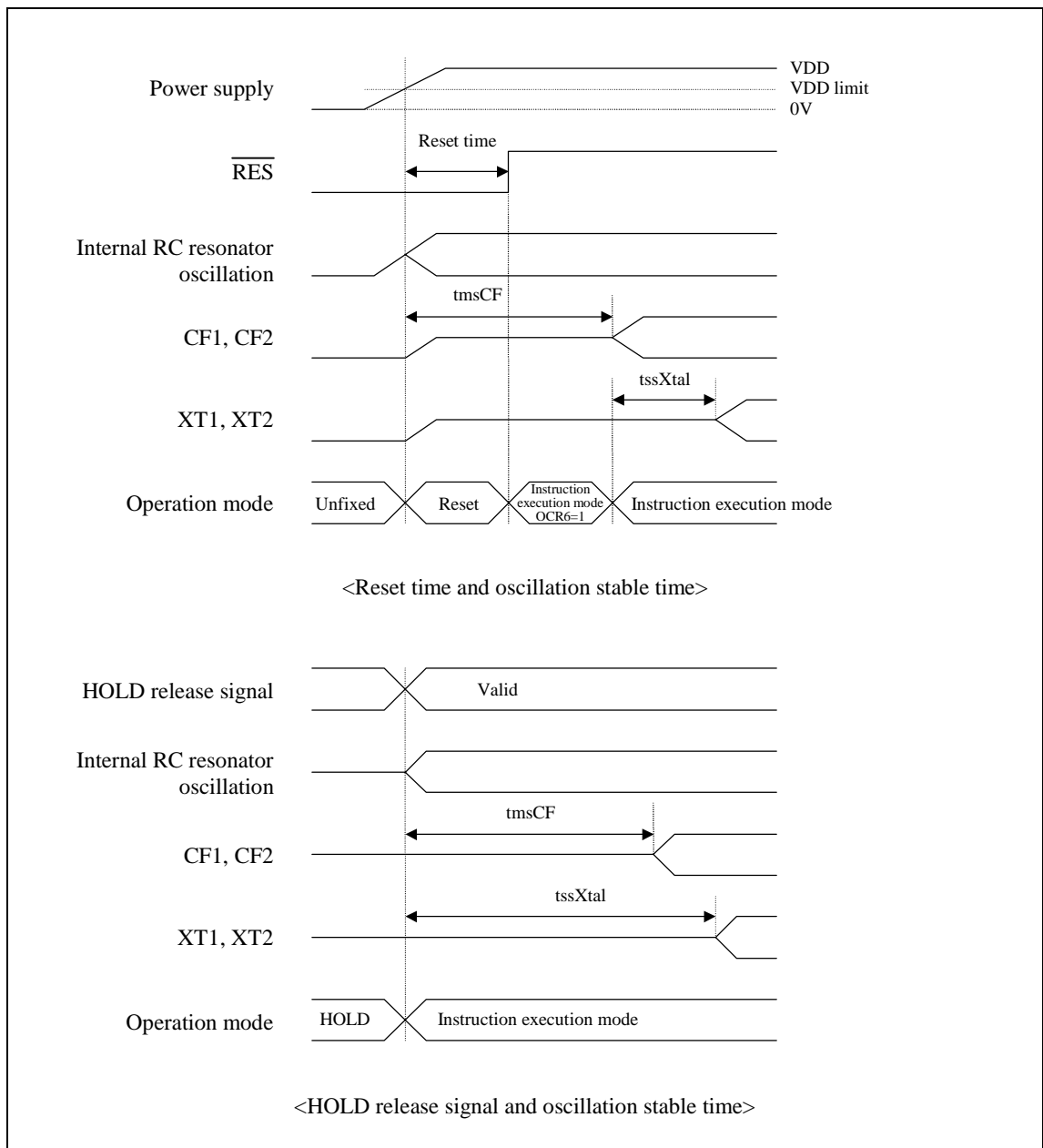
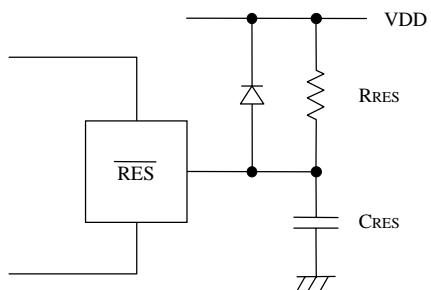


Figure 3 Oscillation stable time



(Note) Fix the value of CRES, RRES that is sure to reset until 200 μ s, after Power supply has been over inferior limit of supply voltage.

Figure 4 Reset circuit

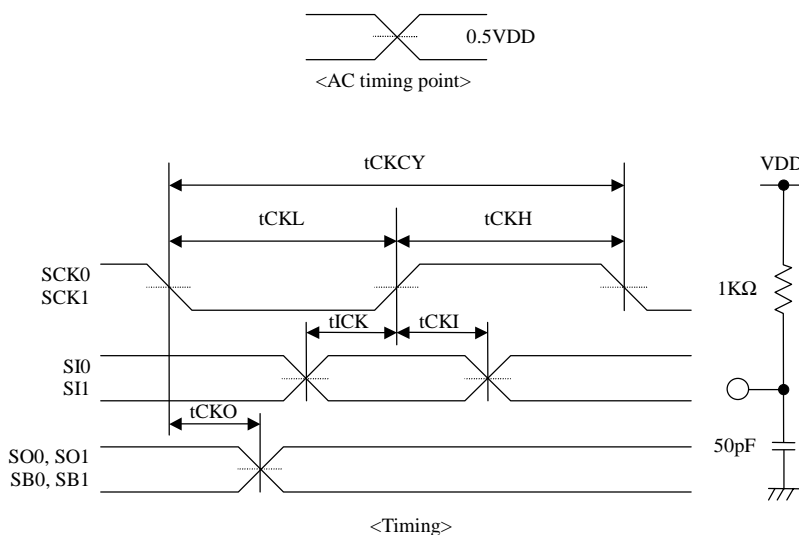


Figure 5 Serial input / output test condition

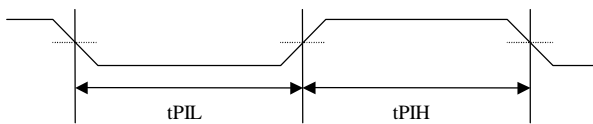
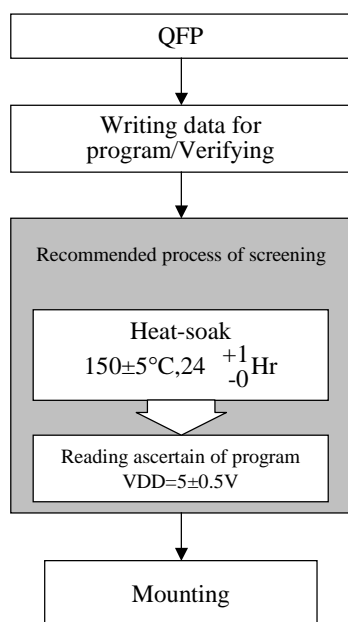


Figure 6 Pulse input timing condition

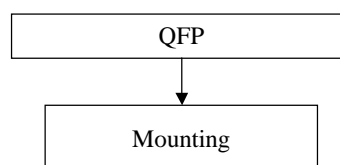
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- It is not possible to perform a writing test on the blank PROM. 100% yield, therefore, cannot be guaranteed.
- Keeping the dry packing
The environment must be held at a temperature of 30°C or less and a humidity level of 70% or less.
- After opening the packing
The preparation procedures shown in the following figure should always be followed prior to mounting the packages on the substrate. After opening the packing, a controlled environment must be maintained until soldering. The environment must be held at a temperature of 30°C or less and a humidity level of 70% or less. Please solder within 96 hours.
Unused devices should be kept in the dry atmosphere such as inside of desiccator or dry these up before assembling on the board.

a. Shipping with a blank PROM
(Programming the data by yourself)



b. Shipping with a programmed PROM
(Programming the data by Sanyo)



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