Features...

- High-performance CMOS EEPROM-based programmable logic devices (PLDs) built on third-generation Multiple Array MatriX (MAX) architecture
- 5.0-V in-system programmability (ISP) through built-in JTAG interface
- High-density EPLD family ranging from 6,000 to 12,000 usable gates (see Table 1)
- 12-ns pin-to-pin logic delays with counter frequencies up to 125 MHz
- PCI-compliant -12 speed grade
- Built-in JTAG boundary-scan test (BST) circuitry as compliant with IEEE Std 1149.1-1990
- Dual-output macrocell for independent use of combinatorial and registered logic
- FastTrack Interconnect continuous routing structure for fast, predictable interconnect delays
- Input/output registers with clear and clock enable on all I/O pins
- Programmable output slew-rate control to reduce switching noise
- 3.3-V or 5.0-V I/O operation on all devices
- Configurable expander product-term distribution allowing up to 32 product terms per macrocell
- Programmable power-saving mode for more than 50% power reduction in each macrocell
- Programmable macrocell flipflops with individual clear, preset, clock, and clock enable controls

Table 1. MAX 9000 Device Features

Feature	EPM9320	EPM9400	EPM9480	EPM9560
Usable gates	6,000	8,000	10,000	12,000
Flipflops	484	580	676	772
Macrocells	320	400	480	560
Logic array blocks (LABs)	20	25	30	35
Maximum user I/O pins	168	159	175	216
t_{PD1} (ns)	12	12	12	12
t_{FSU} (ns)	4	4	4	4
t_{FCO} (ns)	5.5	5.5	5.5	5.5
f_{CNT} (MHz)	125	125	118	118

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MAX 9000

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... and More Features

- Programmable security bit for protection of proprietary designs
- Software design support and automatic place-and-route provided by Altera's MAX+PLUS II development system on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF, Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Data I/O, Exemplar, Mentor Graphics, MINC, OrCAD, Synopsys, VeriBest, and Viewlogic
- Programming support with Altera's Master Programming Unit (MPU) and BitBlaster serial download cable, as well as programming hardware from other manufacturers
- Offered in a variety of package options with 84 to 356 pins (see Table 2)

Table 2. MAX 9000 Package Options & I/O Count   Note (1)

Device	84-Pin PLCC	208-Pin RQFP	240-Pin RQFP	280-Pin PGA	304-Pin RQFP	356-Pin BGA
EPM9320	60 (2)	132	–	168	–	168
EPM9400	59 (2)	139	159	–	–	–
EPM9480	–	146	175	–	–	–
EPM9560	–	153	191	216	216	216

Notes:
(1) Contact Altera Customer Marketing at (408) 894-7104 for up-to-date information on package availability.
(2) Perform a complete thermal analysis before committing a design to this device package. See *Application Note 74 (Evaluating Power for Altera Devices)* in this data book for more information.

General Description

The MAX 9000 family of in-system-programmable, high-density, high-performance EPLDs is based on Altera's third-generation MAX architecture. Fabricated on an advanced CMOS technology, the EEPROM-based MAX 9000 family provides 6,000 to 12,000 usable gates, pin-to-pin delays as fast as 12 ns, and counter speeds of up to 125 MHz. The -12 speed grade of the MAX 9000 family is compliant with the *PCI Local Bus Specification*, version 2. Table 3 shows the speed grades available for MAX 9000 devices.

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Table 3. MAX 9000 Speed Grade Availability

Device	Speed Grade		
	-12	-15	-20
EPM9320	✓ (1)	✓	✓
EPM9400	✓ (1)	✓	✓
EPM9480	✓ (1)	✓	✓
EPM9560	✓ (1)	✓	✓

Note:
(1) This information is preliminary. Contact Altera for up-to-date information on package availability.

Table 4 shows the performance of MAX 9000 devices for typical functions.

Table 4. MAX 9000 Performance   *Note (1)*

Application	Macrocells Used	Speed Grade			Unit
		-12 *(2)*	**-15**	**-20**	
16-bit loadable counter	16	125	118	100	MHz
16-bit up/down counter	16	125	118	100	MHz
16-bit prescaled counter	16	125	118	100	MHz
16-bit address decode	1	6.5 (12)	7.9 (15)	10 (20)	ns
16-to-1 multiplexer	1	8.9 (14.4)	10.9 (18)	16 (26)	ns

Notes:
(1) Internal logic array block (LAB) performance is shown. Numbers in parentheses show external delays from row input to row I/O.
(2) This information is preliminary.

The MAX 9000 architecture supports high-density integration of system-level logic functions. It easily integrates multiple programmable logic devices ranging from PALs, GALs, and 22V10s to field-programmable gate array (FPGA) devices and erasable programmable logic devices (EPLDs). With speed, density, and I/O resources comparable to commonly used masked gate arrays, MAX 9000 EPLDs are also ideal for gate-array prototyping.

All MAX 9000 device packages provide four dedicated inputs for global control signals with large fan-outs. Each I/O pin has an associated I/O cell register with a clock enable control on the periphery of the device. As outputs, these registers provide fast clock-to-output times; as inputs, they offer quick setup times.

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MAX 9000 EPLDs provide 5.0-V in-system programmability (ISP). This feature allows the devices to be programmed and reprogrammed on the printed circuit board (PCB) for quick and efficient iterations during design development and debug cycles. MAX 9000 devices are guaranteed for 100 program and erase cycles.

MAX 9000 EPLDs contain from 320 to 560 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. For increased flexibility, each macrocell offers a dual-output structure that allows the register and the product terms to be used independently. This feature allows register-rich and combinatorial-intensive designs to be implemented efficiently. The dual-output structure of the MAX 9000 macrocell also improves logic utilization, thus increasing the effective capacity of the devices. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 9000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the user to configure one or more macrocells to operate at 50% or less power while adding only a nominal timing delay. MAX 9000 devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. MAX 9000 output drivers can be set for either 3.3-V or 5.0-V operation, allowing MAX 9000 devices to be used in mixed-voltage systems.

The MAX 9000 family is supported by Altera's MAX+PLUS II development system, a single, integrated software package that offers schematic, text—including the Altera Hardware Description Language (AHDL)—and waveform design entry; compilation and logic synthesis; simulation and timing analysis; and device programming. MAX+PLUS II provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and workstation-based EDA tools. MAX+PLUS II runs on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations.

For more information on development tools, go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book.

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Functional Description

MAX 9000 devices use third-generation MAX architecture that yields both high performance and a high degree of utilization for most applications. The MAX 9000 architecture includes the following elements:

- Logic array blocks
- Macrocells
- Expander product terms (shareable and parallel)
- FastTrack Interconnect
- Dedicated inputs
- I/O cells

Figure 1 shows a block diagram of the MAX 9000 architecture.

Figure 1. MAX 9000 Device Block Diagram


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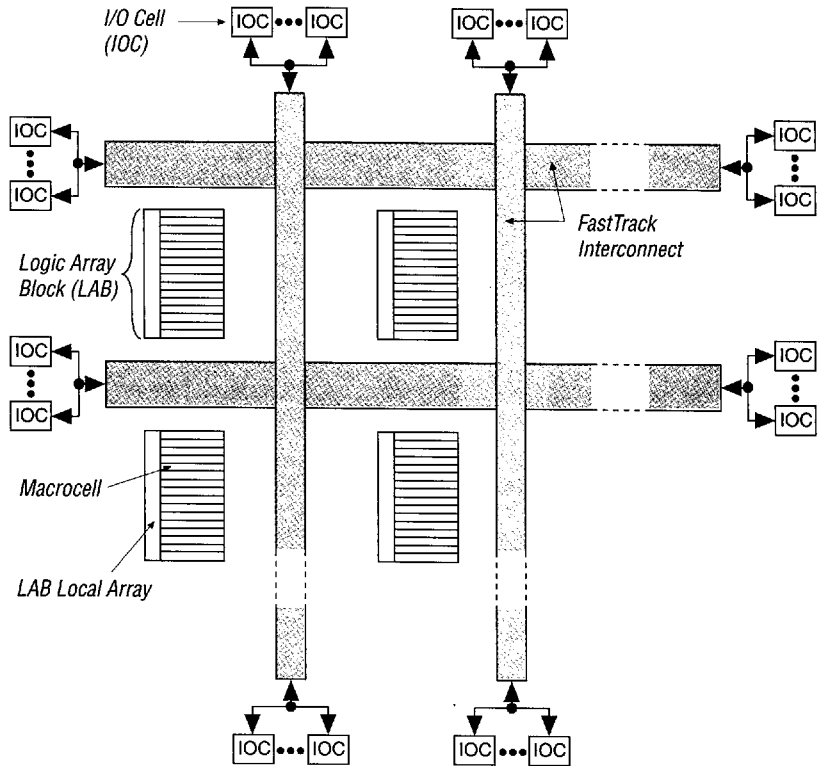
Logic Array Blocks

The MAX 9000 architecture is based on linking of high-performance, flexible logic array modules called logic array blocks (LABs). LABs consist of 16-macrocell arrays that are fed by the LAB local array, as shown in Figure 2. Multiple LABs are linked together via the FastTrack Interconnect, a series of fast, continuous channels that run the entire length and width of the device. The I/O pins are supported by I/O cells (IOCs) located at the end of each row (horizontal) and column (vertical) path of the FastTrack Interconnect.

Each LAB is fed by 33 inputs from the row interconnect and 16 feedback signals from the macrocells within the LAB. All of these signals are available within the LAB in their true and inverted form. In addition, 16 shared expander product terms ("expanders") are available in their inverted form, for a total of 114 signals that feed each product term in the LAB. Each LAB is also fed by two low-skew global clocks and one global clear that can be used for register control signals in all 16 macrocells.

The LAB drives the row and column interconnect directly. Each macrocell can drive out of the LAB onto one or both of these routing resources. Once signals are on the row or column interconnect, they can quickly traverse to other LABs or to the IOCs.

Figure 2. MAX 9000 Logic Array Block

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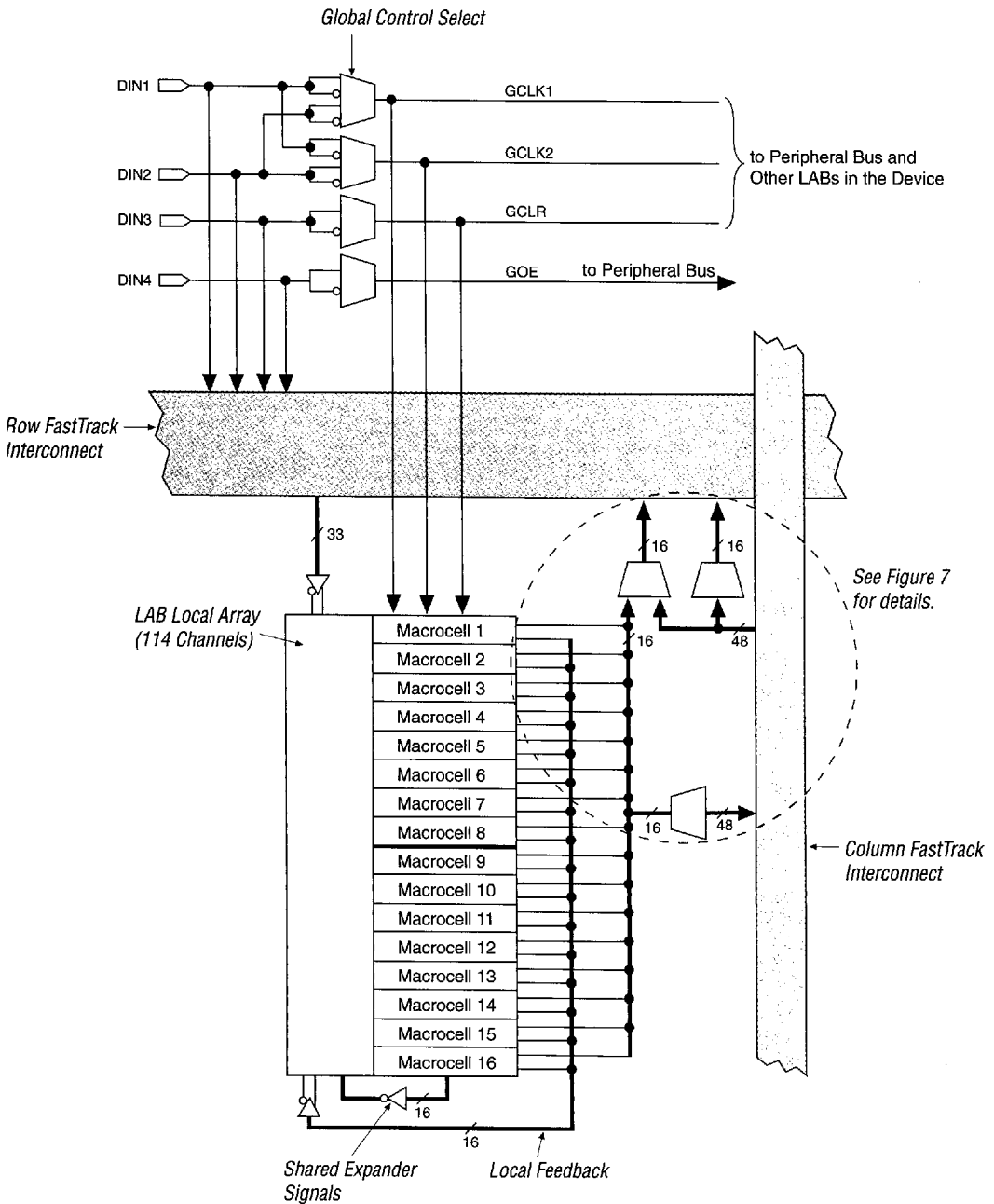
Macrocells

The MAX 9000 macrocell consists of three functional blocks: the product terms, the product-term select matrix, and the programmable register. The macrocell can be individually configured for both sequential and combinatorial logic operation. See Figure 3.

Figure 3. MAX 9000 Macrocell & Local Array
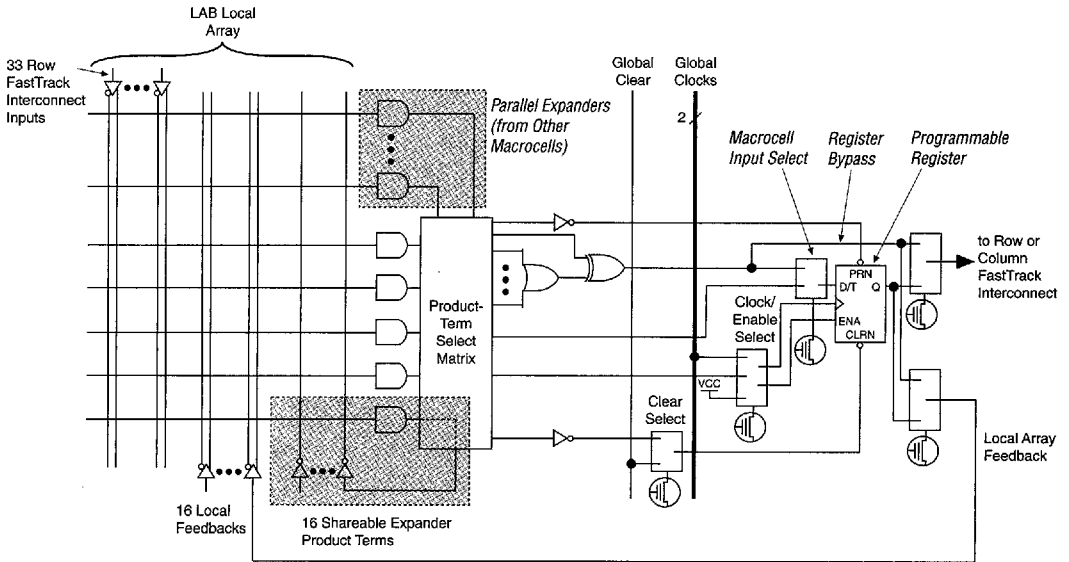
Combinatorial logic is implemented in the local array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register clear, preset, clock, and clock enable control functions. Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

MAX+PLUS II automatically optimizes product-term allocation according to the logic requirements of the design.

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For registered functions, each macrocell register can be individually programmed for D, T, JK, or SR operation with programmable clock control. The flipflop can also be bypassed for combinatorial operation. During design entry, the user specifies the desired register type; MAX+PLUS II then selects the most efficient register operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

■ By either global clock signal. This mode achieves the fastest clock-to-output performance.

■ By a global clock signal and enabled by an active-high clock enable. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.

■ By an array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available. As shown in Figure 2, these global clock signals can be the true or the complement of either of the global clock pins, DIN1 and DIN2.

Each register also supports asynchronous preset and clear functions. As shown in Figure 3, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear inputs to registers are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the dedicated global clear pin (DIN3). The global clear can be programmed for active-high or active-low operation.

All MAX 9000 macrocells offer a dual-output structure that provides independent register and combinatorial logic output within the same macrocell. This function is implemented by a process called register packing. When register packing is used, the product-term select matrix allocates one product term to the D input of the register, while the remaining product terms can be used to implement unrelated combinatorial logic. Both the registered and the combinatorial output of the macrocell can feed either the FastTrack Interconnect or the LAB local array.
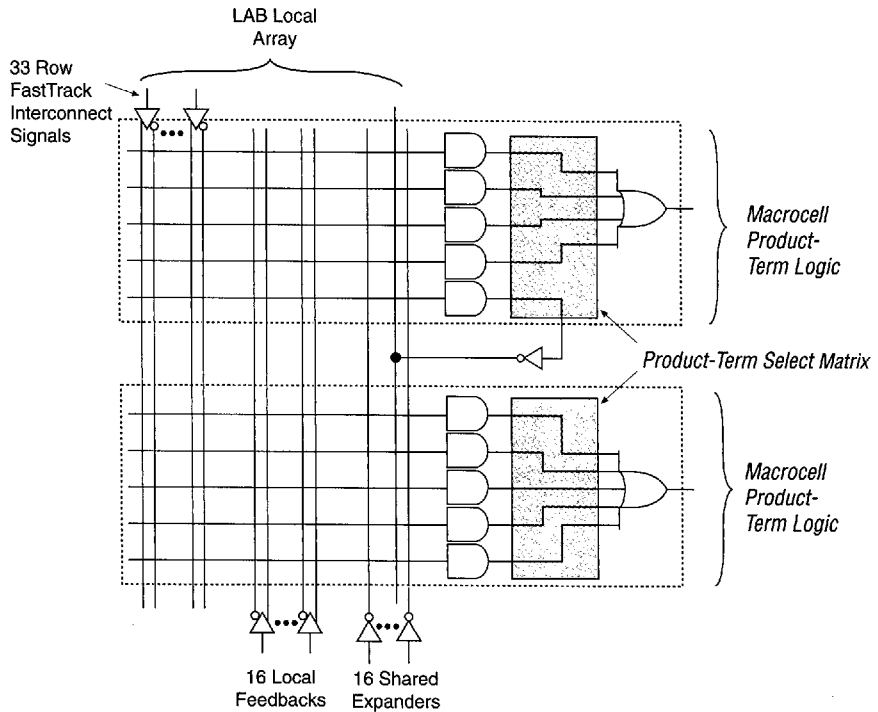
Expander Product Terms

Although most logic functions can be implemented with the five product terms available in each macrocell, some logic functions are more complex and require additional product terms. Although another macrocell can supply the required logic resources, the MAX 9000 architecture also offers both shareable and parallel expander product terms that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the LAB local array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay ($t_{LOCAL} + t_{SEXP}$) is incurred when shareable expanders are used. Figure 4 shows how shareable expanders can feed multiple macrocells.

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Figure 4. Shareable Expanders

Shareable expanders can be shared by any or all macrocells in the LAB.

Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with 5 product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB. Figure 5 shows how parallel expanders can feed the neighboring macrocell.

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Figure 5. Parallel Expanders

Unused product terms in a macrocell can be allocated to a neighboring macrocell.
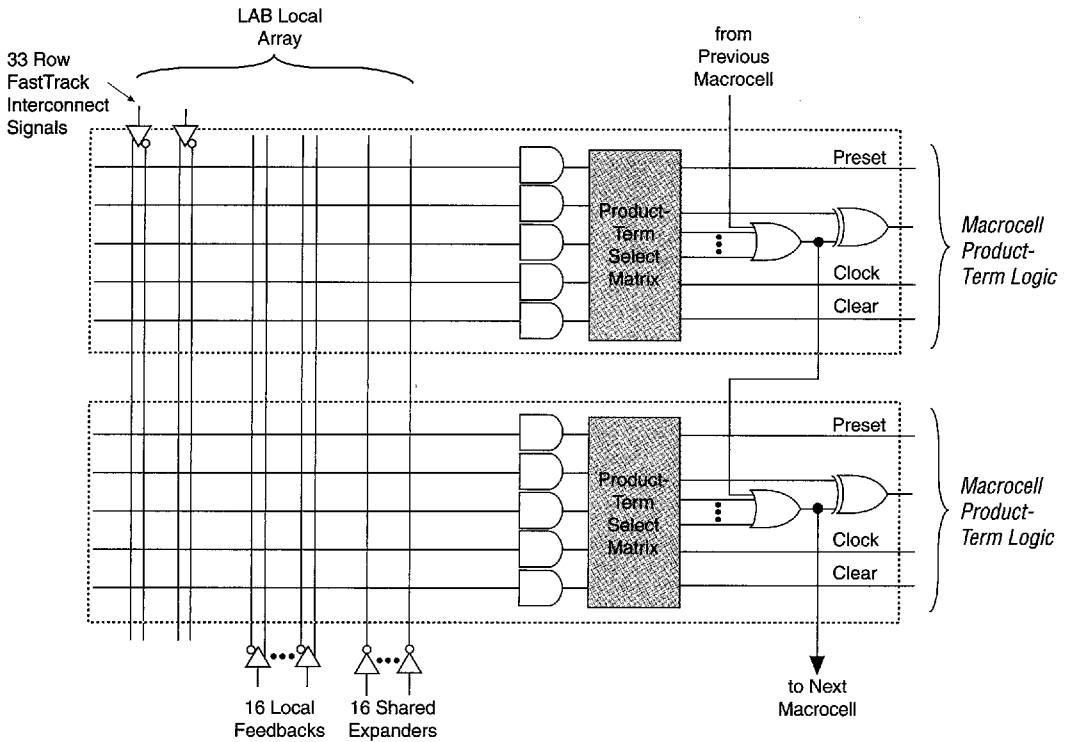
The MAX+PLUS II Compiler can automatically allocate as many as 3 sets of up to 5 parallel expanders to the macrocells that require additional product terms. Each set of expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the 5 dedicated product terms within the macrocell and allocates 2 sets of parallel expanders; the first set includes 5 product terms and the second set includes 4 product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of 8 macrocells within each LAB (e.g., macrocells 1 to 8 and 9 to 16) form 2 chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them.

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FastTrack Interconnect

In the MAX 9000 architecture, connections between macrocells and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal and vertical routing channels that traverse the entire device. This device-wide routing structure provides predictable performance even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance. Figure 6 shows the interconnection of four adjacent LABs with row and column interconnects.

Figure 6. MAX 9000 Device Interconnect Resources

Each LAB is named on the basis of its physical row (A, B, C, etc.) and column (1, 2, 3, etc.) position within the device.
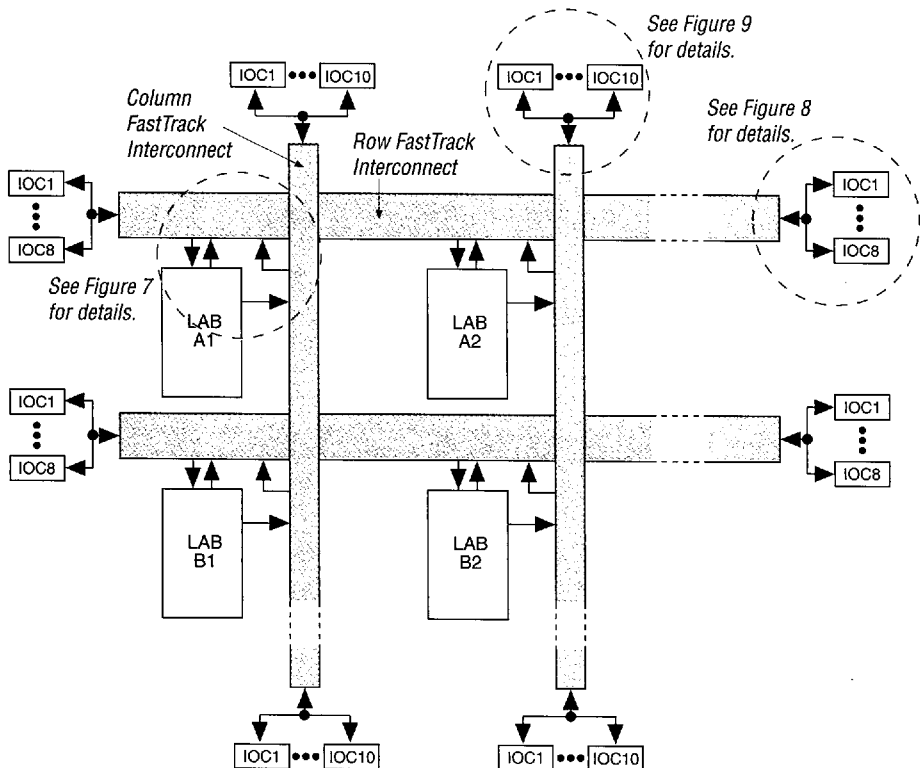

The LABs within MAX 9000 devices are arranged into a matrix of columns and rows. Table 5 shows the number of columns and rows in each MAX 9000 device.

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Table 5. MAX 9000 Rows & Columns		
Device	**Rows**	**Columns**
EPM9320	4	5
EPM9400	5	5
EPM9480	6	5
EPM9560	7	5

Each row of LABs has a dedicated row interconnect that routes signals both into and out of the LABs in the row. The row interconnect can then drive I/O pins or feed other LABs in the device. Each row interconnect has a total of 96 channels. Figure 7 shows how a macrocell drives the row and column interconnect.

Figure 7. LAB Connections to Row & Column Interconnect


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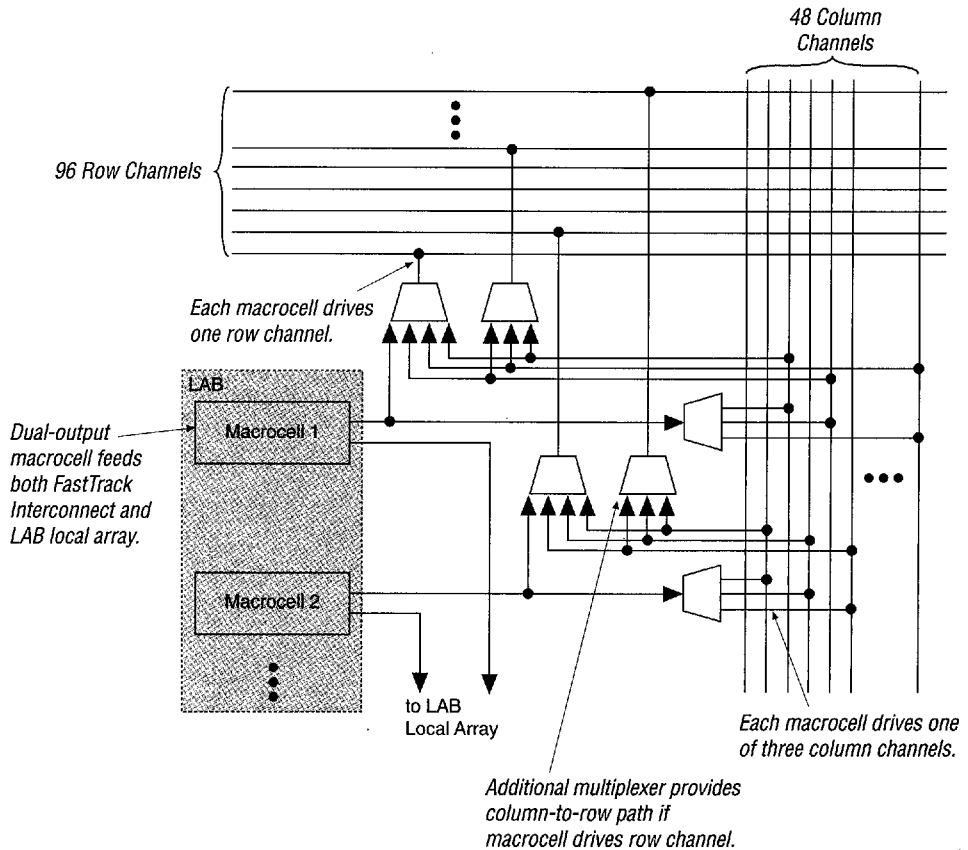
Each macrocell in the LAB can drive one of three separate column interconnect channels. The column channels run vertically across the entire device, and are shared by the macrocells in the same column. The MAX+PLUS II Compiler automatically optimizes connections to a column channel.

A row interconnect channel can be fed by the output of the macrocell through a 4-to-1 multiplexer that the macrocell shares with three column channels. If the multiplexer is used for a macrocell-to-row connection, the three column signals can access another row channel via an additional 3-to-1 multiplexer. Within any LAB, the multiplexers provide all 48 column channels with access to 32 row channels.

Row-to-I/O Cell Connections

Figure 8 illustrates the connections between row interconnect channels and I/O cells (IOCs). An input signal from an IOC can drive two separate row channels. When an IOC is used as an output, the signal is driven by a 10-to-1 multiplexer that selects the row channels. Each end of the row channel feeds up to eight IOCs on the periphery of the device.

Figure 8. MAX 9000 Row-to-IOC Connections

Each IOC is driven by a 10-to-1 multiplexer.

Each IOC can drive up to two row channels.
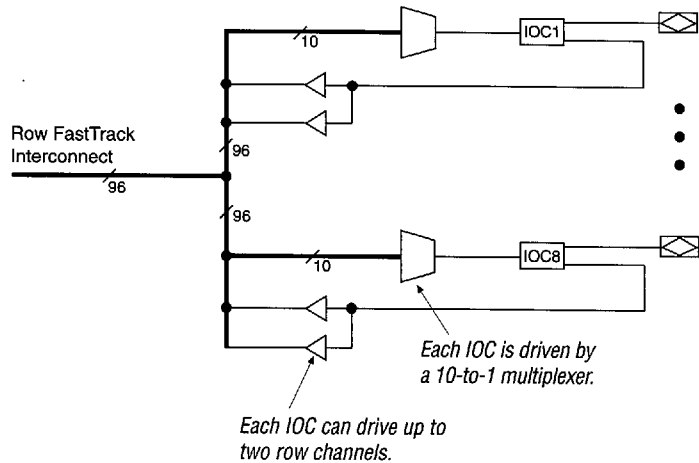
Column-to-I/O Cell Connections

Each end of a column channel has up to 10 IOCs (see Figure 9). An input signal from an IOC can drive two separate column channels. When an IOC is used as an output, the signal is driven by a 17-to-1 multiplexer that selects the column channels.

Figure 9. MAX 9000 Column-to-IOC Connections

Each IOC is driven by a 17-to-1 multiplexer.

Each IOC can drive up to two column channels.

Column FastTrack Interconnect
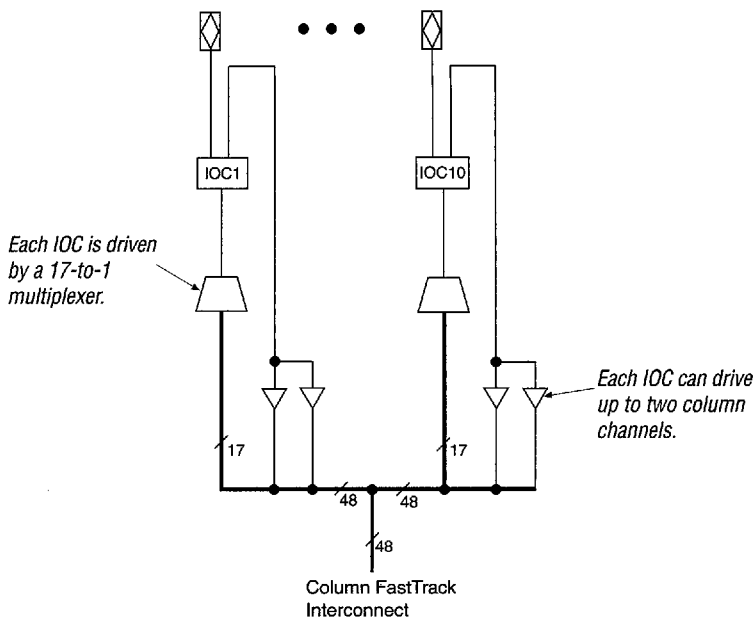
Dedicated Inputs

In addition to the general-purpose I/O pins, MAX 9000 devices have four dedicated input pins. These dedicated inputs provide low-skew, device-wide signal distribution to the LABs and IOCs in the device, and are typically used for global clock, clear, and output enable control signals. The global control signals can feed the macrocell or IOC clock and clear inputs, as well as the IOC output enable. The dedicated inputs can also be used as general-purpose data inputs because they can feed the row FastTrack Interconnect.

I/O Cells

Figure 10 shows the I/O cell (IOC) block diagram. Signals enter the MAX 9000 device from either the I/O pins that provide general-purpose input capability or from the four dedicated inputs. The IOCs are located at the ends of the row and column interconnect channels.

I/O pins can be used as input, output, or bidirectional pins. Each IOC has an IOC register with a clock enable input. This register can be used either as an input register for external data that requires fast setup times, or as an output register for data that requires fast clock-to-output performance. The IOC register clock enable allows the global clock to be used for fast clock-to-output performance, while maintaining the flexibility required for selective clocking.

Figure 10. I/O Cell (IOC)
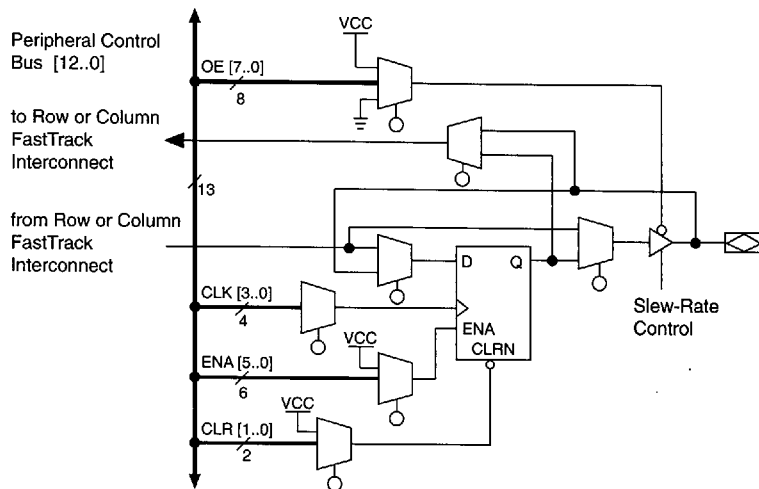
The clock, clock enable, clear, and output enable controls for the IOCs are provided by a network of I/O control signals. These signals can be supplied by either the dedicated input pins or internal logic. The IOC control-signal paths are designed to minimize the skew across the device. All control-signal sources are buffered onto high-speed drivers that drive the signals around the periphery of the device. This "peripheral bus" can be configured to provide up to eight output enable signals, up to four clock signals, up to six clock enable signals, and up to two clear signals. Table 6 shows the sources that drive the peripheral bus and how the IOC control signals share the peripheral bus.

The output buffer in each IOC has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces board-level noise and adds a nominal timing delay to the output buffer delay (t_{OD}) parameter. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a global basis.

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Table 6. Peripheral Bus Sources

Peripheral Control Signal	Source			
	EPM9320	EPM9400	EPM9480	EPM9560
OE0/ENA0	Row C	Row E	Row F	Row G
OE1/ENA1	Row B	Row E	Row F	Row F
OE2/ENA2	Row A	Row E	Row E	Row E
OE3/ENA3	Row B	Row B	Row B	Row B
OE4/ENA4	Row A	Row A	Row A	Row A
OE5	Row D	Row D	Row D	Row D
OE6	Row C	Row C	Row C	Row C
OE7/CLR1	Row B/GOE	Row B/GOE	Row B/GOE	Row B/GOE
CLR0/ENA5	Row A/GCLR	Row A/GCLR	Row A/GCLR	Row A/GCLR
CLK0	GCLK1	GCLK1	GCLK1	GCLK1
CLK1	GCLK2	GCLK2	GCLK2	GCLK2
CLK2	Row D	Row D	Row D	Row D
CLK3	Row C	Row C	Row C	Row C

3.3-V or 5.0-V I/O Operation

All MAX 9000 devices can be set to interface at 3.3 V or 5.0 V. These devices have one set of V_{CC} pins for internal operation and input buffers (V_{CCINT}), and another set for I/O output drivers (V_{CCIO}).

The V_{CCINT} pins must always be connected to a 5.0-V supply. With a 5.0-V V_{CCINT} level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs. The V_{CCIO} pins can be connected to either a 3.3-V or 5.0-V supply, depending on the output requirements. When the V_{CCIO} pins are connected to a 5.0-V supply, the output levels are compatible with 5.0-V systems. When the V_{CCIO} pins are connected to a 3.3-V supply, the output high is at 3.3 V and is therefore compatible with 3.3-V systems. Devices operating with a V_{CCIO} level below 4.75 V incur a nominal timing delay adder for the output buffer delay (t_{OD}).

In-System Programmability (ISP)

MAX 9000 devices can be programmed in-system through a 4-pin JTAG BST interface. In-system programmability (ISP) offers quick and efficient iterations during design development and debug cycles. The MAX 9000 architecture internally generates the 12.0-V programming voltage required to program EEPROM cells, eliminating the need for an external 12.0-V power supply to program the devices on the board. During ISP, the I/O pins are tri-stated to eliminate board conflicts.

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ISP simplifies the manufacturing flow by allowing the devices to be mounted on a printed circuit board with standard pick-and-place equipment before they are programmed. MAX 9000 devices can be programmed by downloading the information via automatic test equipment, embedded processors, or the Altera BitBlaster serial download cable. Programming the devices after they are placed on the board eliminates lead damage on high pin-count packages (e.g., QFP packages) due to device handling. MAX 9000 devices can be reprogrammed in the field. For example, product upgrades can be performed in the field via software or modem.

Go to *Application Brief 141 (In-System Programmability in MAX 9000 Devices)* for more information.

Programming with External Hardware

MAX 9000 devices can be programmed on 486- and Pentium-based PCs with an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device. For more information, see *Altera's Programming Hardware Data Sheet* in this data book.

The MAX+PLUS II software can use text- or waveform-format test vectors created with the MAX+PLUS II Text or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 9000 device with the results of simulation.

Data I/O and other programming hardware manufacturers also provide programming support for Altera devices. See *Programming Hardware Manufacturers* in this data book for more information.

JTAG Operation

All MAX 9000 devices provide JTAG BST circuitry as specified by IEEE Std 1149.1-1990. The supported features are SAMPLE/PRELOAD, EXTEST, and BYPASS. MAX 9000 devices have four dedicated JTAG pins that are used for JTAG BST and in-system programming.

For detailed information on JTAG operation in MAX 9000 devices, refer to *Application Note 39 (JTAG Boundary-Scan Testing in Altera Devices)*.

Programmable Speed/Power Control

MAX 9000 devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, since most logic applications require only a small fraction of all gates to operate at maximum frequency.

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The designer can program each individual macrocell in a MAX 9000 device for either high-speed (Turbo Bit on) or low-power (Turbo Bit off) operation. As a result, speed-critical paths in the design can run at high speed, while remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the LAB local array delay (t_{LOCAL}).

Design Security

All MAX 9000 EPLDs contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is erased.

Generic Testing

MAX 9000 EPLDs are fully functionally tested. Complete testing of each programmable EEPROM bit and all logic functionality ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 11. Test patterns can be used and then erased during the early stages of the production flow.

Figure 11. MAX 9000 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold test must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.
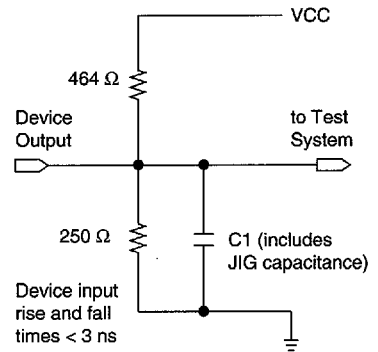
QFP Carrier & Development Socket

MAX 9000 devices in QFP packages with 100 or more pins can be shipped in plastic carriers to protect the fragile QFP leads. The carrier is used with a prototype development socket and special programming hardware available from Altera. This carrier makes it possible to program, test, erase, and reprogram a device without exposing the leads to mechanical stress. When programming in-system, devices in QFP packages generally do not require a carrier and a prototype development socket.

For detailed information, go to the *QFP Carrier & Development Socket Data Sheet* in this data book.

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MAX 9000 Device Absolute Maximum Ratings   *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (2)*	–2.0	7.0	V
V_{CCISP}	Supply voltage during in-system programming		–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	°C
T_{AMB}	Ambient temperature	Under bias	–65	135	°C
T_J	Junction temperature	Ceramic packages, under bias		150	°C
		Plastic and power quad flat pack packages, under bias		135	°C

MAX 9000 Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*Notes (3), (4)*	4.75 (4.50)	5.25 (5.50)	V
V_{CCIO}	Supply voltage for output drivers, 5.0-V operation	*Notes (3), (4)*	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output drivers, 3.3-V operation	*Note (3)*	3.00	3.60	V
V_{CCISP}	Supply voltage during in-system programming		4.75	5.25	V
V_I	Input voltage		0	V_{CCINT}	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Operating temperature	For commercial use	0	70	°C
T_A	Operating temperature	For industrial use	–40	85	°C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

MAX 9000 Device DC Operating Conditions   *Notes (5), (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CCINT} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	5.0-V high level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 4.75 V, *Note (7)*	2.4		V
	3.3-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 3.0 V, *Note (7)*	2.4		V
V_{OL}	5.0-V high level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 4.75 V, *Note (7)*		0.45	V
	3.3-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.0 V, *Note (7)*		0.45	
I_I	Input leakage current	V_I = V_{CC} or GND, *Note (8)*	–10	10	μA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–40	40	μA

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MAX 9000 Device Capacitance   Note (9)

Symbol	Parameter	Conditions	Min	Max	Unit
C_{DIN1}	Dedicated input capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		18	pF
C_{DIN2}	Dedicated input capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		18	pF
C_{DIN3}	Dedicated input capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		17	pF
C_{DIN4}	Dedicated input capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		20	pF
$C_{I/O}$	I/O pin capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		12	pF

MAX 9000 Device Typical I_{CC} Supply Current Values

Symbol	Parameter	Conditions	EPM9320	EPM9400	EPM9480	EPM9560	Unit
I_{CC1}	I_{CC} supply current (low-power mode, standby, typical)	$V_I = $ GND, No load, Note (10)	100	110	140	150	mA

Notes to tables:
(1) See *Operating Requirements for Altera Devices* in this data book.
(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(3) V_{CC} must rise monotonically.
(4) Numbers in parentheses are for industrial-temperature-range versions.
(5) Typical values are for $T_A = 25°$ C and $V_{CC} = 5.0$ V.
(6) Operating conditions: $V_{CCINT} = 5.0$ V $\pm 5\%$, $T_A = 0°$ C to 70° C for commercial use.
        $V_{CCINT} = 5.0$ V $\pm 10\%$, $T_A = -40°$ C to 85° C for industrial use.
        $V_{CCIO} = 5.0$ V $\pm 5\%$ for 5.0-V operation.
        $V_{CCIO} = 3.3$ V $\pm 10\%$ for 3.3-V operation.
(7) This parameter is measured with 50% of the outputs each sinking 12 mA. The I_{OH} parameter refers to high-level TTL output current; the I_{OL} parameter refers to the low-level TTL output current.
(8) JTAG input leakage is typically –60 µA.
(9) Capacitance sample-tested only and measured at 25° C.
(10) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. I_{CC} is measured at 0° C.

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Figure 12 shows typical output drive characteristics for MAX 9000 devices with 5.0-V and 3.3-V V_{CCIO}.

Figure 12. Output Drive Characteristics of MAX 9000 Devices Note (1)
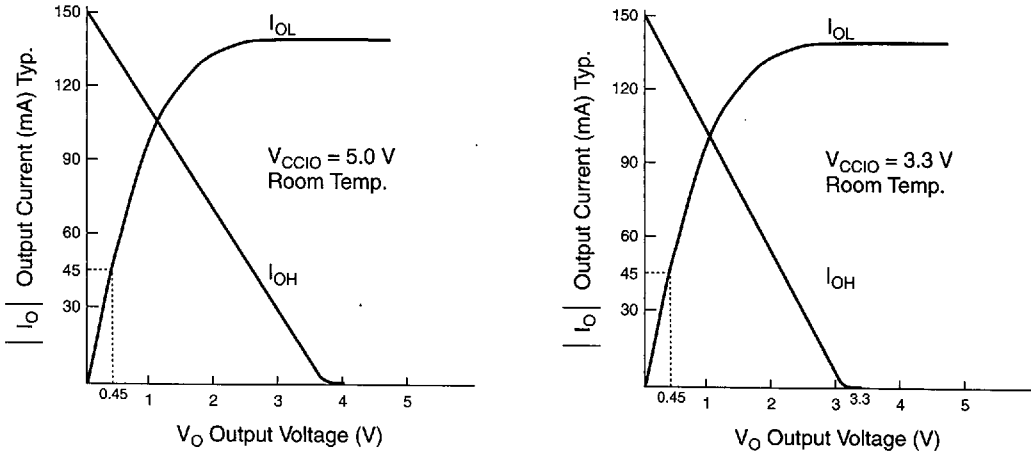
Note:
(1) Output drive characteristics include a JTAG TDO pin.

Timing Model

The continuous, high-performance FastTrack Interconnect routing resources ensure predictable performance and accurate simulation and timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and hence have unpredictable performance. Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time prediction, and device-wide performance analysis.

The MAX 9000 timing model in Figure 13 shows the delays that correspond to various paths and functions in the circuit. This model contains three distinct parts: the macrocell; the IOC; and the interconnect, including the row and column FastTrack Interconnect and LAB local array paths. Each parameter shown in Figure 13 is expressed as a worst-case value in the "Internal Timing Characteristics" tables in this data sheet. Hand-calculations that use the MAX 9000 timing model and these timing parameters can be used to estimate MAX 9000 device performance.

For more information on calculating MAX 9000 timing delays, go to *Application Note 77 (Understanding MAX 9000 Timing)* in this data book.

Figure 13. MAX 9000 Timing Model
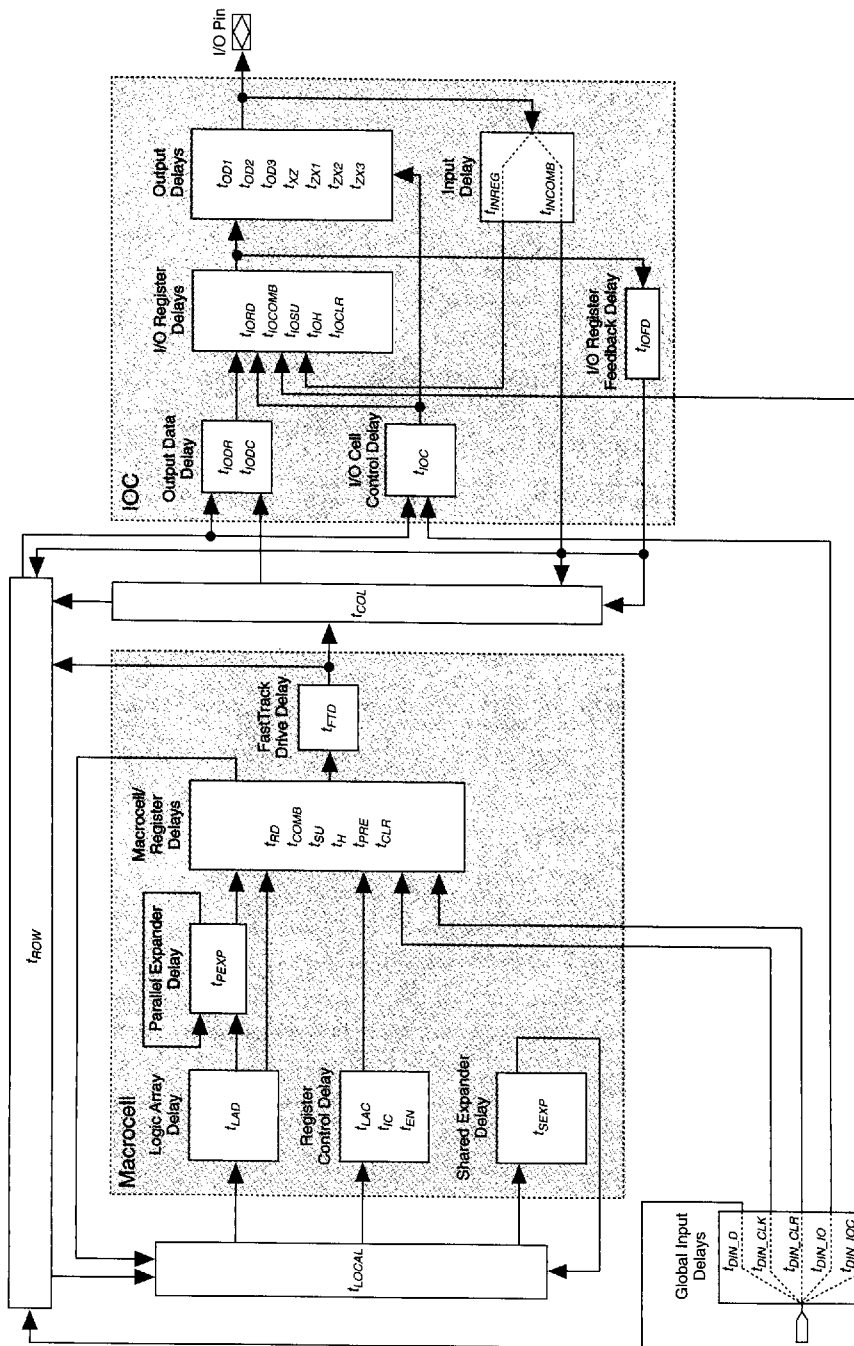
MAX 9000 External Timing Characteristics   Note (1)

Symbol	Parameter	Conditions		-12 Speed Grade (2)		-15 Speed Grade		-20 Speed Grade		
				Min	Max	Min	Max	Min	Max	Unit
t_{PD1}	Row I/O pin input to row I/O pin output	C1 = 35 pF, Note (3)			12.0		15.0		20.0	ns
t_{PD2}	Column I/O pin input to column I/O pin output	C1 = 35 pF	EPM9320		12.8		16.0		23.0	ns
			EPM9400		13.0		16.2		23.2	ns
			EPM9480		13.2		16.4		23.4	ns
			EPM9560		13.4		16.6		23.6	ns
t_{FSU}	Global clock setup time for I/O cell			4.0		5.0		6.0		ns
t_{FH}	Global clock hold time for I/O cell			0.0		0.0		0.0		ns
t_{FCO}	Global clock to I/O cell output delay	C1 = 35 pF			5.5		7.0		8.5	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF, Note (4)		1.0		1.0		1.0		ns
t_{CNT}	Minimum internal global clock period	Note (5)			8.0		8.5		10.0	ns
f_{CNT}	Maximum internal global clock frequency	Note (5)		125.0		117.6		100.0		MHz

MAX 9000 Internal Timing Characteristics   Note (1)

Macrocell Delays				-12 Speed Grade (2)		-15 Speed Grade		-20 Speed Grade		
Symbol	Parameter	Conditions		Min	Max	Min	Max	Min	Max	Unit
t_{LAD}	Logic array delay				3.8		4		4.5	ns
t_{LAC}	Logic control array delay				3.8		4		4.5	ns
t_{IC}	Array clock delay				3.8		4		4.5	ns
t_{EN}	Register enable time				3.8		4		4.5	ns
t_{SEXP}	Shared expander delay				4.1		5		7.5	ns
t_{PEXP}	Parallel expander delay				0.8		1		2	ns
t_{RD}	Register delay				0.8		1		1	ns
t_{COMB}	Combinatorial delay				0.6		1		1	ns
t_{SU}	Register setup time			3.0		3.0		4.0		ns
t_H	Register hold time			2.0		3.5		4.5		ns
t_{PRE}	Register preset time				3.9		4		4.5	ns
t_{CLR}	Register clear time				3.9		4		4.5	ns
t_{FTD}	FastTrack drive delay				0.7		1		2.0	ns
t_{LPA}	Low-power adder	Note (6)			12.0		15.0		20.0	ns

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IOC Delays			-12 Speed Grade *(2)*		-15 Speed Grade		-20 Speed Grade		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Unit
t_{IODR}	I/O row output data delay			0.4		0.2		1.5	ns
t_{IODC}	I/O column output data delay			0.4		0.2		1.5	ns
t_{IOC}	I/O control delay	*Note (7)*		1.2		1.0		2.0	ns
t_{IORD}	I/O register clock-to-output delay			0.7		1.0		1.5	ns
t_{IOCOMB}	I/O combinatorial delay			0.3		1.0		1.5	ns
t_{IOSU}	I/O register setup time before clock		3.0		4.0		5.0		ns
t_{IOH}	I/O register hold time after clock		1.0		1.0		1.0		ns
t_{IOCLR}	I/O register clear delay			2.5		3.0		3.0	ns
t_{IOFD}	I/O register feedback delay			0.0		0.0		0.5	ns
t_{INREG}	I/O input pad and buffer to I/O register delay			3.8		4.5		5.5	ns
t_{INCOMB}	I/O input pad and buffer to row and column delay			1.8		2.0		2.5	ns
t_{OD1}	Output buffer and pad delay, Slow slew rate = off, $V_{CCIO} = 5.0$ V	*Note (8)*		2.0		2.5		2.5	ns
t_{OD2}	Output buffer and pad delay, Slow slew rate = off, $V_{CCIO} = 3.3$ V	*Note (8)*		3.0		3.5		3.5	ns
t_{OD3}	Output buffer and pad delay, Slow slew rate = on, $V_{CCIO} = 5.0$ V or 3.3 V	*Note (8)*		9.0		10.0		10.5	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		2.0		2.5		2.5	ns
t_{ZX1}	Output buffer enable delay, Slow slew rate = off, $V_{CCIO} = 5.0$ V	C1 = 35 pF		2.0		2.5		2.5	ns
t_{ZX2}	Output buffer enable delay, Slow slew rate = off, $V_{CCIO} = 3.3$ V	C1 = 35 pF		3.0		3.5		3.5	ns
t_{ZX3}	Output buffer enable delay, Slow slew rate = on, $V_{CCIO} = 3.3$ V or 5.0 V	C1 = 35 pF		9.0		10.0		10.5	ns

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Interconnect Delays			-12 Speed Grade *(2)*		-15 Speed Grade		-20 Speed Grade		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LOCAL}	LAB local array delay			0.4		0.5		0.5	ns
t_{ROW}	FastTrack row delay	*Note (5)*		1.0		1.4		2.0	ns
t_{COL}	FastTrack column delay	*Note (5)*		1.2		1.7		3.0	ns
t_{DIN_D}	Dedicated input data delay			4.5		4.5		5.0	ns
t_{DIN_CLK}	Dedicated input clock delay			3.0		3.5		4.0	ns
t_{DIN_CLR}	Dedicated input clear delay			4.5		5.0		5.5	ns
t_{DIN_IOC}	Dedicated input I/O register clock delay			2.8		3.5		4.5	ns
t_{DIN_IO}	Dedicated input I/O register control delay			5.5		6.0		6.5	ns

Notes to tables:
(1) Operating conditions: $V_{CCINT} = 5.0$ V $\pm 5\%$, $V_{CCIO} = 5.0$ V $\pm 5\%$ (except where noted).
(2) Timing parameters for the -12 speed grade are preliminary.
(3) Go to *Application Note 77 (Understanding MAX 9000 Timing)* in this data book for more information on test conditions for t_{PD1} and t_{PD2} delays.
(4) This parameter is a guideline that is sample-tested only. It is based on extensive device characterization. This parameter applies for both global and array clocking as well as both macrocell and I/O cell registers.
(5) Measured with a 16-bit loadable, enabled, up/down counter programmed in each LAB.
(6) The t_{LPA} parameter must be added to the t_{LOCAL} parameter for macrocells running in low-power mode.
(7) The t_{ROW}, t_{COL}, and t_{IOC} delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.
(8) Operating conditions: $V_{CCIO} = 5.0$ V $\pm 5\%$ for 5-V operation.
   $V_{CCIO} = 3.3$ V $\pm 10\%$ for 3.3-V operation.

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Power Consumption

Supply power (P) versus frequency (f_{MAX}) for MAX 9000 devices is calculated with the following equation:

$$P = P_{INT} + P_{IO}$$

$$P = I_{CCACTIVE} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)* in this data book. The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic.

The $I_{CCACTIVE}$ value is calculated with the following equation:

$$I_{CCACTIVE} = A \times MC_{TON} + B \times (MC_{DEV} - MC_{TON}) + C \times MC_{USED} \times f_{MAX} \times tog_{LC}$$

The parameters in this equation are as follows:

MC_{TON} = Number of macrocells with Turbo Bit on, as reported in the MAX+PLUS II Report File (.rpt)
MC_{DEV} = Number of macrocells in the device
MC_{USED} = Number of macrocells used in the design, as reported in the MAX+PLUS II Report File (.rpt)
f_{MAX} = Highest clock frequency to the device
tog_{LC} = Average ratio of logic cells toggling at each clock (typically 0.125)
A, B, C = Constants, shown in Table 7

Table 7. MAX 9000 I_{CC} Equation Constants

Device	Constant A	Constant B	Constant C
EPM9320	0.81	0.33	0.056
EPM9400 *(1)*	0.60	0.33	0.053
EPM9480	0.68	0.29	0.064
EPM9560	0.68	0.26	0.052

Note:
(1) This information is preliminary.

This calculation provides an I_{CC} estimate based on typical conditions with no output load, using a typical pattern of a 16-bit, loadable, enabled up/down counter in each LAB. Actual I_{CC} should be verified during operation, because the measurement is sensitive to the actual pattern in the device and the environmental operating conditions.
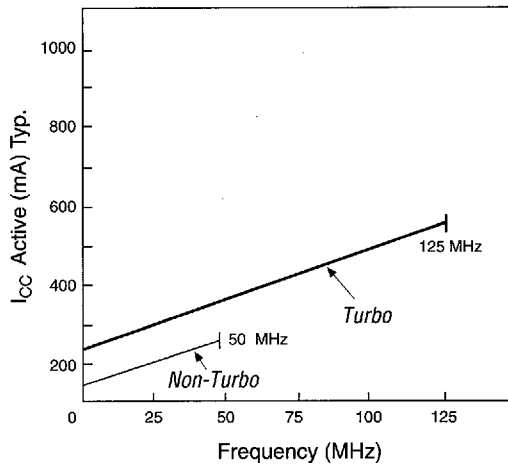
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Figure 14 shows typical supply current versus frequency for MAX 9000 devices.

Figure 14. I_{CC} vs. Frequency for MAX 9000 Devices

EPM9320

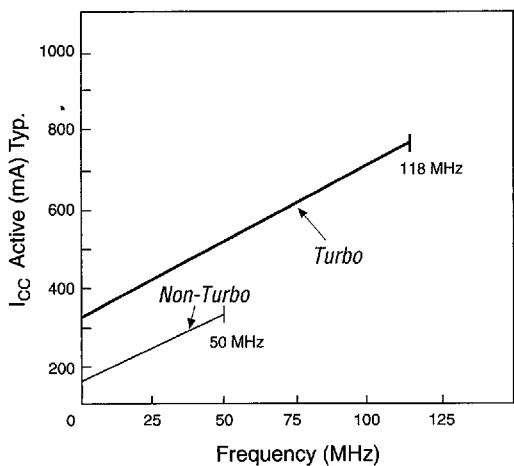
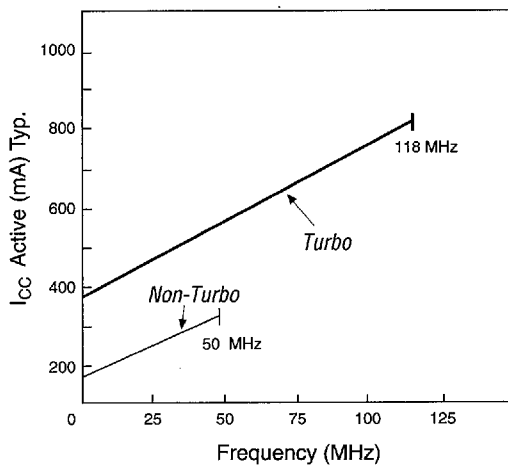
EPM9400

EPM9480

EPM9560

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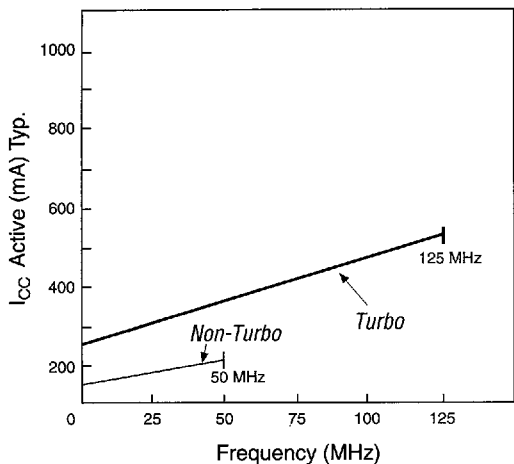
Device Pin-Outs

Tables 8, 9, 10, and 11 show the pin names and numbers for the dedicated pins in each EPM9320, EPM9400, EPM9480, and EPM9560 package, respectively.

Table 8. EPM9320 Dedicated Pin-Outs

Pin Name	84-Pin PLCC (1)	208-Pin RQFP	280-Pin PGA
DIN1 (GCLK1)	1	182	V10
DIN2 (GCLK2)	84	183	U10
DIN3 (GCLR)	13	153	V17
DIN4 (GOE)	72	4	W2
TCK	43	78	A9
TMS	55	49	D6
TDI	42	79	C11
TDO	30	108	A18
GND	6, 18, 24, 25, 48, 61, 67, 70	14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206	D4, D5, D16, E4, E5, E6, E15, E16, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P4, P5, P15, P16, R4, R5, R15, R16, T4, T5, T16
VCCINT (5.0 V only)	14, 21, 28, 57, 64, 71	10, 19, 30, 45, 112, 128, 139, 148	D15, E8, E10, E12, E14, R7, R9, R11, R13, R14, T14
VCCIO (3.3 or 5.0 V)	15, 37, 60, 79	5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195	D14, E7, E9, E11, E13, R6, R8, R10, R12, T13, T15
No Connect (N.C.)	29	6, 7, 8, 9, 11, 12, 13, 15, 16, 17, 18, 109, 140, 141, 142, 144, 145, 146, 147, 149, 150, 151	B6, K19, L2, L4, L18, L19, M1, M2, M3, M4, M16, M17, M18, M19, N1, N2, N3, N4, N16, N17, N18, N19, P1, P2, P3, P17, P18, P19, R1, R2, R3, R17, R18, R19, T1, T2, T3, T17, T18, T19, U1, U2, U3, U17, U18, U19, V1, V2, V19, W1
VPP, Note (2)	56	48	C4

Notes:
(1) Perform a complete thermal analysis before committing a design to this device package. See *Application Note 74* (*Evaluating Power for Altera Devices*) in this data book for more information.
(2) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.

Table 9. EPM9400 Dedicated Pin-Outs

Pin Name	84-Pin PLCC (1)	208-Pin RQFP	240-Pin RQFP
DIN1 (GCLK1)	2	182	210
DIN2 (GCLK2)	1	183	211
DIN3 (GCLR)	12	153	187
DIN4 (GOE)	74	4	234
TCK	43	78	91
TMS	54	49	68
TDI	42	79	92
TDO	31	108	114
GND	6, 13, 20, 26, 27, 47, 60, 66, 69, 73	14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206	5, 14, 25, 34, 45, 54, 65, 66, 81, 96, 110, 115, 126, 127, 146, 147, 166, 167, 186, 200, 216, 229
VCCINT (5.0 V only)	16, 23, 30, 56, 63, 70	10, 19, 30, 45, 112, 128, 139, 148	4, 24, 44, 64, 117, 137, 157, 177
VCCIO (3.3 or 5.0 V)	17, 37, 59, 80	5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195	15, 35, 55, 73, 86, 101, 116, 136, 156, 176, 192, 205, 220, 235
No Connect (N.C.)	–	6, 7, 8, 9, 11, 12, 13, 109, 144, 145, 146, 147, 149, 150, 151	1, 2, 3, 6, 7, 8, 9, 10, 11, 12, 13, 168, 169, 170, 171, 172, 173, 174, 175, 178, 179, 180, 181, 182, 183, 184, 185, 236, 237, 238, 239, 240
VPP, Note (2)	55	48	67

Notes:
(1) Perform a complete thermal analysis before committing a design to this device package. See *Application Note 74 (Evaluating Power for Altera Devices)* in this data book for more information.
(2) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.

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Table 10. EPM9480 Dedicated Pin-Outs

Pin Name	208-Pin RQFP	240-Pin RQFP
DIN1 (GCLK1)	182	210
DIN2 (GCLK2)	183	211
DIN3 (GCLR)	153	187
DIN4 (GOE)	4	234
TCK	78	91
TMS	49	68
TDI	79	92
TDO	108	114
GND	14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206	5, 14, 25, 34, 45, 54, 65, 66, 81, 96, 110, 115, 126, 127, 146, 147, 166, 167, 186, 200, 216, 229
VCCINT (5.0 V only)	10, 19, 30, 45, 112, 128, 139, 148	4, 24, 44, 64, 117, 137, 157, 177
VCCIO (3.3 or 5.0 V)	5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195	15, 35, 55, 73, 86, 101, 116, 136, 156, 176, 192, 205, 220, 235
No Connect (N.C.)	6, 7, 8, 9, 109, 149, 150, 151	1, 2, 3, 178, 179, 180, 181, 182, 183, 184, 185, 236, 237, 238, 239, 240
VPP, Note (1)	48	67

Note:
(1)   During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.

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Table 11. EPM9560 Dedicated Pin-Outs

Pin Name	208-Pin CQFP	240-Pin RQFP	280-Pin PGA	304-Pin RQFP
DIN1 (GCLK1)	182	210	V10	266
DIN2 (GCLK2)	183	211	U10	267
DIN3 (GCLR)	153	187	V17	237
DIN4 (GOE)	4	234	W2	296
TCK	78	91	A9	114
TMS	49	68	D6	85
TDI	79	92	C11	115
TDO	108	114	A18	144
GND	14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206	5, 14, 25, 34, 45, 54, 65, 66, 81, 96, 110, 115, 126, 127, 146, 147, 166, 167, 186, 200, 216, 229	D4, D5, D16, E4, E5, E6, E15, E16, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P4, P5, P15, P16, R4, R5, R15, R16, T4, T5, T16	13, 22, 33, 42, 53, 62, 73, 74, 102, 121, 138, 155, 166, 167, 186, 187, 206, 207, 226, 254, 273, 290
VCCINT (5.0 V only)	10, 19, 30, 45, 112, 128, 139, 148	4, 24, 44, 64, 117, 137, 157, 177	D15, E8, E10, E12, E14, R7, R9, R11, R13, R14, T14	12, 32, 52, 72, 157, 177, 197, 217
VCCIO (3.3 or 5.0 V)	5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195	15, 35, 55, 73, 86, 101, 116, 136, 156, 176, 192, 205, 220, 235	D14, E7, E9, E11, E13, R6, R8, R10, R12, T13, T15	3, 23, 43, 63, 91, 108, 127, 156, 176, 196, 216, 243, 260, 279
No Connect (N.C.)	109	–	B6, W1	1, 2, 76, 77, 78, 79, 80, 81, 82, 83, 84, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 227, 228, 229, 230, 231, 232, 233, 234, 235, 236, 297, 298, 299, 300, 301, 302, 303, 304
VPP, Note (1)	48	67	C4	75

Note:
(1) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.

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