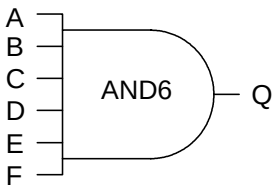
AND6 is a 6-input AND gate with 1x drive strength.

Truth Table

A	B	C	D	E	F	Q
L	X	X	X	X	X	L
X	L	X	X	X	X	L
X	X	L	X	X	X	L
X	X	X	L	X	X	L
X	X	X	X	L	X	L
X	X	X	X	X	L	L
H	H	H	H	H	H	H



Capacitance

	Ci (pF)
A	0.050
B	0.043
C	0.047
D	0.050
E	0.043
F	0.047

Area

1.08 $mils^2$

Power

2.83 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(L) with L = Output Load [pF]

AC Characteristics : Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

Characteristics	Symbol	SL = 0.1			SL = 2.0		
		L = 0.1	L = 0.7	L = 1.0	L = 0.1	L = 0.7	L = 1.0
Delay A to Q	tpdar	0.54	1.84	2.58	0.59	1.89	2.58
	tpdaf	0.58	1.68	2.21	0.91	2.01	2.55
Delay B to Q	tpdbr	0.57	1.88	2.60	0.58	1.89	2.56
	tpdbf	0.64	1.73	2.28	0.99	2.12	2.67
Delay C to Q	tpdcr	0.57	1.88	2.60	0.54	1.83	2.47
	tpdcf	0.70	1.77	2.35	1.06	2.20	2.71
Delay D to Q	tpddr	0.54	1.92	2.51	0.60	1.89	2.57
	tpddf	0.60	1.69	2.21	0.95	2.01	2.53
Delay E to Q	tpder	0.58	1.95	2.59	0.57	1.87	2.56
	tpdef	0.66	1.75	2.28	1.02	2.11	2.62
Delay F to Q	tpdfr	0.59	1.95	2.56	0.53	1.83	2.51
	tpdff	0.72	1.83	2.33	1.11	2.19	2.74
Output Slope A to Q	op_slar	1.07	5.32	7.46	1.02	5.28	7.37
	op_slaf	0.75	3.78	5.05	0.73	3.62	5.02
Output Slope B to Q	op_slbr	1.08	5.31	7.43	1.05	5.31	7.37
	op_slbf	0.75	3.61	5.07	0.77	3.70	5.27

Characteristics	Symbol	SL = 0.1			SL = 2.0		
		L = 0.1	L = 0.7	L = 1.0	L = 0.1	L = 0.7	L = 1.0
Output Slope C to Q	op_slcr	1.08	5.31	7.46	1.05	5.30	7.37
	op_slcf	0.78	3.60	5.10	0.81	3.66	4.98
Output Slope D to Q	op_sldr	1.08	5.31	7.50	1.02	5.30	7.37
	op_sldf	0.81	3.67	4.97	0.83	3.65	4.96
Output Slope E to Q	op_sler	1.07	5.32	7.47	1.02	5.28	7.37
	op_slef	0.82	3.58	4.98	0.83	3.60	4.97
Output Slope F to Q	op_slfr	1.05	5.32	7.55	1.05	5.30	7.35
	op_slff	0.85	3.70	4.92	0.86	3.60	4.92